



1. Description

1.1. Project

Project Name	stm32work
Board Name	custom
Generated with:	STM32CubeMX 6.5.0
Date	07/20/2022

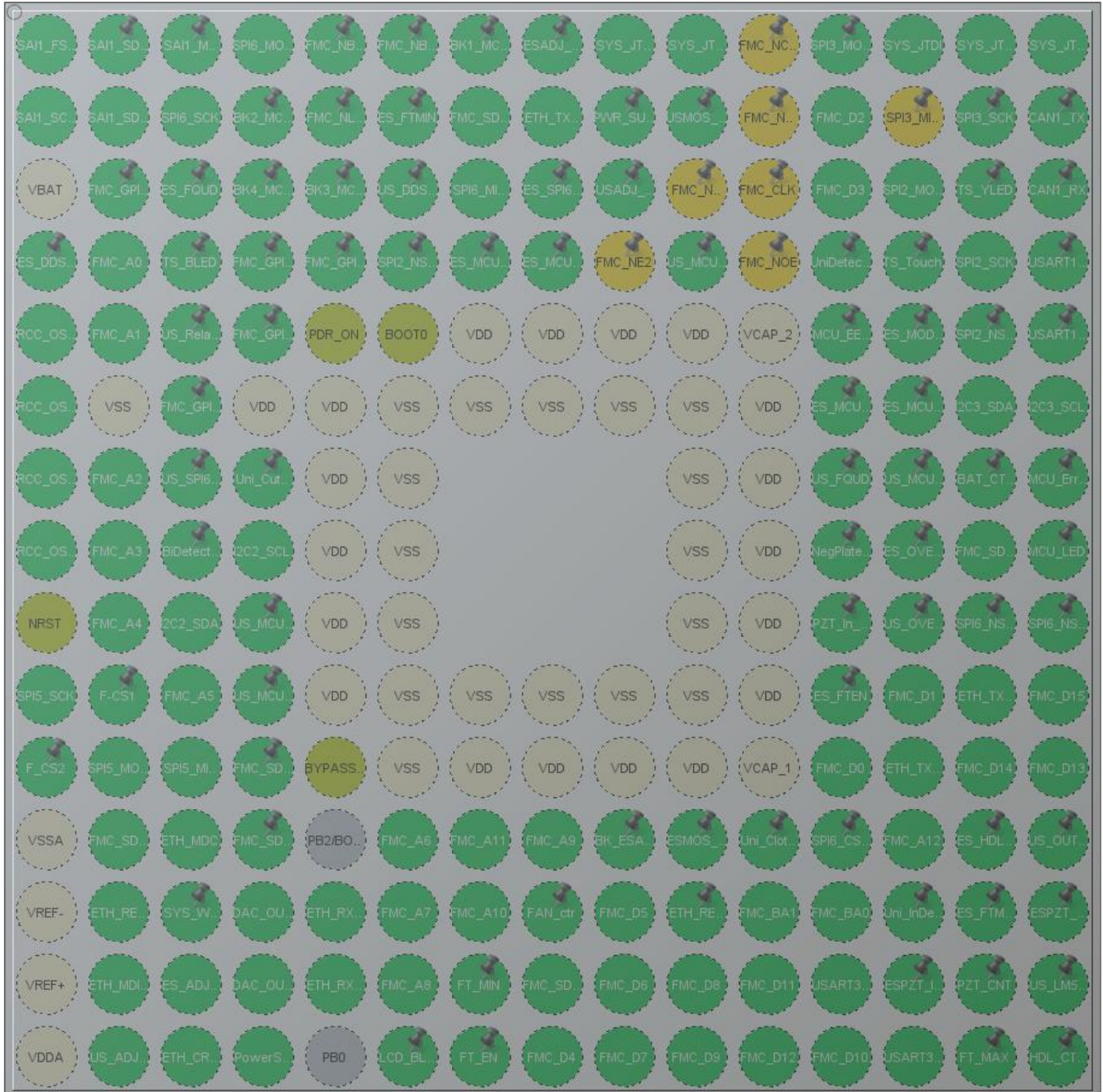
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429NIHx
MCU Package	TFBGA216
MCU Pin number	216

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration



TFBGA216 (Top view)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE4	I/O	SAI1_FS_A	
A2	PE3	I/O	SAI1_SD_B	
A3	PE2	I/O	SAI1_MCLK_A	
A4	PG14	I/O	SPI6_MOSI	
A5	PE1	I/O	FMC_NBL1	
A6	PE0	I/O	FMC_NBL0	
A7	PB8 *	I/O	GPIO_Output	BK1_MCU_FPGA
A8	PB5 *	I/O	GPIO_Output	ESADJ_CTRL
A9	PB4	I/O	SYS_JTRST	
A10	PB3	I/O	SYS_JTDO-SWO	
A11	PD7 **	I/O	FMC_NCE2	
A12	PC12	I/O	SPI3_MOSI	
A13	PA15	I/O	SYS_JTDI	
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
B1	PE5	I/O	SAI1_SCK_A	
B2	PE6	I/O	SAI1_SD_A	
B3	PG13	I/O	SPI6_SCK	
B4	PB9 *	I/O	GPIO_Output	BK2_MCU_FPGA
B5	PB7 *	I/O	GPIO_Output	FMC_NL-NADV
B6	PB6 *	I/O	GPIO_Input	ES_FTMIN
B7	PG15	I/O	FMC_SDNCAS	
B8	PG11	I/O	ETH_TX_EN	
B9	PJ13 *	I/O	GPIO_Input	PWR_SUPV
B10	PJ12 *	I/O	GPIO_Output	USMOS_EN
B11	PD6 **	I/O	FMC_NWAIT	
B12	PD0	I/O	FMC_D2	
B13	PC11 **	I/O	SPI3_MISO	
B14	PC10	I/O	SPI3_SCK	
B15	PA12	I/O	CAN1_TX	
C1	VBAT	Power		
C2	PI8 *	I/O	GPIO_Output	FMC_GPIO2
C3	PI4 *	I/O	GPIO_Output	ES_FQUD
C4	PK7 *	I/O	GPIO_Output	BK4_MCU_FPGA
C5	PK6 *	I/O	GPIO_Output	BK3_MCU_FPGA
C6	PK5 *	I/O	GPIO_Output	US_DDSRST

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
C7	PG12	I/O	SPI6_MISO	
C8	PG10 *	I/O	GPIO_Output	ES_SPI6_MISO_OE
C9	PJ14 *	I/O	GPIO_Output	USADJ_ctrl
C10	PD5 **	I/O	FMC_NWE	
C11	PD3 **	I/O	FMC_CLK	
C12	PD1	I/O	FMC_D3	
C13	PI3	I/O	SPI2_MOSI	
C14	PI2 *	I/O	GPIO_Output	TS_YLED
C15	PA11	I/O	CAN1_RX	
D1	PC13 *	I/O	GPIO_Output	ES_DDSRST
D2	PF0	I/O	FMC_A0	
D3	PI5 *	I/O	GPIO_Output	TS_BLED
D4	PI7 *	I/O	GPIO_Output	FMC_GPIO1
D5	PI10 *	I/O	GPIO_Output	FMC_GPIO4
D6	PI6 *	I/O	GPIO_Output	SPI2_NSS_ES_DAC
D7	PK4 *	I/O	GPIO_Output	ES_MCU Spare2
D8	PK3 *	I/O	GPIO_Output	ES_MCU Spare1
D9	PG9 **	I/O	FMC_NE2	
D10	PJ15 *	I/O	GPIO_Output	US_MCU Spare3
D11	PD4 **	I/O	FMC_NOE	
D12	PD2 *	I/O	GPIO_Output	UniDetect_EN
D13	PH15 *	I/O	GPIO_Input	TS_Touch
D14	PI1	I/O	SPI2_SCK	
D15	PA10	I/O	USART1_RX	
E1	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
E2	PF1	I/O	FMC_A1	
E3	PI12 *	I/O	GPIO_Output	US_RelayCtrl
E4	PI9 *	I/O	GPIO_Output	FMC_GPIO3
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDD	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
E12	PH13 *	I/O	GPIO_Input	MCU_EEPROM
E13	PH14 *	I/O	GPIO_Output	ES_MOD_SW
E14	PI0 *	I/O	GPIO_Output	SPI2_NSS_US_DAC
E15	PA9	I/O	USART1_TX	

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F1	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
F2	VSS	Power		
F3	PI11 *	I/O	GPIO_Output	FMC_GPIO5
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F12	PK1 *	I/O	GPIO_Output	ES_MCU Spare3
F13	PK2 *	I/O	GPIO_Output	ES_MCU Spare4
F14	PC9	I/O	I2C3_SDA	
F15	PA8	I/O	I2C3_SCL	
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	PF2	I/O	FMC_A2	
G3	PI13 *	I/O	GPIO_Output	US_SPI6_MISO_OE
G4	PI15 *	I/O	GPIO_Input	Uni_CutBtn
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDD	Power		
G12	PJ11 *	I/O	GPIO_Output	US_FQUD
G13	PK0 *	I/O	GPIO_Output	US_MCU Spare4
G14	PC8 *	I/O	GPIO_Output	BAT_CTRL
G15	PC7 *	I/O	GPIO_Output	MCU_ErrorLED
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3	I/O	FMC_A3	
H3	PI14 *	I/O	GPIO_Output	BiDetect_EN
H4	PH4	I/O	I2C2_SCL	
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDD	Power		
H12	PJ8 *	I/O	GPIO_Input	NegPlate_InsDect
H13	PJ10 *	I/O	GPIO_Input	ES_OVERCurrent
H14	PG8	I/O	FMC_SDCLK	
H15	PC6 *	I/O	GPIO_Output	MCU_LED

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J1	NRST	Reset		
J2	PF4	I/O	FMC_A4	
J3	PH5	I/O	I2C2_SDA	
J4	PH3 *	I/O	GPIO_Output	US_MCU Spare2
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
J12	PJ7 *	I/O	GPIO_Input	PZT_In_Dect
J13	PJ9 *	I/O	GPIO_Input	US_OVERCurren
J14	PG7 *	I/O	GPIO_Output	SPI6_NSS_ES
J15	PG6 *	I/O	GPIO_Output	SPI6_NSS_US
K1	PF7	I/O	SPI5_SCK	
K2	PF6 *	I/O	GPIO_Output	F-CS1
K3	PF5	I/O	FMC_A5	
K4	PH2 *	I/O	GPIO_Output	US_MCU Spare1
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K12	PJ6 *	I/O	GPIO_Input	ES_FTEN
K13	PD15	I/O	FMC_D1	
K14	PB13	I/O	ETH_TXD1	
K15	PD10	I/O	FMC_D15	
L1	PF10 *	I/O	GPIO_Output	F_CS2
L2	PF9	I/O	SPI5_MOSI	
L3	PF8	I/O	SPI5_MISO	
L4	PC3	I/O	FMC_SDCKE0	
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
L12	PD14	I/O	FMC_D0	

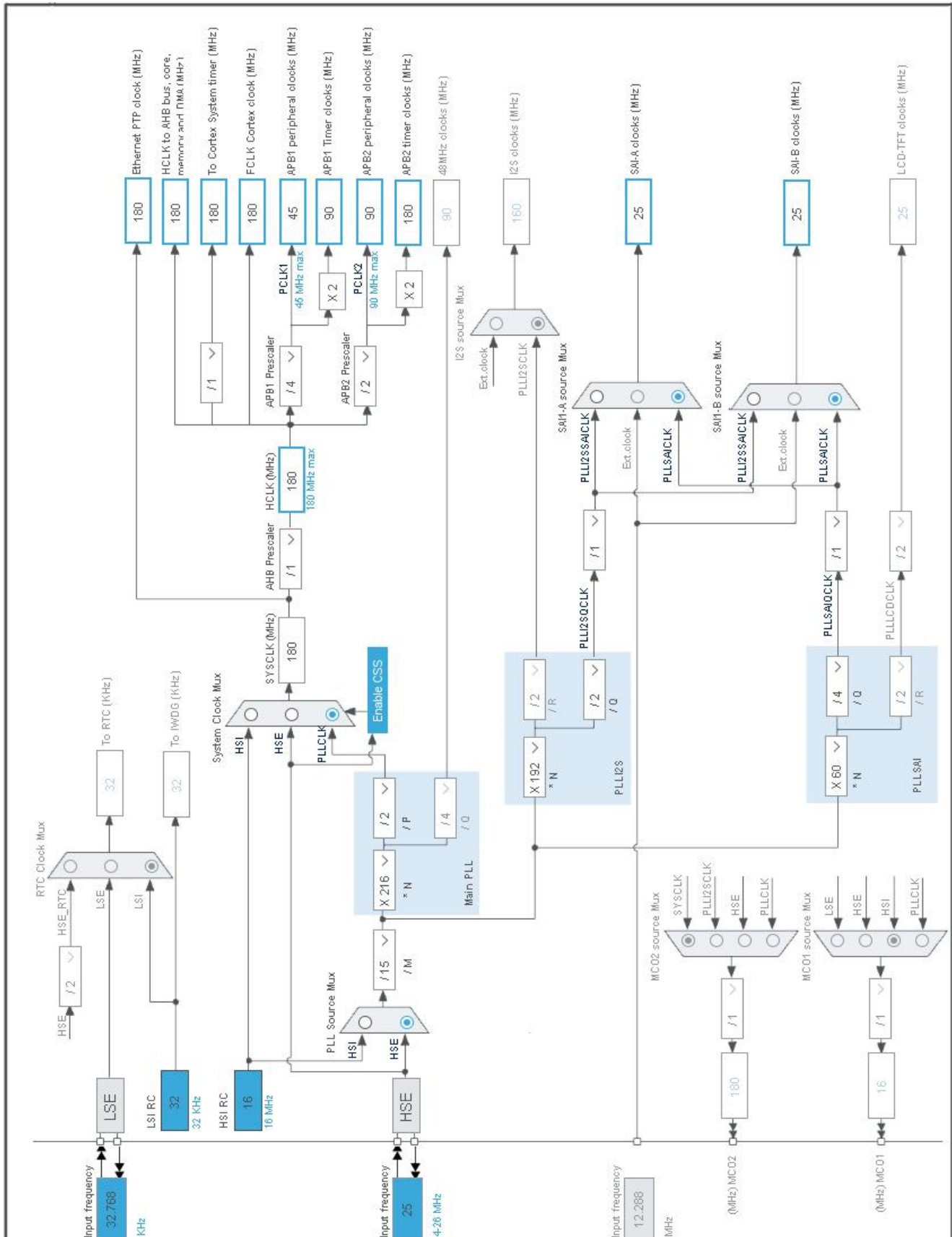
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
L13	PB12	I/O	ETH_TXD0	
L14	PD9	I/O	FMC_D14	
L15	PD8	I/O	FMC_D13	
M1	VSSA	Power		
M2	PC0	I/O	FMC_SDNWE	
M3	PC1	I/O	ETH_MDC	
M4	PC2	I/O	FMC_SDNE0	
M6	PF12	I/O	FMC_A6	
M7	PG1	I/O	FMC_A11	
M8	PF15	I/O	FMC_A9	
M9	PJ4 *	I/O	GPIO_Output	BK_ESADJ_SW
M10	PD12 *	I/O	GPIO_Output	ESMOS_EN
M11	PD13 *	I/O	GPIO_Input	Uni_ClotBtn
M12	PG3 *	I/O	GPIO_Output	SPI6_CS_PG3_ES
M13	PG2	I/O	FMC_A12	
M14	PJ5 *	I/O	GPIO_Output	ES_HDLctrl
M15	PH12 *	I/O	GPIO_Output	US_OUT_SW
N1	VREF-	Power		
N2	PA1	I/O	ETH_REF_CLK	
N3	PA0/WKUP	I/O	SYS_WKUP	
N4	PA4	I/O	DAC_OUT1	
N5	PC4	I/O	ETH_RXD0	
N6	PF13	I/O	FMC_A7	
N7	PG0	I/O	FMC_A10	
N8	PJ3 *	I/O	GPIO_Output	FAN_ctr
N9	PE8	I/O	FMC_D5	
N10	PD11 *	I/O	GPIO_Output	ETH_RESET
N11	PG5	I/O	FMC_BA1	
N12	PG4	I/O	FMC_BA0	
N13	PH7 *	I/O	GPIO_Input	Uni_InDect
N14	PH9 *	I/O	GPIO_Input	ES_FTMAX
N15	PH11 *	I/O	GPIO_Input	ESPZT_CNT
P1	VREF+	Power		
P2	PA2	I/O	ETH_MDIO	
P3	PA6	I/O	ADC1_IN6	ES_ADJ_FDBK
P4	PA5	I/O	DAC_OUT2	
P5	PC5	I/O	ETH_RXD1	
P6	PF14	I/O	FMC_A8	
P7	PJ2 *	I/O	GPIO_Input	FT_MIN

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
P8	PF11	I/O	FMC_SDNRAS	
P9	PE9	I/O	FMC_D6	
P10	PE11	I/O	FMC_D8	
P11	PE14	I/O	FMC_D11	
P12	PB10	I/O	USART3_TX	
P13	PH6 *	I/O	GPIO_Input	ESPZT_InDect
P14	PH8 *	I/O	GPIO_Input	PZT_CNT
P15	PH10 *	I/O	GPIO_Output	US_LM5085_SW
R1	VDDA	Power		
R2	PA3	I/O	ADC1_IN3	US_ADJ_FDBK
R3	PA7	I/O	ETH_CRS_DV	
R4	PB1	I/O	ADC1_IN9	PowerSupplyV
R6	PJ0 *	I/O	GPIO_Output	LCD_BL_Ctrl
R7	PJ1 *	I/O	GPIO_Input	FT_EN
R8	PE7	I/O	FMC_D4	
R9	PE10	I/O	FMC_D7	
R10	PE12	I/O	FMC_D9	
R11	PE15	I/O	FMC_D12	
R12	PE13	I/O	FMC_D10	
R13	PB11	I/O	USART3_RX	
R14	PB14 *	I/O	GPIO_Input	FT_MAX
R15	PB15 *	I/O	GPIO_Output	HDL_CTRL

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	stm32work
Project Folder	G:\stm32work
Toolchain / IDE	MDK-ARM V5.32
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x1000
Minimum Stack Size	0x1000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_FMC_Init	FMC
4	MX_ADC1_Init	ADC1
5	MX_CAN1_Init	CAN1
6	MX_DAC_Init	DAC
7	MX_I2C2_Init	I2C2
8	MX_I2C3_Init	I2C3
9	MX_SAI1_Init	SAI1
10	MX_SPI2_Init	SPI2
11	MX_SPI3_Init	SPI3

Rank	Function Name	Peripheral Instance Name
12	MX_SPI5_Init	SPI5
13	MX_SPI6_Init	SPI6
14	MX_USART1_UART_Init	USART1
15	MX_LWIP_Init	LWIP
16	MX_DMA_Init	DMA
17	MX_TIM7_Init	TIM7
18	MX_USART3_UART_Init	USART3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429NIHx
Datasheet	DS9405_Rev9

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

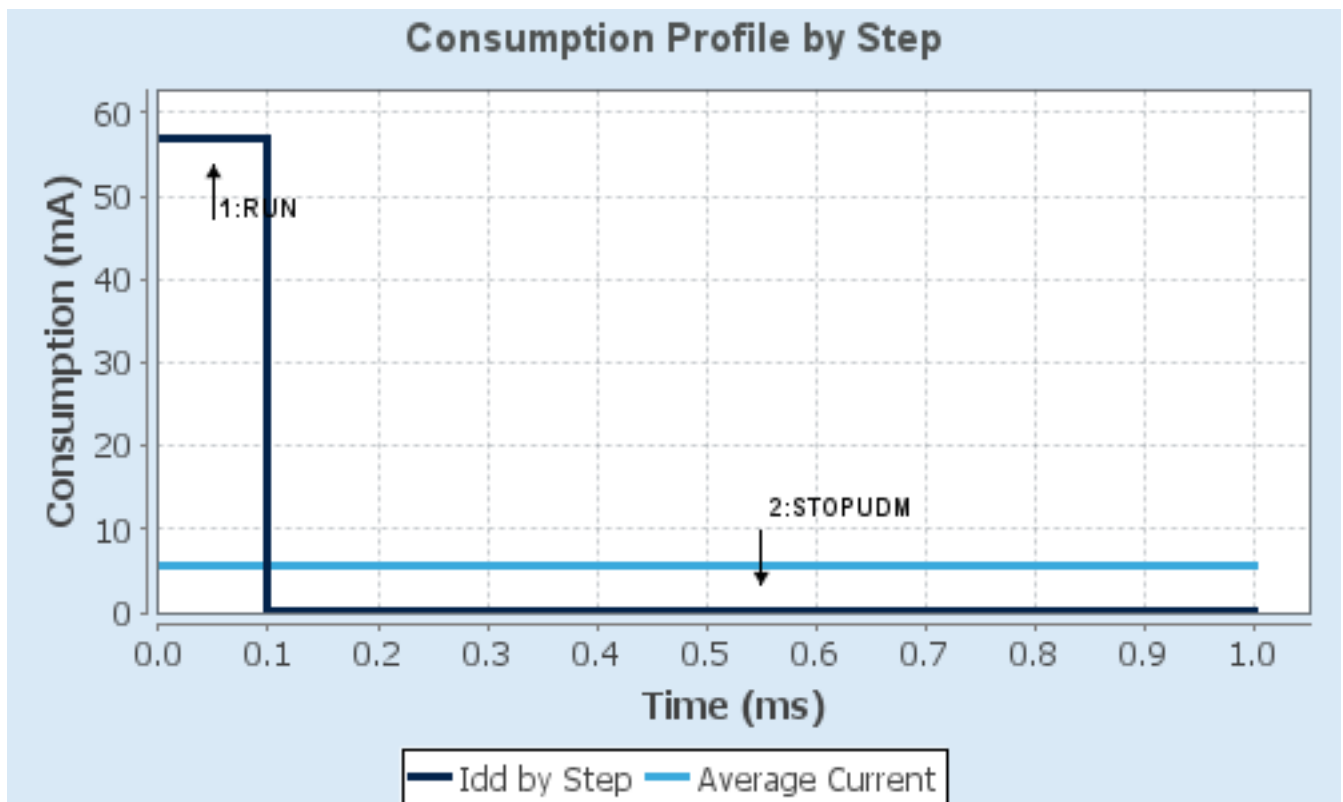
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	57 mA	100 μ A
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	99.55	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	5.79 mA
Battery Life	24 days, 10 hours	Average DMIPS	225.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN3

mode: IN6

mode: IN9

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Enabled

Continuous Conversion Mode **Enabled ***

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled ***

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 3

Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions **2 ***

External Trigger Source Injected Conversion launched by software

External Trigger Edge None

Injected Conversion Mode None

Injected Rank 1

Channel Channel 3

Sampling Time 3 Cycles

Injected Offset 0

Injected Rank **2 ***

Channel **Channel 6 ***

Sampling Time 3 Cycles

Injected Offset 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. CAN1

mode: Activated

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	355.55555555555554 *
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	1066 *
Baud Rate	937500 *
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal
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7.3. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

7.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Disable *
Trigger	None

DAC Out2 Settings:

Output Buffer	Disable *
Trigger	None

7.4. ETH

Mode: RMII

7.4.1. Parameter Settings:

General : Ethernet Configuration:

Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Rx Buffers Length	1536

Ethernet Basic Configuration:

Rx Mode	Interrupt Mode
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7.4.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Reset delay these values are based on a 1 ms SysTick interrupt	0x000000FF *
PHY Configuration delay	0x000000FF *
PHY Read TimeOut	0x0000FFFF *
PHY Write TimeOut	0x0000FFFF *

Common : External PHY Configuration:

Transceiver Basic Control Register	0x00 *
Transceiver Basic Status Register	0x01 *
PHY Reset	0x8000 *
Select loop-back mode	0x4000 *
Set the full-duplex mode at 100 Mb/s	0x2100 *
Set the half-duplex mode at 100 Mb/s	0x2000 *
Set the full-duplex mode at 10 Mb/s	0x0100 *
Set the half-duplex mode at 10 Mb/s	0x0000 *
Enable auto-negotiation function	0x1000 *
Restart auto-negotiation function	0x0200 *
Select the power down mode	0x0800 *
Isolate PHY from MII	0x0400 *
Auto-Negotiation process completed	0x0020 *
Valid link established	0x0004 *

Jabber condition detected **0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset **0x10 ***
 PHY Speed mask **0x0002 ***
 PHY Duplex mask **0x0004 ***
 PHY Interrupt Source Flag register Offset **0x001D ***
 PHY Link down interrupt **0x000B ***

7.5. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 13 bits

Data: 16 bits

Byte enable: 16-bit byte enable

7.5.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	9 bits *
Number of row address bits	13 bits
CAS latency	3 memory clock cycles *
Write protection	Disabled
SDRAM common clock	2 HCLK clock cycles *
SDRAM common burst read	Enabled *
SDRAM common read pipe delay	1 HCLK clock cycle *

SDRAM timing in memory clock cycles:

Load mode register to active delay	2 *
Exit self-refresh delay	8 *
Self-refresh time	6 *
SDRAM common row cycle delay	6 *
Write recovery time	4 *
SDRAM common row precharge delay	2 *
Row to column delay	2 *

7.6. I2C2

I2C: I2C

7.6.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Timing configuration:

Coefficient of Digital Filter	0
Analog Filter	Enabled

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.7. I2C3

I2C: I2C

7.7.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Timing configuration:

Coefficient of Digital Filter	0
Analog Filter	Enabled

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.8.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

7.9. SAI1

SAI_A Mode: Master with Master Clock Out

SAI_B Mode: Synchronous Slave

7.9.1. Parameter Settings:

SAI A:

Basic Parameters

Protocol	Free
Audio Mode	Master Transmit
Frame Length	64 bits *
Data Size	24 Bits
Slot Size	32 Bits *

Frame Parameters

First Bit	MSB First
Frame Synchro Active Level Length	32 *
Frame Synchro Definition	Channel Identification *
Frame Synchro Polarity	Active Low
Frame Synchro Offset	Before First Bit *

Slot Parameters

First Bit Offset	0
Number of Slots (only Even Values)	2
Slot Active Final Value	0x0000FFFF *
Slot Active	All *

Clock Parameters

Clock Source	SAI PLL Clock
Master Clock Divider	Enabled
Audio Frequency	44 KHz *
Real Audio Frequency	48.828 KHz *
Error between Selected	10.97 % *
Clock Strobing	Falling Edge

Advanced Parameters

Fifo Threshold	One Quarter Full *
Output Drive	Enabled *

SAI B:

Basic Parameters

Protocol	Free
Audio Mode	Slave Receive
Frame Length (only Even Values)	64 *
Data Size	24 Bits
Slot Size	32 Bits *

Frame Parameters

First Bit	MSB First
Frame Synchro Active Level Length	32 *
Frame Synchro Definition	Channel Identification *
Frame Synchro Polarity	Active Low
Frame Synchro Offset	Before First Bit *

Slot Parameters

First Bit Offset	0
Number of Slots (only Even Values)	2
Slot Active Final Value	0x00000000
Slot Active	User Setting *
Slot 0 Active	0
Slot 1 Active	0

Clock Parameters

Clock Strobing	Falling Edge
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Advanced Parameters

Fifo Threshold	Empty
Output Drive	Disabled

7.10. SPI2

Mode: Half-Duplex Master

7.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	22.5 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.11. SPI3

Mode: Transmit Only Master

7.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	LSB First *

Clock Parameters:

Prescaler (for Baud Rate)	8 *
Baud Rate	5.625 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.12. SPI5

Mode: Full-Duplex Master

7.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	128 *
Baud Rate	703.125 KBits/s *
Clock Polarity (CPOL)	High *
Clock Phase (CPHA)	2 Edge *

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.13. SPI6

Mode: Full-Duplex Master

7.13.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	45.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.14. SYS

Debug: JTAG (5 pins)

mode: System Wake-Up

Timebase Source: TIM12

7.15. TIM7

mode: Activated

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	179 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	999 *
auto-reload preload	Enable *

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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7.16. USART1

Mode: Asynchronous

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.17. USART3

Mode: Asynchronous

7.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.18. FREERTOS

Interface: CMSIS_V2

7.18.1. Config parameters:

API:

FreeRTOS API	CMSIS v2
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Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Enabled *

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

7.18.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled

vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Enabled *
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.18.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT Disabled

Project settings (see parameter description first):

Use FW pack heap file Enabled

7.19. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.19.1. General Settings:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **) 2.1.2

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module) Disabled

IP Address Settings:

IP_ADDRESS (IP Address) **192.168.000.001 ***

NETMASK_ADDRESS (Netmask Address) **255.255.255.255 ***

GATEWAY_ADDRESS (Gateway Address)	192.168.000.254 *
RTOS Dependency:	
WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Enabled
CMSIS_VERSION (CMSIS API Version used)	CMSIS v2
Platform Settings:	
PHY Driver	Choose/LAN8742/DP83848
Protocols Options:	
LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Disabled *
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.19.2. Key Options:

Infrastructure - OS Awareness Option:	
NO_SYS (OS Awareness)	OS Used
Infrastructure - Timers Options:	
LWIP_TIMERS (Use Support For sys_timeout)	Enabled
Infrastructure - Core Locking and MPU Options:	
SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled
Infrastructure - Heap and Memory Pools Options:	
MEM_SIZE (Heap Memory Size)	1600
LWIP_RAM_HEAP_POINTER (RAM Heap Pointer)	0x30044000 *
Infrastructure - Internal Memory Pool Sizes:	
MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1
Pbuf Options:	
PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592
IPv4 - ARP Options:	
LWIP_ARP (ARP Functionality)	Enabled
Callback - TCP Options:	
TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144

TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled
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Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	24
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled
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Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0
LWIP_SOCKET_SELECT (Select for Socket)	Enabled
LWIP_SOCKET_POLL (Poll for Socket)	Enabled

7.19.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled
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7.19.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled
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7.19.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **) Disabled

7.19.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent) Disabled

7.19.7. SNTP/SMTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **) Disabled

SMTP Options:

LWIP_SMTP (LWIP SMTP Support ** CubeMX specific **) Disabled

7.19.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **) Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **) Disabled

7.19.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks) Disabled

LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks) Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP) Disabled

7.19.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statistic Collection) Disabled

7.19.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Enabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Enabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Enabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.19.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All
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7.19.13. Platform Settings:

Driver_PHY	LAN8742
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* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	ES_ADJ_FDBK
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	US_ADJ_FDBK
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	PowerSupplyV
CAN1	PA12	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA11	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	
ETH	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC2	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C2	PH4	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PH5	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SAI1	PE4	SAI1_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE3	SAI1_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE2	SAI1_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	SAI1_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PI3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PI1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI3	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI6	PG14	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PG13	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PG12	SPI6_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PB4	SYS_JTRST	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
	PA15	SYS_JTDI	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS-	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
		SWDIO				
	PA0/WKUP	SYS_WKUP	n/a	n/a	n/a	
USART1	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
Single Mapped Signals	PD7	FMC_NCE2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD6	FMC_NWAIT	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD3	FMC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG9	FMC_NE2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PB8	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	High *	BK1_MCU_FPGA
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ESADJ_CTRL
	PB9	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Very High *	BK2_MCU_FPGA
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FMC_NL-NADV
	PB6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ES_FTMIN
	PJ13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PWR_SUPV
	PJ12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USMOS_EN
	PI8	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	FMC_GPIO2
	PI4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ES_FQUD
	PK7	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	BK4_MCU_FPGA
	PK6	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	BK3_MCU_FPGA
	PK5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	US_DDSRST
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ES_SPI6_MISO_OE
	PJ14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USADJ_ctrl
	PI2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TS_YLED
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ES_DDSRST
	PI5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TS_BLED
	PI7	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	FMC_GPIO1
	PI10	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	FMC_GPIO4

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PI6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_NSS_ES_DAC
	PK4	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	ES_MCUSpare2
	PK3	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	ES_MCUSpare1
	PJ15	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	US_MCUSpare3
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UniDetect_EN
	PH15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TS_Touch
	PI12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	US_RelayCtrl
	PI9	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	FMC_GPIO3
	PH13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	MCU_EEPROM
	PH14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ES_MOD_SW
	PI0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_NSS_US_DAC
	PI11	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	FMC_GPIO5
	PK1	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	ES_MCUSpare3
	PK2	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	ES_MCUSpare4
	PI13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	US_SPI6_MISO_OE
	PI15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Uni_CutBtn
	PJ11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	US_FQUD
	PK0	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	US_MCUSpare4
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BAT_CTRL
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MCU_ErrorLED
	PI14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BiDetect_EN
	PJ8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NegPlate_InsDect
	PJ10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ES_OVERCurrent
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MCU_LED
	PH3	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	US_MCUSpare2
	PJ7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PZT_In_Dect
	PJ9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	US_OVERCurren
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI6_NSS_ES
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI6_NSS_US
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	F-CS1
	PH2	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	US_MCUSpare1
	PJ6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ES_FTEN
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	F_CS2
	PJ4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BK_ESADJ_SW
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ESMOS_EN
	PD13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Uni_ClotBtn
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI6_CS_PG3_ES
	PJ5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ES_HDLctrl

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PH12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	US_OUT_SW
	PJ3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FAN_ctr
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ETH_RESET
	PH7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Uni_InDect
	PH9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ES_FTMAX
	PH11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ESPZT_CNT
	PJ2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	FT_MIN
	PH6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ESPZT_InDect
	PH8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PZT_CNT
	PH10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	US_LM5085_SW
	PJ0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_BL_Ctrl
	PJ1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	FT_EN
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	FT_MAX
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	HDL_CTRL

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low
SAI1_A	DMA2_Stream1	Memory To Peripheral	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode: Normal
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Half Word
 Memory Data Width: Half Word

SAI1_A: DMA2_Stream1 DMA request Settings:

Mode: Normal
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Word
 Memory Data Width: Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
I2C2 event interrupt	true	5	0
I2C2 error interrupt	true	5	0
USART1 global interrupt	true	5	0
USART3 global interrupt	true	5	0
TIM8 break interrupt and TIM12 global interrupt	true	15	0
TIM7 global interrupt	true	5	0
DMA2 stream0 global interrupt	true	5	0
DMA2 stream1 global interrupt	true	5	0
Ethernet global interrupt	true	5	0
I2C3 event interrupt	true	5	0
I2C3 error interrupt	true	5	0
SAI1 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
CAN1 TX interrupts	unused		
CAN1 RX0 interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
SPI2 global interrupt	unused		
FMC global interrupt	unused		
SPI3 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		
SPI5 global interrupt	unused		
SPI6 global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
I2C2 event interrupt	false	true	true
I2C2 error interrupt	false	true	true
USART1 global interrupt	false	true	true
USART3 global interrupt	false	true	true
TIM8 break interrupt and TIM12 global interrupt	false	true	true
TIM7 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream1 global interrupt	false	true	true
Ethernet global interrupt	false	true	true
I2C3 event interrupt	false	true	true
I2C3 error interrupt	false	true	true
SAI1 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware						
<div><div>FREERTOS </div><div>LWIP </div></div>						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA	ADC1	TIM7	CAN1	SAI1		
GPIO	DAC		ETH			
NVIC			FMC			
RCC			I2C2			
SYS			I2C3			
			SPI2			
			SPI3			
			SPI5			
			SPI6			
			USART1			
			USART3			

10. Docs & Resources

Type	Link
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Training Material	https://www.st.com/resource/en/sales_guide/sg_sc2154.pdf
Flyers	https://www.st.com/resource/en/flyer/flnucleolrwan.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstmcsuite.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32gui.pdf
Product Certifications	https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
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Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
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for related Tools [direct-drive-using-the-stm32f10xx-fsmc-peripheral-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an3241-qvga-tftlcd-for-related-Tools-direct-drive-using-the-stm32f10xx-fsmc-peripheral-stmicroelectronics.pdf)

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