CENG3420

Lab 3-3: LC-3b Datapath

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香港中文大學 The Chinese University of Hong Kong

Introduction

Lab3-3 Assignment





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The Slides are self-contained? NO!

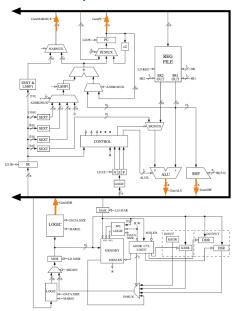
Do please refer to following document:

- ► LC-3b-datapath.pdf
- ► LC-3b-ISA.pdf





LC-3b Datapath

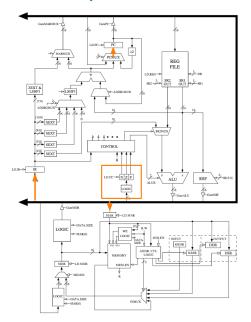


In lab 3-2, we write data into bus.





LC-3b Datapath



In this lab, we read data from bus:

- NEXT_LATCHES.PC
- NEXT_LATCHES.IR
- NEXT_LATCHES.MAR
- NEXT_LATCHES.N
- NEXT_LATCHES.Z
- ► NEXT_LATCHES.P





Introduction

Lab3-3 Assignment





Lab3-3 Assignment 1

- Paste your previous codes into eval_bus_drivers() & drive_bus().
- Finish the following function.

```
77 void latch_datapath_values()
                     if (GetLD_MDR(CURRENT_LATCHES.MICROINSTRUCTION))
                                   if (GetMIO_EN(CURRENT_LATCHES.MICROINSTRUCTION))
                                               NEXT LATCHES.MDR = MemOut/*Low16bits(CMEMORYFCURRENT LATCHES.MAR >> 1]F1] << 8) + MEMORYFCURRENT LATCHES.MAR >> 1]F0])*/:
                                                NEXT_LATCHES.MDR = blockMDRLogic2(partVal(CURRENT_LATCHES.MAR, 0, 0), GetDATA_SIZE(CURRENT_LATCHES.MICROINSTRUCTION), BUS);
                     if (GetLD_BEN(CURRENT_LATCHES.MICROINSTRUCTION))
                                  NEXT_LATCHES, BEN = (pgrtVal(CURRENT_LATCHES, IR, 11, 11) & CURRENT_LATCHES, IR, 10, 10) & CURRENT_LATCHES, IR, 10, 10) & CURRENT_LATCHES, IR, 11, 11) & CURRENT_LATCHES, IR, 11, 11) & CURRENT_LATCHES, IR, 12, 10) & CURRENT_LATCHES, IR, 13, 14) & CURRENT_LATCHES, IR, 14, 15) & CURRENT_LATCHES, IR, 15, 16) & CURRENT_LATCHES, IR, 16, 16) & CURRENT_LATCHES, IR, 17, 16) & CURRENT_LATCHES, IR, 18, 10) & CURRENT_LATCHES, IR, 11, 11) & CURRENT_LATCHES, IR, 12, 10) & CURRENT_LATCHES, IR, 13, 14) & CURRENT_LATCHES, IR, 14, 15) & CURRENT_LATCHES, IR, 15, 16) & CURRENT_LATCHES, IR, 16, 16) & CURRENT_LATCHES, IR, 16, 16) & CURRENT_LATCHES, IR, 17, 16) & CURRENT_LATCHES, IR, 18, 18, 18) & CURRENT_LATCHES, IR, 18) & CURRENT_LATCHES, IR, 18) & CURREN
                     if (GetLD REG(CURRENT LATCHES.MICROINSTRUCTION))
                                  NEXT_LATCHES.REGS[blockDRMUX(GetDRMUX(CURRENT_LATCHES.MICROINSTRUCTION), partVal(CURRENT_LATCHES.IR, 11, 9), 7)] = BUS;
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 4 D > 4 A > 4 B > 4 B > -
```

Lab3-3 Assignment 2: blockPCMUX

```
int blockPCMUX(int lPCMUX, int lPCAdd2, int lBUS, int
lAdder)
```

Special treatment again! The PCMUX selection criteria is different based on your SID

Orig

lPCMUX = 0: lPCAdd2 or1: lBUS; 2: lAdder;

SID with even ending:

lPCMUX = 0: lBUS; 1: lPCAdd2; 2: lAdder;

SID with odd ending:

lPCMUX = 0: lAdder; 1: lBUS; 2: lPCAdd2;



Introduction

Lab3-3 Assignment





Assignment Package

- ▶ lc3bsim3-3.c, lc3bsim3.h: codes to work on
- ▶ libems3-3-(darwin/linux).a: library
- ▶ ucode3: FSM
- Makefile
- bench: folder with benchmarks

Run the simulator:

- 1. make, then binary "lc3bsim3-3" is generated
- 2. For even ending SID: ./lc3bsim3-3 ucode3-even bench/toupper.cod
- 3. For odd ending SID: ./lc3bsim3-3 ucode3-odd bench/toupper.cod





Golden Results - case toupper.cod

► Please refer to Lab 3-1 slides.





Golden Results - case count 10. cod

► Please refer to Lab 3-2 slides.





Thanks. For any question:

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