ESP32-S3-MINI-1
ESP32-S3-MINI-1U

Datasheet Version 1.4

Small-sized module supporting 2.4 GHz Wi-Fi (802.11b/g/n) and Bluetooth® 5
Built around ESP32-S3 series of SoCs, Xtensa® dual-core 32-bit LX7 microprocessor
Flash up to 8 MB, optional 2 MB PSRAM in chip package
39 GPIOs, rich set of peripherals
On-board PCB antenna or external antenna connector

ESP32-S3-MINI-1

ESP32-S3-MINI-1U

ESPRESSIF

1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://www.espressif.com/documentation/esp32-s3-mini-1_mini-1u_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32-S3 embedded, Xtensa® dual-core 32-bit LX7 microprocessor (with single precision FPU), up to 240 MHz
- 384 KB ROM
- 512 KB SRAM
- 16 KB SRAM in RTC
- Up to 8 MB Quad SPI flash
- 2 MB PSRAM (ESP32-S3FH4R2 only)

Wi-Fi

- 802.11b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Bluetooth

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

Peripherals

- 39 GPIOs
  - 4 strapping GPIOs
- SPI, LCD interface, Camera interface, UART, I2C, I2S, remote control, pulse counter, LED PWM, full-speed USB 2.0 OTG, USB Serial/JTAG controller, MCPWM, SD/MMC host controller, GDMA, TWAI® controller (compatible with ISO 11898-1, i.e. CAN Specification 2.0), ADC, touch sensor, temperature sensor, timers and watchdogs

Integrated Components on Module

- 40 MHz crystal oscillator

Antenna Options

- ESP32-S3-MINI-1: On-board PCB antenna
- ESP32-S3-MINI-1U: External antenna via a connector

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature: −40 ~ 85 °C

Certification

- RF certification: See certificates
- Green certification: RoHS/REACH

Test

- HTOL/HTSL/uHAST/TCT/ESD

1.2 Series Comparison

ESP32-S3-MINI-1 and ESP32-S3-MINI-1U are two powerful, generic Wi-Fi + Bluetooth LE MCU modules that feature a rich set of peripherals, yet an optimized size. They are an ideal choice for a wide variety of application scenarios related to Internet of Things (IoT), such as embedded systems, smart home, wearable electronics, etc.

ESP32-S3-MINI-1 comes with a PCB antenna. ESP32-S3-MINI-1U comes with a connector for an external antenna. They feature an up to 8 MB SPI flash and an optional 2 MB SPI Pseudo static RAM (PSRAM). Both ESP32-S3-MINI-1 and ESP32-S3-MINI-1U come in two versions, with the ordering code ending with -N8 and -N4R2 respectively. The two versions only vary in flash and PSRAM size.

The series comparison for the two modules is as follows:

Table 1: ESP32-S3-MINI-1 and ESP32-S3-MINI-1U Series Comparison

Ordering Code	Flash[1, 2]	PSRAM[1]	Ambient Temp.[3] (°C)	Size[4] (mm)
ESP32-S3-MINI-1-N8	8 MB (Quad SPI)	-	−40 ~ 85	15.4 × 20.5 × 2.4
ESP32-S3-MINI-1-N4R2	4 MB (Quad SPI)	2 MB (Quad SPI)		
ESP32-S3-MINI-1U-N8	8 MB (Quad SPI)	-		15.4 × 15.4 × 2.4
ESP32-S3-MINI-1U-N4R2	4 MB (Quad SPI)	2 MB (Quad SPI)		

[1] The modules use flash and PSRAM integrated in the chip's package. The integrated flash supports:
- More than 100,000 program/erase cycles
- More than 20 years data retention time

[2] By default, the SPI flash on the module operates at a maximum clock frequency of 80 MHz and does not support the auto suspend feature. If you have a requirement for a higher flash clock frequency of 120 MHz or if you need the flash auto suspend feature, please contact us.

[3] Ambient temperature specifies the recommended temperature range of the environment immediately outside the Espressif module.

[4] For details, refer to Section 10.1 *Module Dimensions*.

At the core of the modules is an ESP32-S3 series of SoC, an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. You can power off the CPU and make use of the low-power co-processor to constantly monitor the peripherals for changes or crossing of thresholds.

Note:
For more information on ESP32-S3, please refer to *ESP32-S3 Series Datasheet*.
For chip revision identification, ESP-IDF release that supports a specific chip revision, and other information on chip revisions, please refer to *ESP32-S3 Series SoC Errata* > Section *Chip Revision Identification*.

1.3 Applications

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines

- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- USB Devices
- Speech Recognition
- Image Recognition
- Wi-Fi + Bluetooth Networking Card
- Touch and Proximity Sensing

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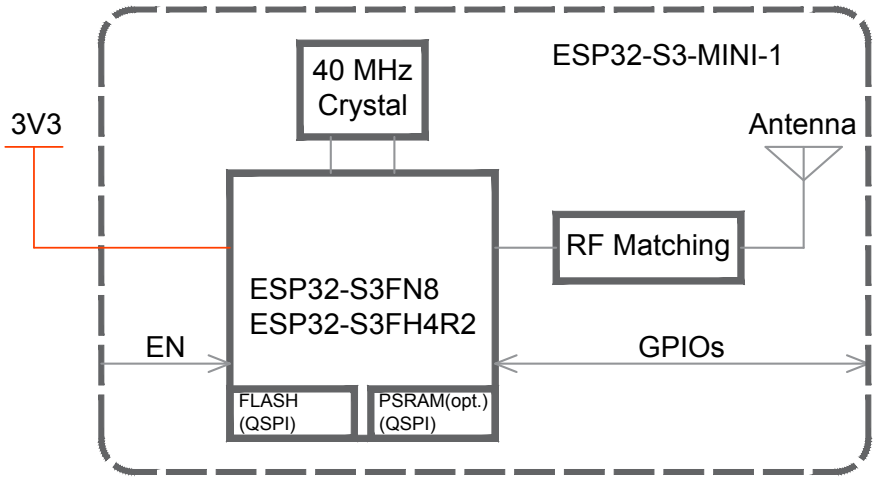

Figure 1: ESP32-S3-MINI-1 Block Diagram

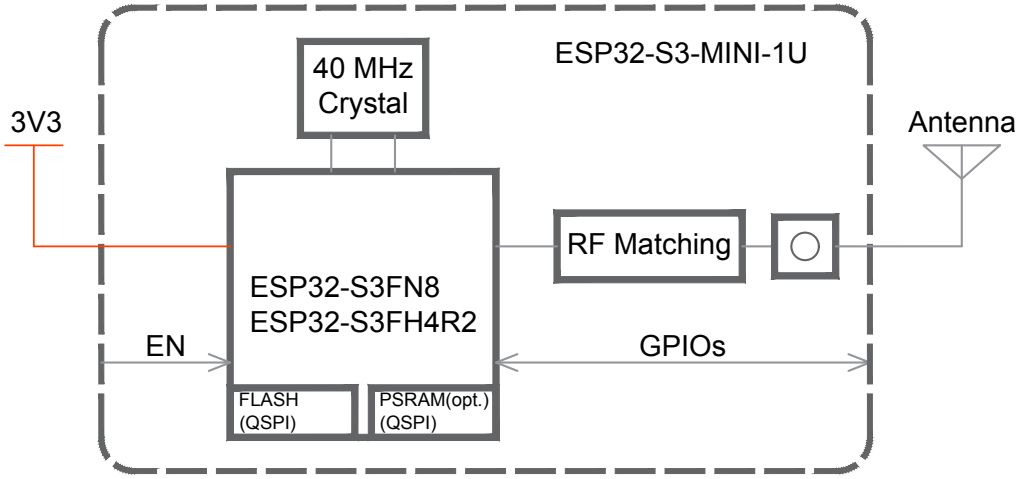

Figure 2: ESP32-S3-MINI-1U Block Diagram

Note:

For the pin mapping between the chip and the in-package flash and PSRAM, please refer to *ESP32-S3 Series Datasheet* > Table *Pin Mapping Between Chip and In-package Flash/PSRAM*.

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 10.1 *Module Dimensions*.

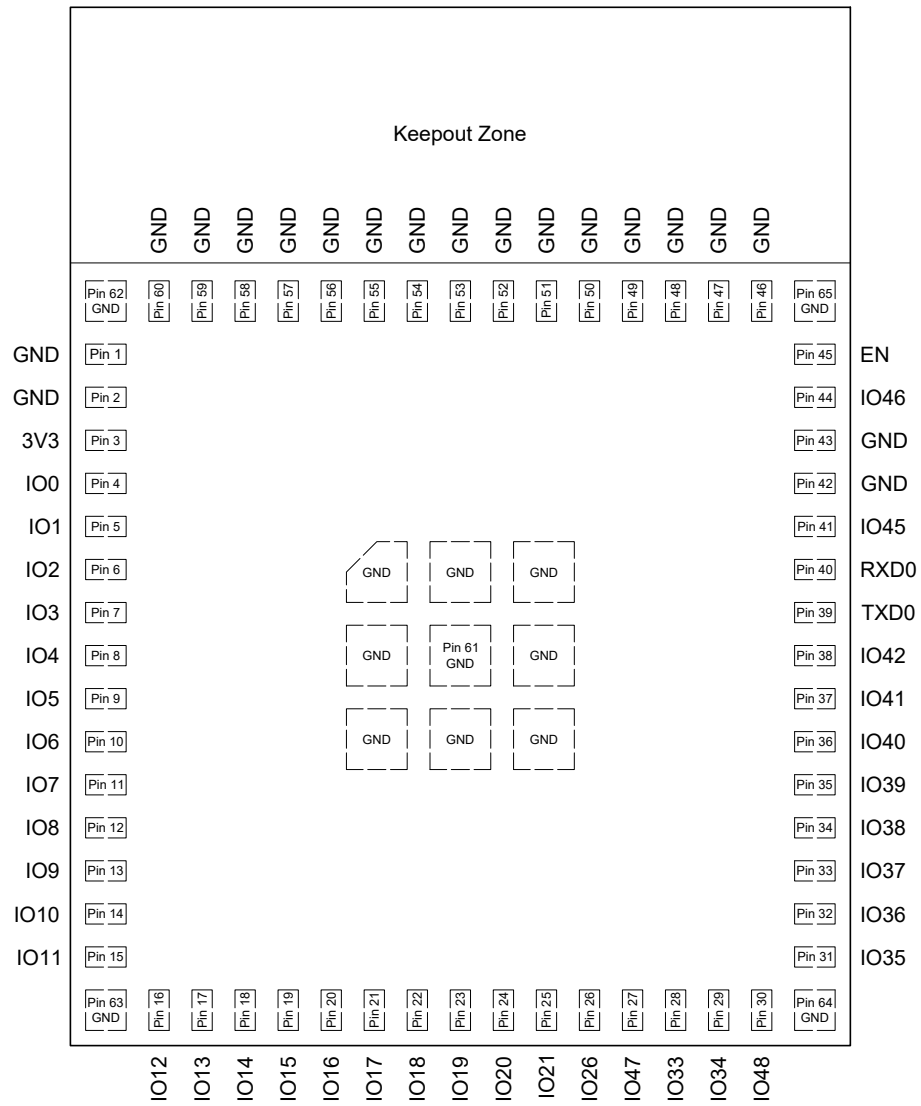

Figure 3: Pin Layout (Top View)

Note A:
The pin diagram is applicable to ESP32-S3-MINI-1 and ESP32-S3-MINI-1U, but the latter has no antenna keepout zone. To learn more about the keepout zone for module's antenna on the base board, please refer to *ESP32-S3 Hardware Design Guidelines* > Section *Positioning a Module on a Base Board*.

3.2 Pin Description

The module has 65 pins. See pin definitions in Table 2 *Pin Definitions*.

For explanations of pin names and function names, as well as configurations of peripheral pins, please refer to *ESP32-S3 Series Datasheet*.

Table 2: Pin Definitions

Name	No.	Type [a]	Function
GND	1, 2, 42, 43, 46-65	P	GND
3V3	3	P	Power supply
IO0	4	I/O/T	RTC_GPIO0, **GPIO0**
IO1	5	I/O/T	RTC_GPIO1, **GPIO1**, TOUCH1, ADC1_CH0
IO2	6	I/O/T	RTC_GPIO2, **GPIO2**, TOUCH2, ADC1_CH1
IO3	7	I/O/T	RTC_GPIO3, **GPIO3**, TOUCH3, ADC1_CH2
IO4	8	I/O/T	RTC_GPIO4, **GPIO4**, TOUCH4, ADC1_CH3
IO5	9	I/O/T	RTC_GPIO5, **GPIO5**, TOUCH5, ADC1_CH4
IO6	10	I/O/T	RTC_GPIO6, **GPIO6**, TOUCH6, ADC1_CH5
IO7	11	I/O/T	RTC_GPIO7, **GPIO7**, TOUCH7, ADC1_CH6
IO8	12	I/O/T	RTC_GPIO8, **GPIO8**, TOUCH8, ADC1_CH7, SUBSPICS1
IO9	13	I/O/T	RTC_GPIO9, **GPIO9**, TOUCH9, ADC1_CH8, FSPIHD, SUBSPIHD
IO10	14	I/O/T	RTC_GPIO10, **GPIO10**, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4, SUBSPICS0
IO11	15	I/O/T	RTC_GPIO11, **GPIO11**, TOUCH11, ADC2_CH0, FSPID, FSPIIO5, SUBSPID
IO12	16	I/O/T	RTC_GPIO12, **GPIO12**, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6, SUBSPICLK
IO13	17	I/O/T	RTC_GPIO13, **GPIO13**, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7, SUBSPIQ
IO14	18	I/O/T	RTC_GPIO14, **GPIO14**, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS, SUBSPIWP
IO15	19	I/O/T	RTC_GPIO15, **GPIO15**, U0RTS, ADC2_CH4, XTAL_32K_P
IO16	20	I/O/T	RTC_GPIO16, **GPIO16**, U0CTS, ADC2_CH5, XTAL_32K_N
IO17	21	I/O/T	RTC_GPIO17, **GPIO17**, U1TXD, ADC2_CH6
IO18	22	I/O/T	RTC_GPIO18, **GPIO18**, U1RXD, ADC2_CH7, CLK_OUT3
IO19	23	I/O/T	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, **USB_D-**
IO20	24	I/O/T	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, **USB_D+**
IO21	25	I/O/T	RTC_GPIO21, **GPIO21**
IO26[b]	26	I/O/T	SPICS1, **GPIO26**
IO47	27	I/O/T	SPICLK_P_DIFF, **GPIO47**, SUBSPICLK_P_DIFF
IO33	28	I/O/T	SPIIO4, **GPIO33**, FSPIHD, SUBSPIHD
IO34	29	I/O/T	SPIIO5, **GPIO34**, FSPICS0, SUBSPICS0
IO48	30	I/O/T	SPICLK_N_DIFF, **GPIO48**, SUBSPICLK_N_DIFF
IO35	31	I/O/T	SPIIO6, **GPIO35**, FSPID, SUBSPID
IO36	32	I/O/T	SPIIO7, **GPIO36**, FSPICLK, SUBSPICLK
IO37	33	I/O/T	SPIDQS, **GPIO37**, FSPIQ, SUBSPIQ
IO38	34	I/O/T	**GPIO38**, FSPIWP, SUBSPIWP
IO39	35	I/O/T	**MTCK**, GPIO39, CLK_OUT3, SUBSPICS1
IO40	36	I/O/T	**MTDO**, GPIO40, CLK_OUT2
IO41	37	I/O/T	**MTDI**, GPIO41, CLK_OUT1

Cont'd on next page

Table 2 – cont'd from previous page

Name	No.	Type [a]	Function
IO42	38	I/O/T	**MTMS**, GPIO42
TXD0	39	I/O/T	**U0TXD**, GPIO43, CLK_OUT1
RXD0	40	I/O/T	**U0RXD**, GPIO44, CLK_OUT2
IO45	41	I/O/T	**GPIO45**
IO46	44	I/O/T	**GPIO46**
EN	45	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.

[a] P: power supply; I: input; O: output; T: high impedance. Pin functions in bold font are the default pin functions. For pin 28 ∼ 29, 31 ∼ 33, the default function is decided by eFuse bit.

[b] For modules with ordering codes ending with -N4R2, IO26 connects to the embedded PSRAM and is not available for other uses.

4 Boot Configurations

Note:
The content below is excerpted from *ESP32-S3 Series Datasheet* > Section *Boot Configurations*. For the strapping pin mapping between the chip and modules, please refer to Chapter 8 *Module Schematics*.

The chip allows for configuring the following boot parameters through strapping pins and eFuse bits at power-up or a hardware reset, without microcontroller interaction.

- **Chip boot mode**
  - Strapping pin: GPIO0 and GPIO46
- **VDD_SPI voltage**
  - Strapping pin: GPIO45
  - eFuse parameter: EFUSE_VDD_SPI_FORCE and EFUSE_VDD_SPI_TIEH
- **ROM message printing**
  - Strapping pin: GPIO46
  - eFuse parameter: EFUSE_UART_PRINT_CONTROL and EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
- **JTAG signal source**
  - Strapping pin: GPIO3
  - eFuse parameter: EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_STRAP_JTAG_SEL

The default values of all the above eFuse parameters are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once programmed to 1, it can never be reverted to 0. For how to program eFuse parameters, please refer to *ESP32-S3 Technical Reference Manual* > Chapter *eFuse Controller*.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 3: Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Weak pull-up	1
GPIO3	Floating	–
GPIO45	Weak pull-down	0
GPIO46	Weak pull-down	0

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-S3 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in

any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 4 and Figure 4.

Table 4: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

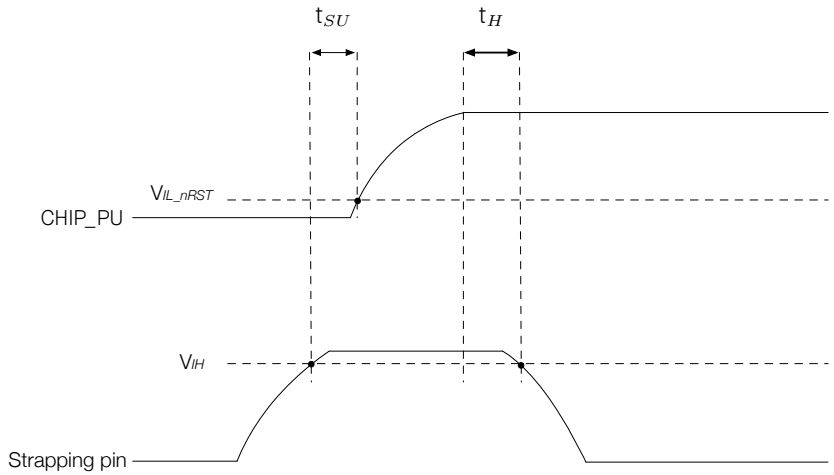

Figure 4: Visualization of Timing Parameters for the Strapping Pins

4.1 Chip Boot Mode Control

GPIO0 and GPIO46 control the boot mode after the reset is released. See Table 5 *Chip Boot Mode Control*.

Table 5: Chip Boot Mode Control

Boot Mode	GPIO0	GPIO46
SPI Boot	**1**	Any value
Joint Download Boot [2]	0	0

[1] **Bold** marks the default value and configuration.

[2] Joint Download Boot mode supports the following download methods:

- USB Download Boot:
  - USB-Serial-JTAG Download Boot
  - USB-OTG Download Boot
- UART Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system.

In Joint Download Boot mode, users can download binary files into flash using UART0 or USB interface. It is also possible to download binary files into SRAM and execute it from SRAM.

In addition to SPI Boot and Joint Download Boot modes, ESP32-S3 also supports SPI Download Boot mode. For details, please see *ESP32-S3 Technical Reference Manual* > Chapter *Chip Boot Control*.

4.2 VDD_SPI Voltage Control

Depending on the value of EFUSE_VDD_SPI_FORCE, the voltage can be controlled in two ways.

Table 6: VDD_SPI Voltage Control

VDD_SPI power source [2]	Voltage	EFUSE_VDD_SPI_FORCE	GPIO45	EFUSE_VDD_SPI_TIEH
VDD3P3_RTC via R_{SPI}	**3.3 V**	**0**	**0**	Ignored
Flash Voltage Regulator	1.8 V		1	
Flash Voltage Regulator	1.8 V	1	Ignored	0
VDD3P3_RTC via R_{SPI}	3.3 V			1

[1] **Bold** marks the default value and configuration.

[2] See *ESP32-S3 Series Datasheet* > Section *Power Scheme*.

4.3 ROM Messages Printing Control

During boot process the messages by the ROM code can be printed to:

- **(Default) UART0 and USB Serial/JTAG controller**
- USB Serial/JTAG controller
- UART0

The ROM messages printing to UART or USB Serial/JTAG controller can be respectively disabled by configuring registers and eFuse. For detailed information, please refer to *ESP32-S3 Technical Reference Manual* > Chapter *Chip Boot Control*.

4.4 JTAG Signal Source Control

The strapping pin GPIO3 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

As Table 7 shows, GPIO3 is used in combination with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_STRAP_JTAG_SEL.

Table 7: JTAG Signal Source Control

JTAG Signal Source	EFUSE_DIS_PAD_JTAG	EFUSE_DIS_USB_JTAG	EFUSE_STRAP_JTAG_SEL	GPIO3
USB Serial/JTAG Controller	**0**	**0**	**0**	Ignored
	0	0	1	1
	1	0	Ignored	Ignored
JTAG pins [2]	0	0	1	0
	0	1	Ignored	Ignored
JTAG is disabled	1	1	Ignored	Ignored

[1] **Bold** marks the default value and configuration.

[2] JTAG pins refer to MTDI, MTCK, MTMS, and MTDO.

5 Peripherals

5.1 Peripheral Overview

ESP32-S3 integrates a rich set of peripherals including SPI, LCD, Camera interface, UART, I2C, I2S, remote control, pulse counter, LED PWM, USB Serial/JTAG, MCPWM, SD/MMC host controller, TWAI® controller (compatible with ISO 11898-1, i.e., CAN Specification 2.0), ADC, touch sensor, and temperature sensor. It also includes a full-speed USB 2.0 On-The-Go (OTG) interface to enable USB communication.

To learn more about on-chip components, please refer to *ESP32-S3 Series Datasheet* > Section *Functional Description*.

Note:
The content below is sourced from *ESP32-S3 Series Datasheet* > Section *Peripherals*. Some information may not be applicable to ESP32-S3-MINI-1 and ESP32-S3-MINI-1U as not all the IO signals are exposed on the module.
To learn more about peripheral signals, please refer to *ESP32-S3 Technical Reference Manual* > Section *Peripheral Signals via GPIO Matrix*.

5.2 Peripheral Description

This section describes the chip's peripheral capabilities, covering connectivity interfaces and on-chip sensors that extend its functionality.

5.2.1 Connectivity Interface

This subsection describes the connectivity interfaces on the chip that enable communication and interaction with external devices and networks.

5.2.1.1 UART Controller

ESP32-S3 has three UART (Universal Asynchronous Receiver Transmitter) controllers, i.e., UART0, UART1, and UART2, which support IrDA and asynchronous communication (RS232 and RS485) at a speed of up to 5 Mbps.

Feature List

- Three clock sources that can be divided
- Programmable baud rate
- 1024 x 8-bit RAM shared by TX FIFOs and RX FIFOs of the three UART controllers
- Full-duplex asynchronous communication
- Automatic baud rate detection of input signals
- Data bits ranging from 5 to 8
- Stop bits of 1, 1.5, 2, or 3 bits
- Parity bit

- Special character AT_CMD detection
- RS485 protocol
- IrDA protocol
- High-speed data communication using GDMA
- UART as wake-up source
- Software and hardware flow control

Pin Assignment

- UART0
  - The pins U0TXD and U0RXD that are connected to transmit and receive signals are multiplexed with GPIO43 ~ GPIO44 via IO MUX, and can also be connected to any GPIO via the GPIO Matrix.
  - The pins U0RTS and U0CTS that are connected to hardware flow control signals are multiplexed with GPIO15 ~ GPIO16, RTC_GPIO15 ~ RTC_GPIO16, XTAL_32K_P and XTAL_32K_N, and SAR ADC2 interface via IO MUX, and can also be connected to any GPIO via the GPIO Matrix.
  - The pins U0DTR and U0DSR that are connected to hardware flow control signals can be chosen from any GPIO via the GPIO Matrix.
- UART1
  - The pins U1TXD and U1RXD that are connected to transmit and receive signals are multiplexed with GPIO17 ~ GPIO18, RTC_GPIO17 ~ RTC_GPIO18, and SAR ADC2 interface via IO MUX, and can also be connected to any GPIO via the GPIO Matrix.
  - The pins U1RTS and U1CTS that are connected to hardware flow control signals are multiplexed with GPIO19 ~ GPIO20, RTC_GPIO19 ~ RTC_GPIO20, USB_D- and USB_D+ pins, and SAR ADC2 interface via IO MUX, and can also be connected to any GPIO via the GPIO Matrix.
  - The pins U1DTR and U1DSR that are connected to hardware flow control signals can be chosen from any GPIO via the GPIO Matrix.
- UART2: The pins used can be chosen from any GPIO via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.2 I2C Interface

ESP32-S3 has two I2C bus interfaces which are used for I2C master mode or slave mode, depending on the user's configuration.

Feature List

- Standard mode (100 kbit/s)
- Fast mode (400 kbit/s)
- Up to 800 kbit/s (constrained by SCL and SDA pull-up strength)
- 7-bit and 10-bit addressing mode

- Double addressing mode (slave addressing and slave register addressing)

The hardware provides a command abstraction layer to simplify the usage of the I2C peripheral.

Pin Assignment

For I2C, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.3 I2S Interface

ESP32-S3 includes two standard I2S interfaces. They can operate in master mode or slave mode, in full-duplex mode or half-duplex communication mode, and can be configured to operate with an 8-bit, 16-bit, 24-bit, or 32-bit resolution as an input or output channel. BCK clock frequency, from 10 kHz up to 40 MHz, is supported.

The I2S interface has a dedicated DMA controller. It supports TDM PCM, TDM MSB alignment, TDM LSB alignment, TDM Phillips, and PDM interface.

Pin Assignment

For I2S, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.4 LCD and Camera Controller

The LCD and Camera controller of ESP32-S3 consists of a LCD module and a camera module.

The LCD module is designed to send parallel video data signals, and its bus supports 8-bit ~ 16-bit parallel RGB, I8080, and MOTO6800 interfaces. These interfaces operate at 40 MHz or lower, and support conversion among RGB565, YUV422, YUV420, and YUV411.

The camera module is designed to receive parallel video data signals, and its bus supports an 8-bit ~ 16-bit DVP image sensor, with clock frequency of up to 40 MHz. The camera interface supports conversion among RGB565, YUV422, YUV420, and YUV411.

Pin Assignment

For LCD and Camera controller, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.5 Serial Peripheral Interface (SPI)

ESP32-S3 has the following SPI interfaces:

- **SPI0** used by ESP32-S3's GDMA controller and cache to access in-package or off-package flash/PSRAM
- **SPI1** used by the CPU to access in-package or off-package flash/PSRAM

- **SPI2** is a general purpose SPI controller with access to a DMA channel allocated by the GDMA controller
- **SPI3** is a general purpose SPI controller with access to a DMA channel allocated by the GDMA controller

Feature List

- SPI0 and SPI1:
  - Supports Single SPI, Dual SPI, Quad SPI, Octal SPI, QPI, and OPI modes
  - 8-line SPI mode supports single data rate (SDR) and double data rate (DDR)
  - Configurable clock frequency with a maximum of 120 MHz for 8-line SPI SDR/DDR modes
  - Data transmission is in bytes
- SPI2:
  - Supports operation as a master or slave
  - Connects to a DMA channel allocated by the GDMA controller
  - Supports Single SPI, Dual SPI, Quad SPI, Octal SPI, QPI, and OPI modes
  - Configurable clock polarity (CPOL) and phase (CPHA)
  - Configurable clock frequency
  - Data transmission is in bytes
  - Configurable read and write data bit order: most-significant bit (MSB) first, or least-significant bit (LSB) first
  - As a master
    * Supports 2-line full-duplex communication with clock frequency up to 80 MHz
    * Full-duplex 8-line SPI mode supports single data rate (SDR) only
    * Supports 1-, 2-, 4-, 8-line half-duplex communication with clock frequency up to 80 MHz
    * Half-duplex 8-line SPI mode supports both single data rate (up to 80 MHz) and double data rate (up to 40 MHz)
    * Provides six SPI_CS pins for connection with six independent SPI slaves
    * Configurable CS setup time and hold time
  - As a slave
    * Supports 2-line full-duplex communication with clock frequency up to 60 MHz
    * Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 60 MHz
    * Full-duplex and half-duplex 8-line SPI mode supports single data rate (SDR) only
- SPI3:
  - Supports operation as a master or slave
  - Connects to a DMA channel allocated by the GDMA controller
  - Supports Single SPI, Dual SPI, Quad SPI, and QPI modes

  - Configurable clock polarity (CPOL) and phase (CPHA)
  - Configurable clock frequency
  - Data transmission is in bytes
  - Configurable read and write data bit order: most-significant bit (MSB) first, or least-significant bit (LSB) first
  - As a master
    * Supports 2-line full-duplex communication with clock frequency up to 80 MHz
    * Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 80 MHz
    * Provides three SPI_CS pins for connection with three independent SPI slaves
    * Configurable CS setup time and hold time
  - As a slave
    * Supports 2-line full-duplex communication with clock frequency up to 60 MHz
    * Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 60 MHz

Pin Assignment

Note:
Please refer to *ESP32-S3 Series Datasheet* > Section *IO MUX Function* > Table *IO MUX Pin Functions* for the corresponding SPI interface details.

- SPI0/1
  - Via IO MUX:
    * Interface *4a* is multiplexed with GPIO26 ~ GPIO32 via IO MUX. When used in conjunction with *4b*, it can operate as the lower 4 bits data line interface and the CLK, CS0, and CS1 interfaces in 8-line SPI mode.
    * Interface *4b* is multiplexed with GPIO33 ~ GPIO37 and SPI interfaces *4e* and *4f* via IO MUX. When used in conjunction with *4a*, it can operate as the higher 4 bits data line interface and DQS interface in 8-line SPI mode.
    * Interface *4d* is multiplexed with GPIO8 ~ GPIO14, RTC_GPIO8 ~ RTC_GPIO14, Touch Sensor interface, SAR ADC interface, and SPI interfaces *4c* and *4g* via IO MUX. Note that the fast SPI2 interface will not be available.
    * Interface *4e* is multiplexed with GPIO33 ~ GPIO39, JTAG MTCK interface, and SPI interfaces *4b* and *4f* via IO MUX. It is an alternative group of signal lines that can be used if SPI0/1 does not use 8-line SPI connection.
  - Via GPIO Matrix: The pins used can be chosen from any GPIOs via the GPIO Matrix.
- SPI2
  - Via IO MUX:
    * Interface *4c* is multiplexed with GPIO9 ~ GPIO14, RTC_GPIO9 ~ RTC_GPIO14, Touch Sensor interface, SAR ADC interface, and SPI interfaces *4d* and *4g* via IO MUX. It is the SPI2 main interface for fast SPI connection.

        * (not recommended) Interface *4f* is multiplexed with GPIO33 ~ GPIO38, SPI interfaces *4e* and *4b* via IO MUX. It is the alternative SPI2 interface if the main SPI2 is not available. Its performance is comparable to SPI2 via GPIO matrix, so use the GPIO matrix instead.
        * (not recommended) Interface *4g* is multiplexed with GPIO10 ~ GPIO14, RTC_GPIO10 ~ RTC_GPIO14, Touch Sensor interface, SAR ADC interface, and SPI interfaces *4c* and *4d* via IO MUX. It is the alternative SPI2 interface signal lines for 8-line SPI connection.
    - Via GPIO Matrix: The pins used can be chosen from any GPIOs via the GPIO Matrix.
- SPI3: The pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.6 Two-Wire Automotive Interface (TWAI®)

The Two-Wire Automotive Interface (TWAI®) is a multi-master, multi-cast communication protocol with error detection and signaling as well as inbuilt message priorities and arbitration.

Feature List

- Compatible with ISO 11898-1 protocol (CAN Specification 2.0)
- Standard frame format (11-bit ID) and extended frame format (29-bit ID)
- Bit rates from 1 Kbit/s to 1 Mbit/s
- Multiple modes of operation:
    - Normal
    - Listen Only
    - Self-Test (no acknowledgment required)
- 64-byte receive FIFO
- Acceptance filter (single and dual filter modes)
- Error detection and handling:
    - Error counters
    - Configurable error interrupt threshold
    - Error code capture
    - Arbitration lost capture

Pin Assignment

For TWAI, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.7 USB 2.0 OTG Full-Speed Interface

ESP32-S3 features a full-speed USB OTG interface along with an integrated transceiver. The USB OTG interface complies with the USB 2.0 specification.

General Features

- FS and LS data rates
- HNP and SRP as A-device or B-device
- Dynamic FIFO (DFIFO) sizing
- Multiple modes of memory access
  - Scatter/Gather DMA mode
  - Buffer DMA mode
  - Slave mode
- Can choose integrated transceiver or external transceiver
- Utilizing integrated transceiver with USB Serial/JTAG by time-division multiplexing when only integrated transceiver is used
- Support USB OTG using one of the transceivers while USB Serial/JTAG using the other one when both integrated transceiver or external transceiver are used

Device Mode Features

- Endpoint number 0 always present (bi-directional, consisting of EP0 IN and EP0 OUT)
- Six additional endpoints (endpoint numbers 1 to 6), configurable as IN or OUT
- Maximum of five IN endpoints concurrently active at any time (including EP0 IN)
- All OUT endpoints share a single RX FIFO
- Each IN endpoint has a dedicated TX FIFO

Host Mode Features

- Eight channels (pipes)
  - A control pipe consists of two channels (IN and OUT), as IN and OUT transactions must be handled separately. Only Control transfer type is supported.
  - Each of the other seven channels is dynamically configurable to be IN or OUT, and supports Bulk, Isochronous, and Interrupt transfer types.
- All channels share an RX FIFO, non-periodic TX FIFO, and periodic TX FIFO. The size of each FIFO is configurable.

Pin Assignment

When using the on-chip PHY, the differential signal pins USB_D- and USB_D+ of the USB OTG are multiplexed with GPIO19 ~ GPIO20, RTC_GPIO19 ~ RTC_GPIO20, UART1 interface, and SAR ADC2 interface via IO MUX.

When using external PHY, the USB OTG pins are multiplexed with GPIO21, RTC_GPIO21, GPIO38 ~ GPIO42, and SPI interface via IO MUX:

- VP signal connected to MTMS pin
- VM signal connected to MTDI pin
- RCV signal connected to GPIO21
- OEN signal connected to MTDO pin
- VPO signal connected to MTCK pin
- VMO signal connected to GPIO38

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.8 USB Serial/JTAG Controller

ESP32-S3 integrates a USB Serial/JTAG controller.

Feature List

- USB Full-speed device.
- Can be configured to either use internal USB PHY of ESP32-S3 or external PHY via GPIO matrix.
- Fixed function device, hardwired for CDC-ACM (Communication Device Class - Abstract Control Model) and JTAG adapter functionality.
- Two OUT Endpoints, three IN Endpoints in addition to Control Endpoint 0; Up to 64-byte data payload size.
- Internal PHY, so no or very few external components needed to connect to a host computer.
- CDC-ACM adherent serial port emulation is plug-and-play on most modern OSes.
- JTAG interface allows fast communication with CPU debug core using a compact representation of JTAG instructions.
- CDC-ACM supports host controllable chip reset and entry into download mode.

Pin Assignment

When using the on-chip PHY, the differential signal pins USB_D- and USB_D+ of the USB Serial/JTAG controller are multiplexed with GPIO19 ~ GPIO20, RTC_GPIO19 ~ RTC_GPIO20, UART1 interface, and SAR ADC2 interface via IO MUX.

When using external PHY, the USB Serial/JTAG controller pins are multiplexed with GPIO38 ~ GPIO42 and SPI interface via IO MUX:

- VP signal connected to MTMS pin
- VM signal connected to MTDI pin
- OEN signal connected to MTDO pin
- VPO signal connected to MTCK pin
- VMO signal connected to GPIO38

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.9 SD/MMC Host Controller

ESP32-S3 has an SD/MMC Host controller.

Feature List

- Secure Digital (SD) memory version 3.0 and version 3.01
- Secure Digital I/O (SDIO) version 3.0
- Consumer Electronics Advanced Transport Architecture (CE-ATA) version 1.1
- Multimedia Cards (MMC version 4.41, eMMC version 4.5 and version 4.51)
- Up to 80 MHz clock output
- Three data bus modes:
  - 1-bit
  - 4-bit (supports two SD/SDIO/MMC 4.41 cards, and one SD card operating at 1.8 V in 4-bit mode)
  - 8-bit

Pin Assignment

For SD/MMC Host, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.10 LED PWM Controller

The LED PWM controller can generate independent digital waveforms on eight channels.

Feature List

- Can generate a digital waveform with configurable periods and duty cycle. The duty cycle resolution can be up to 14 bits within a 1 ms period
- Multiple clock sources, including APB clock and external main crystal clock
- Can operate when the CPU is in Light-sleep mode
- Gradual increase or decrease of duty cycle, useful for the LED RGB color-fading generator

Pin Assignment

For LED PWM, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.11 Motor Control PWM (MCPWM)

ESP32-S3 integrates two MCPWMs that can be used to drive digital motors and smart light. Each MCPWM peripheral has one clock divider (prescaler), three PWM timers, three PWM operators, and a capture module. PWM timers are used for generating timing references. The PWM operators generate desired waveform based on the timing references. Any PWM operator can be configured to use the timing references of any PWM timers. Different PWM operators can use the same PWM timer's timing references to produce related PWM signals. PWM operators can also use different PWM timers' values to produce the PWM signals that work alone. Different PWM timers can also be synchronized together.

Pin Assignment

For MCPWM, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.12 Remote Control Peripheral (RMT)

The Remote Control Peripheral (RMT) is designed to send and receive infrared remote control signals.

Feature List

- Four TX channels
- Four RX channels
- Support multiple channels (programmable) transmitting data simultaneously
- Eight channels share a 384 x 32-bit RAM
- Support modulation on TX pulses
- Support filtering and demodulation on RX pulses
- Wrap TX mode
- Wrap RX mode
- Continuous TX mode
- DMA access for TX mode on channel 3
- DMA access for RX mode on channel 7

Pin Assignment

For RMT, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.13 Pulse Count Controller (PCNT)

The pulse count controller (PCNT) captures pulse and counts pulse edges through multiple modes.

Feature List

- Four independent pulse counters (units) that count from 1 to 65535
- Each unit consists of two independent channels sharing one pulse counter
- All channels have input pulse signals (e.g. sig_ch0_u*n*) with their corresponding control signals (e.g. ctrl_ch0_u*n*)
- Independently filter glitches of input pulse signals (sig_ch0_u*n* and sig_ch1_u*n*) and control signals (ctrl_ch0_u*n* and ctrl_ch1_u*n*) on each unit
- Each channel has the following parameters:
  1. Selection between counting on positive or negative edges of the input pulse signal
  2. Configuration to Increment, Decrement, or Disable counter mode for control signal's high and low states

Pin Assignment

For pulse count controller, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.2 Analog Signal Processing

This subsection describes components on the chip that sense and process real-world data.

5.2.2.1 SAR ADC

ESP32-S3 integrates two 12-bit SAR ADCs and supports measurements on 20 channels (analog-enabled pins). For power-saving purpose, the ULP coprocessors in ESP32-S3 can also be used to measure voltage in sleep modes. By using threshold settings or other methods, we can awaken the CPU from sleep modes.

Pin Assignment

The pins for the SAR ADC are multiplexed with GPIO1 ~ GPIO20, RTC_GPIO1 ~ RTC_GPIO20, Touch Sensor interface, SPI interface, UART interface, and USB_D- and USB_D+ pins via IO MUX.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.2.2 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature. The voltage is internally converted via an ADC into a digital value.

The temperature sensor has a range of −40 °C to 125 °C. It is designed primarily to sense the temperature changes inside the chip. The temperature value depends on factors such as microcontroller clock frequency or I/O load. Generally, the chip's internal temperature is higher than the ambient temperature.

5.2.2.3 Touch Sensor

ESP32-S3 has 14 capacitive-sensing GPIOs, which detect variations induced by touching or approaching the GPIOs with a finger or other objects. The low-noise nature of the design and the high sensitivity of the circuit allow relatively small pads to be used. Arrays of pads can also be used, so that a larger area or more points can be detected. The touch sensing performance can be further enhanced by the waterproof design and digital filtering feature.

Note:
ESP32-S3 touch sensor has not passed the Conducted Susceptibility (CS) test for now, and thus has limited application scenarios.

Pin Assignment

The pins for touch sensor are multiplexed with GPIO1 ~ GPIO14, RTC_GPIO1 ~ RTC_GPIO14, SAR ADC interface, and SPI interface via IO MUX.

For more information about the pin assignment, see *ESP32-S3 Series Datasheet* > Section *IO Pins* and *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses above those listed in Table 8 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 9 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	−0.3	3.6	V
T_{STORE}	Storage temperature	−40	105	°C

6.2 Recommended Operating Conditions

Table 9: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T_A	Operating ambient temperature	−40	—	85	°C

6.3 DC Characteristics (3.3 V, 25 °C)

Table 10: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL}	Low-level input voltage	−0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Internal weak pull-up resistor	—	45	—	kΩ
R_{PD}	Internal weak pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage (EN voltage is within the specified range)	0.75 × VDD[1]	—	VDD[1] + 0.3	V

Cont'd on next page

Table 10 – cont'd from previous page

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL_nRST}	Chip reset voltage (EN voltage is within the specified range)	−0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for pins of a particular power domain.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

6.4 Current Consumption Characteristics

6.4.1 Current Consumption in Active Mode

With the use of advanced power-management technologies, the module can switch between different power modes. For details on different power modes, please refer to Section *Power Management Unit* in *ESP32-S3 Series Datasheet*.

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 11: Current Consumption in Avtice Mode

Work mode	Description		Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, @20.5 dBm	355
		802.11g, 54 Mbps, @18 dBm	297
		802.11n, HT20, MCS 7, @17.5 dBm	286
		802.11n, HT40, MCS 7, @17 dBm	285
	RX	802.11b/g/n, HT20	95
		802.11n, HT40	97

Note:
The content below is excerpted from *Section Power Consumption in Other Modes* in *ESP32-S3 Series Datasheet*.

6.4.2 Current Consumption in Other Modes

Please note that if the chip embedded has in-package PSRAM, the current consumption of the module might be higher compared to the measurements below.

Table 12: Current Consumption in Modem-sleep Mode

Work mode	Frequency (MHz)	Description	Typ[1] (mA)	Typ[2] (mA)
Modem-sleep[3]	40	WAITI (Dual core in idle state)	13.2	18.8
		Single core running 32-bit data access instructions, the other core in idle state	16.2	21.8
		Dual core running 32-bit data access instructions	18.7	24.4
		Single core running 128-bit data access instructions, the other core in idle state	19.9	25.4
		Dual core running 128-bit data access instructions	23.0	28.8
	80	WAITI	22.0	36.1
		Single core running 32-bit data access instructions, the other core in idle state	28.4	42.6
		Dual core running 32-bit data access instructions	33.1	47.3
		Single core running 128-bit data access instructions, the other core in idle state	35.1	49.6
		Dual core running 128-bit data access instructions	41.8	56.3
	160	WAITI	27.6	42.3
		Single core running 32-bit data access instructions, the other core in idle state	39.9	54.6
		Dual core running 32-bit data access instructions	49.6	64.1
		Single core running 128-bit data access instructions, the other core in idle state	54.4	69.2
		Dual core running 128-bit data access instructions	66.7	81.1
	240	WAITI	32.9	47.6
		Single core running 32-bit data access instructions, the other core in idle state	51.2	65.9
		Dual core running 32-bit data access instructions	66.2	81.3
		Single core running 128-bit data access instructions, the other core in idle state	72.4	87.9
		Dual core running 128-bit data access instructions	91.7	107.9

[1] Current consumption when all peripheral clocks are **disabled**.

[2] Current consumption when all peripheral clocks are **enabled**. In practice, the current consumption might be different depending on which peripherals are enabled.

[3] In Modem-sleep mode, Wi-Fi is clock gated, and the current consumption might be higher when accessing flash. For a flash rated at 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

Table 13: Current Consumption in Low-Power Modes

Work mode	Description	Typ (μA)
Light-sleep[1]	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high-impedance.	240
Deep-sleep	RTC memory and RTC peripherals are powered up.	8
	RTC memory is powered up. RTC peripherals are powered down.	7

Power off	CHIP_PU is set to low level. The chip is shut down.	1

[1] In Light-sleep mode, all related SPI pins are pulled up. For chips embedded with PSRAM, please add corresponding PSRAM consumption values, e.g., 140 μA for 8 MB Octal PSRAM (3.3 V), 200 μA for 8 MB Octal PSRAM (1.8 V) and 40 μA for 2 MB Quad PSRAM (3.3 V).

7 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The external antennas used for the tests on the modules with external antenna connectors have an impedance of 50 Ω.Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

7.1 Wi-Fi Radio

Table 14: Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	2412 ~ 2484 MHz
Wi-Fi wireless standard	IEEE 802.11b/g/n

7.1.1 Wi-Fi RF Transmitter (TX) Characteristics

Table 15: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	20.5	—
802.11b, 11 Mbps	—	20.5	—
802.11g, 6 Mbps	—	20.0	—
802.11g, 54 Mbps	—	18.0	—
802.11n, HT20, MCS 0	—	19.0	—
802.11n, HT20, MCS 7	—	17.5	—
802.11n, HT40, MCS 0	—	18.5	—
802.11n, HT40, MCS 7	—	17.0	—

Table 16: TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11b, 1 Mbps, @20.5 dBm	—	-24.5	-10
802.11b, 11 Mbps, @20.5 dBm	—	-24.5	-10
802.11g, 6 Mbps, @20 dBm	—	-23.0	-5
802.11g, 54 Mbps, @18 dBm	—	-29.5	-25
802.11n, HT20, MCS 0, @19 dBm	—	-24.0	-5

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Table 16 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11n, HT20, MCS 7, @17.5 dBm	—	–30.5	–27
802.11n, HT40, MCS 0, @18.5 dBm	—	–25.0	–5
802.11n, HT40, MCS 7, @17 dBm	—	–30.0	–27

[1] EVM is measured at the corresponding typical TX power provided in Table 15 *TX Power with Spectral Mask and EVM Meeting 802.11 Standards* above.

7.1.2 Wi-Fi RF Receiver (RX) Characteristics

For RX tests, the PER (packet error rate) limit is 8% for 802.11b, and 10% for 802.11g/n.

Table 17: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	–98.2	—
802.11b, 2 Mbps	—	–95.6	—
802.11b, 5.5 Mbps	—	–92.8	—
802.11b, 11 Mbps	—	–88.5	—
802.11g, 6 Mbps	—	–93.0	—
802.11g, 9 Mbps	—	–92.0	—
802.11g, 12 Mbps	—	–90.8	—
802.11g, 18 Mbps	—	–88.5	—
802.11g, 24 Mbps	—	–85.5	—
802.11g, 36 Mbps	—	–82.2	—
802.11g, 48 Mbps	—	–78.0	—
802.11g, 54 Mbps	—	–76.2	—
802.11n, HT20, MCS 0	—	–93.0	—
802.11n, HT20, MCS 1	—	–90.6	—
802.11n, HT20, MCS 2	—	–88.4	—
802.11n, HT20, MCS 3	—	–84.8	—
802.11n, HT20, MCS 4	—	–81.6	—
802.11n, HT20, MCS 5	—	–77.4	—
802.11n, HT20, MCS 6	—	–75.6	—
802.11n, HT20, MCS 7	—	–74.2	—
802.11n, HT40, MCS 0	—	–90.0	—
802.11n, HT40, MCS 1	—	–87.5	—
802.11n, HT40, MCS 2	—	–85.0	—
802.11n, HT40, MCS 3	—	–82.0	—
802.11n, HT40, MCS 4	—	–78.5	—
802.11n, HT40, MCS 5	—	–74.4	—
802.11n, HT40, MCS 6	—	–72.5	—

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Table 17 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11n, HT40, MCS 7	—	–71.2	—

Table 18: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MCS 0	—	5	—
802.11n, HT20, MCS 7	—	0	—
802.11n, HT40, MCS 0	—	5	—
802.11n, HT40, MCS 7	—	0	—

Table 19: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps	—	35	—
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	14	—
802.11n, HT20, MCS 0	—	31	—
802.11n, HT20, MCS 7	—	13	—
802.11n, HT40, MCS 0	—	19	—
802.11n, HT40, MCS 7	—	8	—

7.2 Bluetooth LE Radio

Table 20: Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	–24.0 ~ 20.0 dBm

7.2.1 Bluetooth LE RF Transmitter (TX) Characteristics

Table 21: Bluetooth LE - Transmitter Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\ 1,\ 2,\ ..k}$	—	2.50	—	kHz
	Max $\|f_0 - f_n\|$	—	2.00	—	kHz
	Max $\|f_n - f_{n-5}\|$	—	1.40	—	kHz
	$\|f_1 - f_0\|$	—	1.00	—	kHz
Modulation characteristics	$\Delta\ f1_{avg}$	—	249.00	—	kHz
	Min $\Delta\ f2_{max}$ (for at least 99.9% of all $\Delta\ f2_{max}$)	—	198.00	—	kHz
	$\Delta\ f2_{avg}/\Delta\ f1_{avg}$	—	0.86	—	—
In-band spurious emissions	±2 MHz offset	—	-37.00	—	dBm
	±3 MHz offset	—	-42.00	—	dBm
	>±3 MHz offset	—	-44.00	—	dBm

Table 22: Bluetooth LE - Transmitter Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\ 1,\ 2,\ ..k}$	—	2.50	—	kHz
	Max $\|f_0 - f_n\|$	—	2.00	—	kHz
	Max $\|f_n - f_{n-5}\|$	—	1.40	—	kHz
	$\|f_1 - f_0\|$	—	1.00	—	kHz
Modulation characteristics	$\Delta\ f1_{avg}$	—	499.00	—	kHz
	Min $\Delta\ f2_{max}$ (for at least 99.9% of all $\Delta\ f2_{max}$)	—	416.00	—	kHz
	$\Delta\ f2_{avg}/\Delta\ f1_{avg}$	—	0.89	—	—
In-band spurious emissions	±4 MHz offset	—	-42.00	—	dBm
	±5 MHz offset	—	-44.00	—	dBm
	>±5 MHz offset	—	-47.00	—	dBm

Table 23: Bluetooth LE - Transmitter Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\ 1,\ 2,\ ..k}$	—	0.80	—	kHz
	Max $\|f_0 - f_n\|$	—	1.00	—	kHz
	$\|f_n - f_{n-3}\|$	—	0.30	—	kHz
	$\|f_0 - f_3\|$	—	1.00	—	kHz
Modulation characteristics	$\Delta\ f1_{avg}$	—	248.00	—	kHz
	Min $\Delta\ f1_{max}$ (for at least 99.9% of all$\Delta\ f1_{max}$)	—	222.00	—	kHz
In-band spurious emissions	±2 MHz offset	—	-37.00	—	dBm
	±3 MHz offset	—	-42.00	—	dBm
	>±3 MHz offset	—	-44.00	—	dBm

Table 24: Bluetooth LE - Transmitter Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\ 1,\ 2,\ ..k}$	—	0.80	—	kHz
	Max $\|f_0 - f_n\|$	—	1.00	—	kHz
	$\|f_n - f_{n-3}\|$	—	0.85	—	kHz
	$\|f_0 - f_3\|$	—	0.34	—	kHz
Modulation characteristics	$\Delta\ f2_{avg}$	—	213.00	—	kHz
	Min $\Delta\ f2_{max}$ (for at least 99.9% of all $\Delta\ f2_{max}$)	—	196.00	—	kHz
In-band spurious emissions	±2 MHz offset	—	−37.00	—	dBm
	±3 MHz offset	—	−42.00	—	dBm
	>±3 MHz offset	—	−44.00	—	dBm

7.2.2 Bluetooth LE RF Receiver (RX) Characteristics

Table 25: Bluetooth LE - Receiver Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	−96.5	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	8	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	4	—	dB
	F = F0 − 1 MHz	—	4	—	dB
	F = F0 + 2 MHz	—	−23	—	dB
	F = F0 − 2 MHz	—	−23	—	dB
	F = F0 + 3 MHz	—	−34	—	dB
	F = F0 − 3 MHz	—	−34	—	dB
	F > F0 + 3 MHz	—	−36	—	dB
	F > F0 − 3 MHz	—	−37	—	dB
Image frequency	—	—	−36	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	−39	—	dB
	F = F_{image} − 1 MHz	—	−34	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	−12	—	dBm
	2003 MHz ~ 2399 MHz	—	−18	—	dBm
	2484 MHz ~ 2997 MHz	—	−16	—	dBm
	3000 MHz ~ 12.75 GHz	—	−10	—	dBm
Intermodulation	—	—	−29	—	dBm

Table 26: Bluetooth LE - Receiver Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	−92	—	dBm
Maximum received signal @30.8% PER	—	—	3	—	dBm

Cont'd on next page

Table 26 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
Co-channel C/I	F = F0 MHz	—	8	—	dB
Adjacent channel selectivity C/I	F = F0 + 2 MHz	—	4	—	dB
	F = F0 – 2 MHz	—	4	—	dB
	F = F0 + 4 MHz	—	–27	—	dB
	F = F0 – 4 MHz	—	–27	—	dB
	F = F0 + 6 MHz	—	–38	—	dB
	F = F0 – 6 MHz	—	–38	—	dB
	F > F0 + 6 MHz	—	–41	—	dB
	F > F0 – 6 MHz	—	–41	—	dB
Image frequency	—	—	–27	—	dB
Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–38	—	dB
	F = F_{image} – 2 MHz	—	4	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–15	—	dBm
	2003 MHz ~ 2399 MHz	—	–21	—	dBm
	2484 MHz ~ 2997 MHz	—	–21	—	dBm
	3000 MHz ~ 12.75 GHz	—	–9	—	dBm
Intermodulation	—	—	–29	—	dBm

Table 27: Bluetooth LE - Receiver Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–103.5	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	4	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	1	—	dB
	F = F0 – 1 MHz	—	2	—	dB
	F = F0 + 2 MHz	—	–26	—	dB
	F = F0 – 2 MHz	—	–26	—	dB
	F = F0 + 3 MHz	—	–36	—	dB
	F = F0 – 3 MHz	—	–39	—	dB
	F > F0 + 3 MHz	—	–42	—	dB
	F > F0 – 3 MHz	—	–43	—	dB
Image frequency	—	—	–42	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–43	—	dB
	F = F_{image} – 1 MHz	—	–36	—	dB

Table 28: Bluetooth LE - Receiver Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–100	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	4	—	dB

Cont'd on next page

Table 28 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
Adjacent channel selectivity C/I	F = FO + 1 MHz	—	1	—	dB
	F = FO – 1 MHz	—	0	—	dB
	F = FO + 2 MHz	—	–24	—	dB
	F = FO – 2 MHz	—	–24	—	dB
	F = FO + 3 MHz	—	–37	—	dB
	F = FO – 3 MHz	—	–39	—	dB
	F > FO + 3 MHz	—	–38	—	dB
	F > FO – 3 MHz	—	–42	—	dB
Image frequency	—	—	–38	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–42	—	dB
	F = F_{image} – 1 MHz	—	–37	—	dB

8 Module Schematics

This is the reference design of the module.

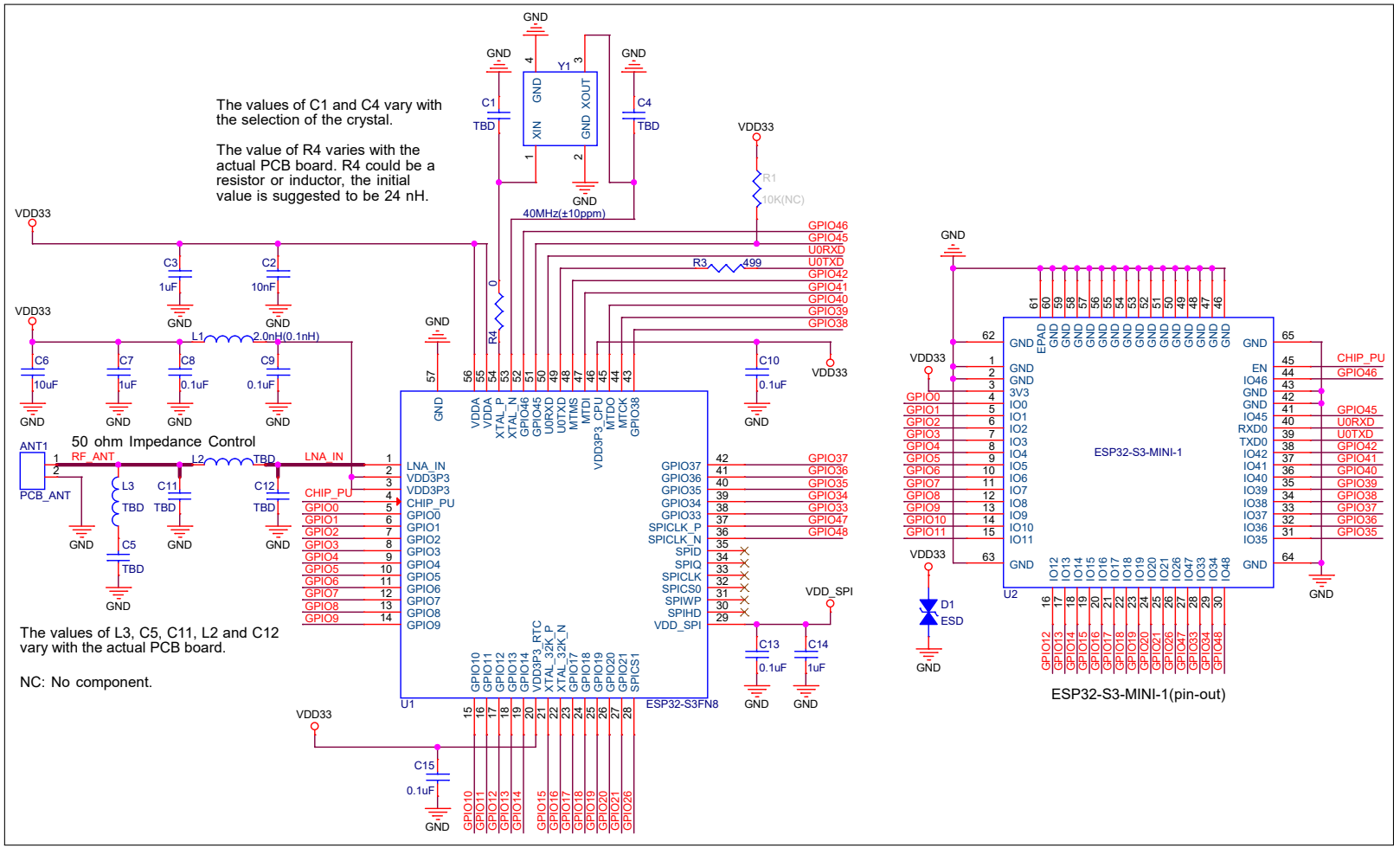

Figure 5: ESP32-S3-MINI-1 Schematics

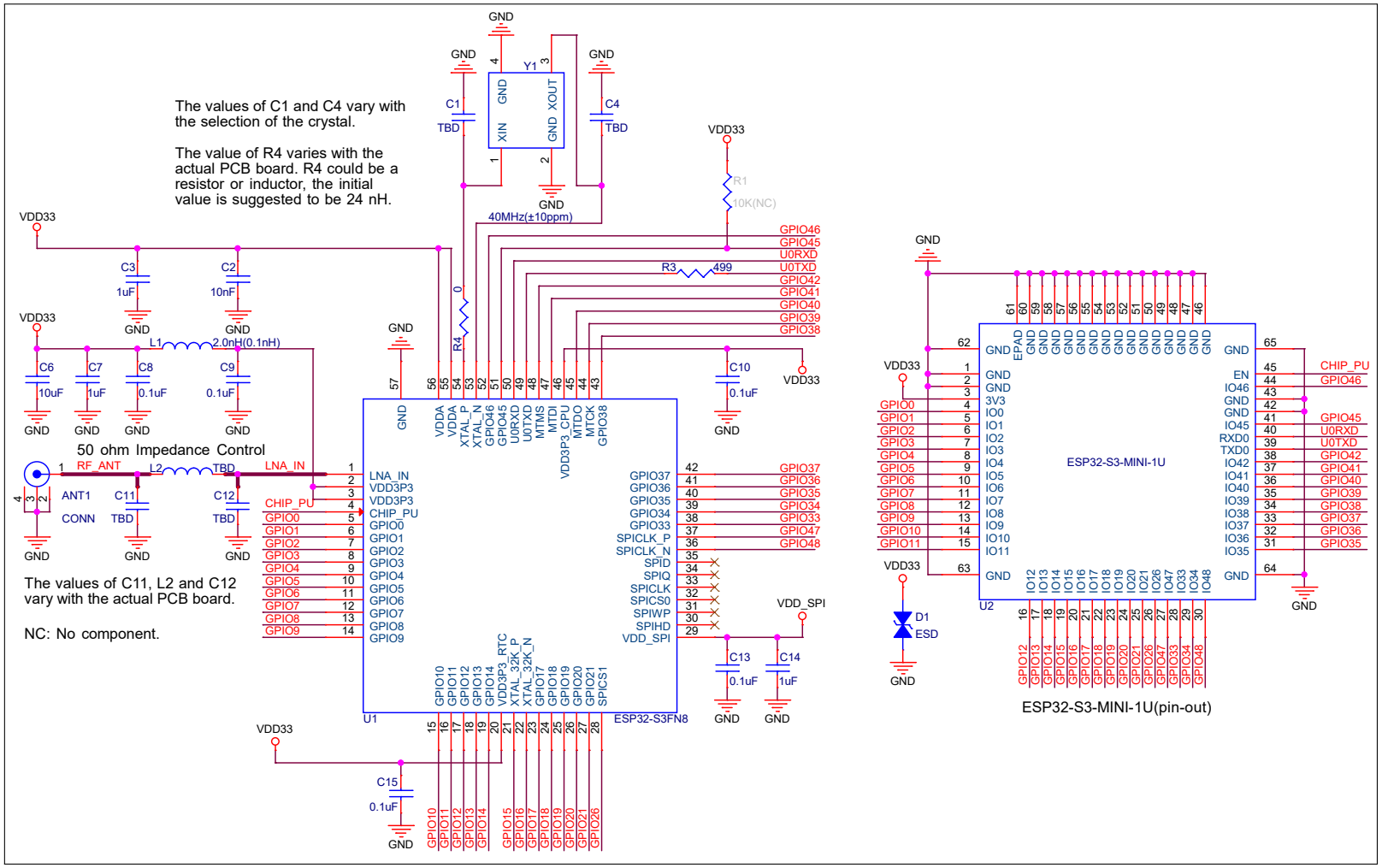

Figure 6: ESP32-S3-MINI-1U Schematics

9 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

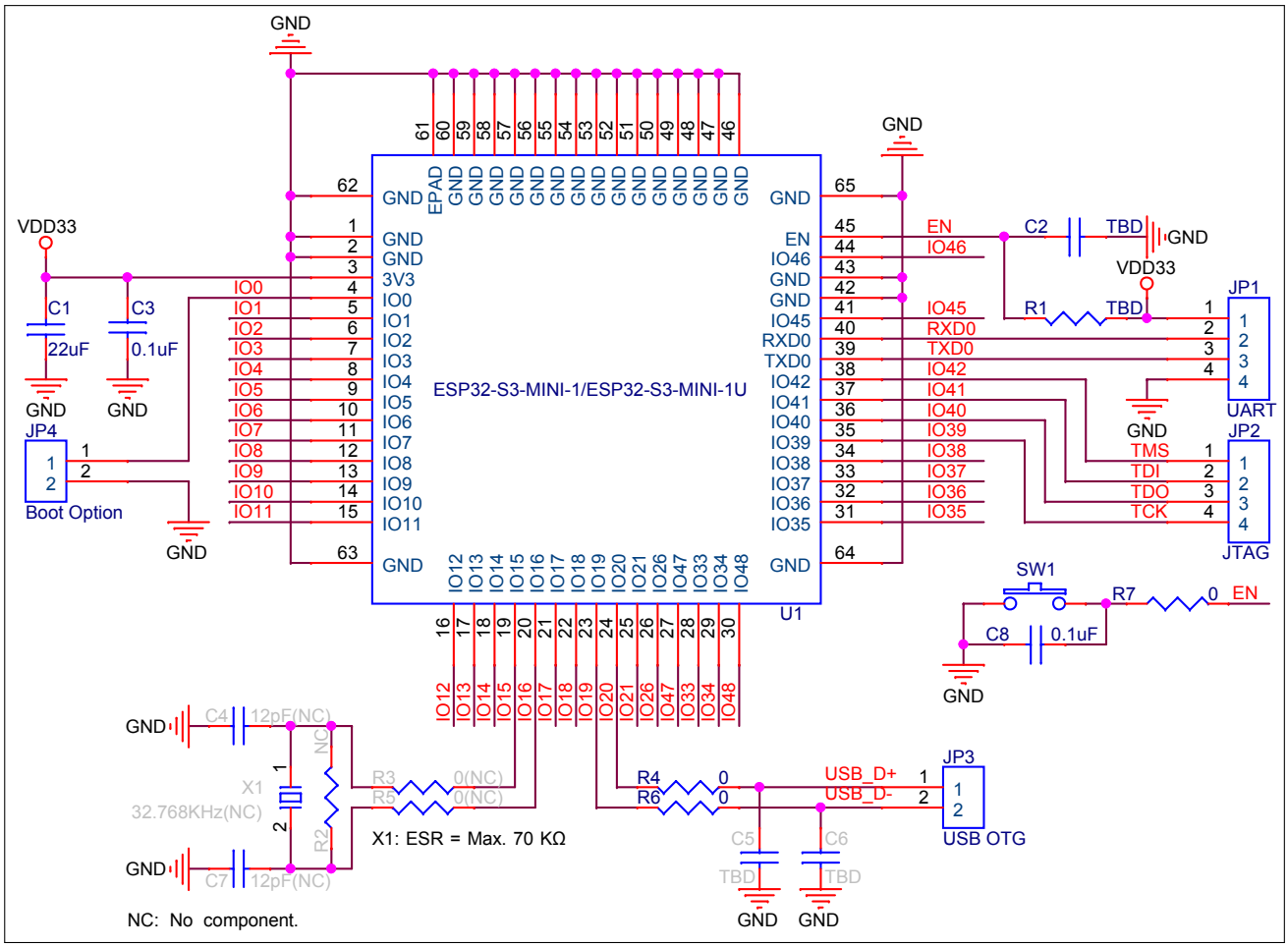

Figure 7: Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32-S3 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S3's power-up and reset sequence timing diagram, please refer to *ESP32-S3 Series Datasheet* > Section *Power Supply*.

10 Physical Dimensions

10.1 Module Dimensions

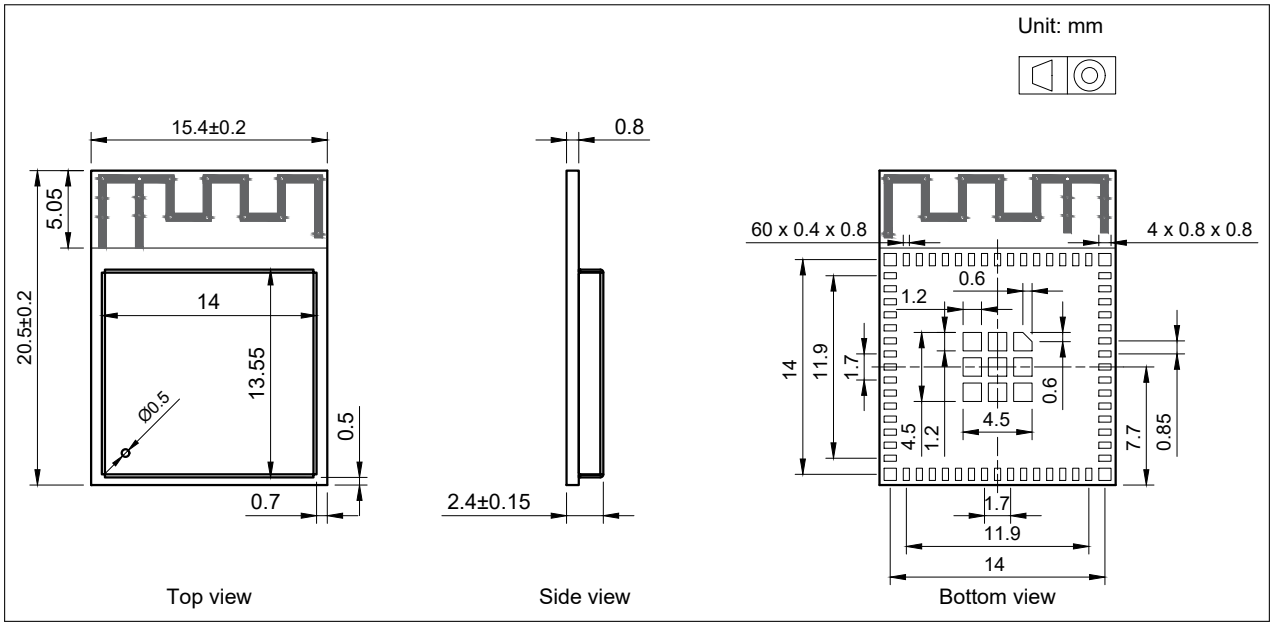

Figure 8: ESP32-S3-MINI-1 Physical Dimensions

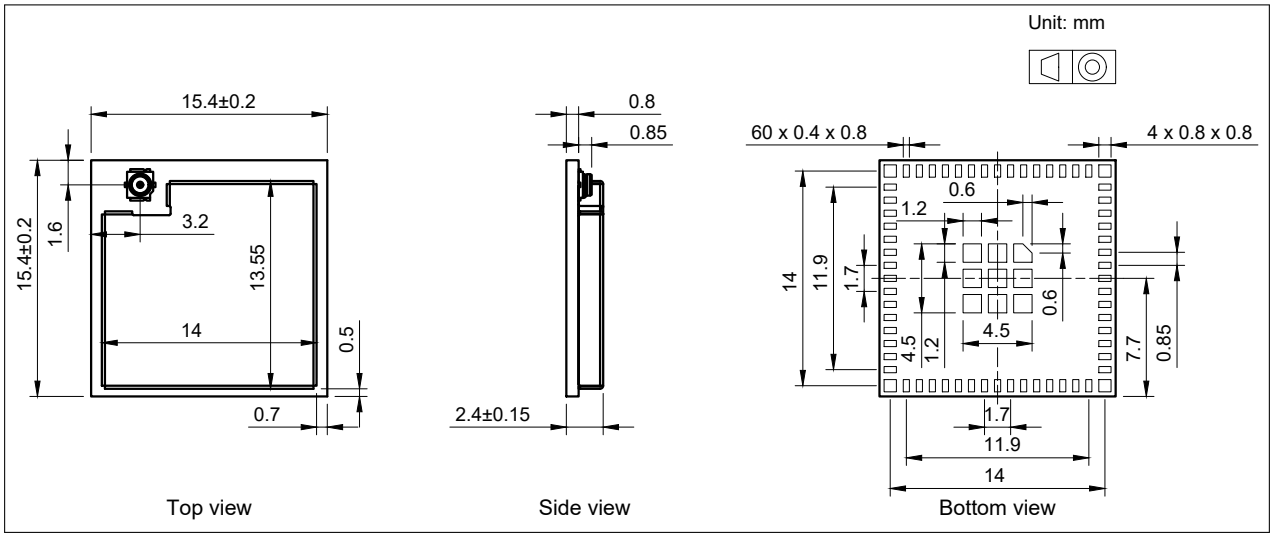

Figure 9: ESP32-S3-MINI-1U Physical Dimensions

Note:

For information about tape, reel, and product marking, please refer to *ESP32-S3 Module Packaging Information*.

10.2 Dimensions of External Antenna Connector

ESP32-S3-MINI-1U uses the third generation external antenna connector as shown in Figure 10 *Dimensions of External Antenna Connector*. This connector is compatible with the following connectors:

- W.FL Series connector from Hirose
- MHF III connector from I-PEX
- AMMC connector from Amphenol

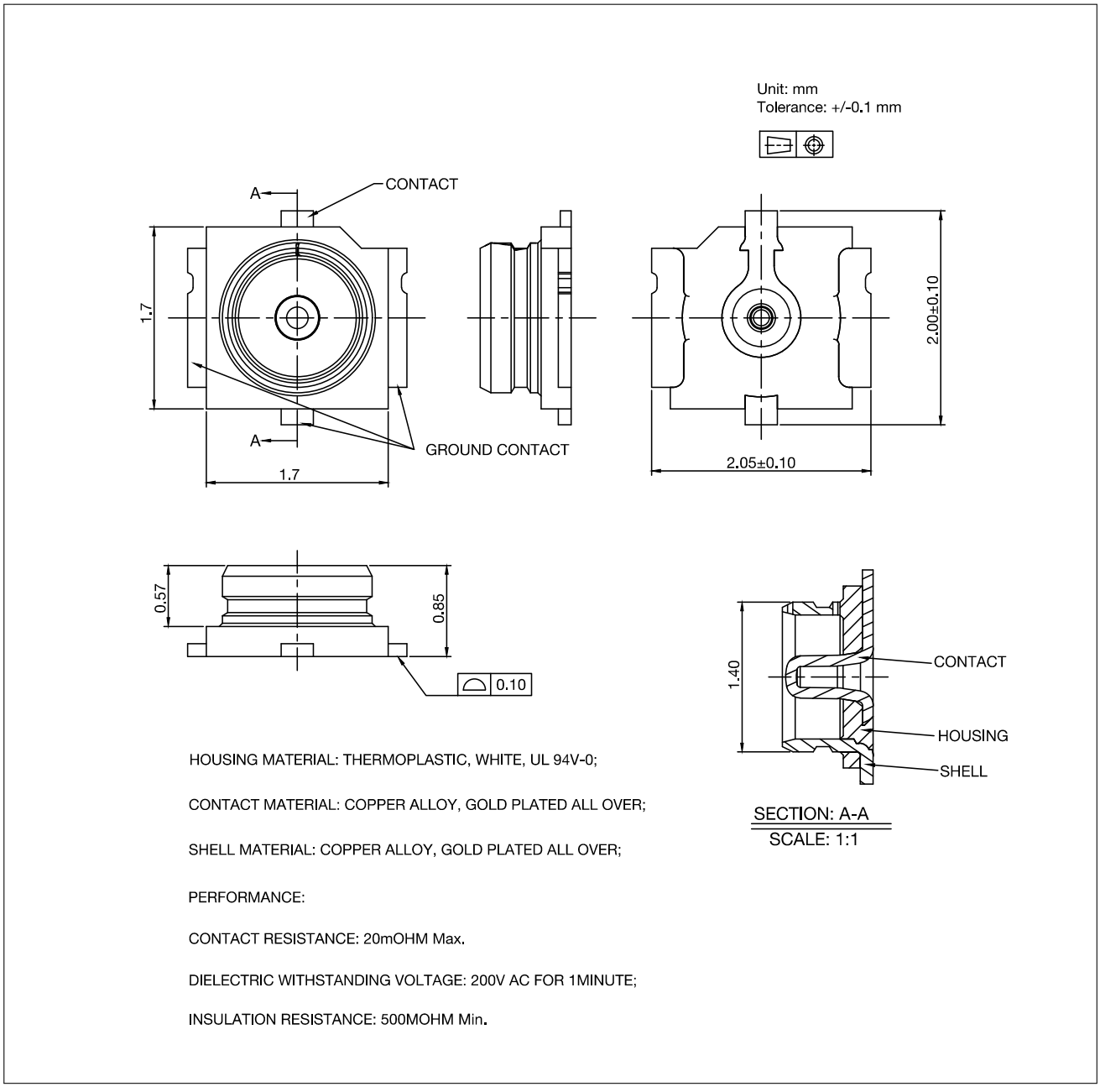

Figure 10: Dimensions of External Antenna Connector

11 PCB Layout Recommendations

11.1 PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 11 *ESP32-S3-MINI-1 Recommended PCB Land Pattern* and Figure 12 *ESP32-S3-MINI-1U Recommended PCB Land Pattern*.
- Source files of recommended PCB land patterns to measure dimensions not covered in Figure 11 and Figure 12. You can view the source files for ESP32-S3-MINI-1 and ESP32-S3-MINI-1U with Autodesk Viewer.
- 3D models of ESP32-S3-MINI-1 and ESP32-S3-MINI-1U. Please make sure that you download the 3D model file in .STEP format (beware that some browsers might add .txt).

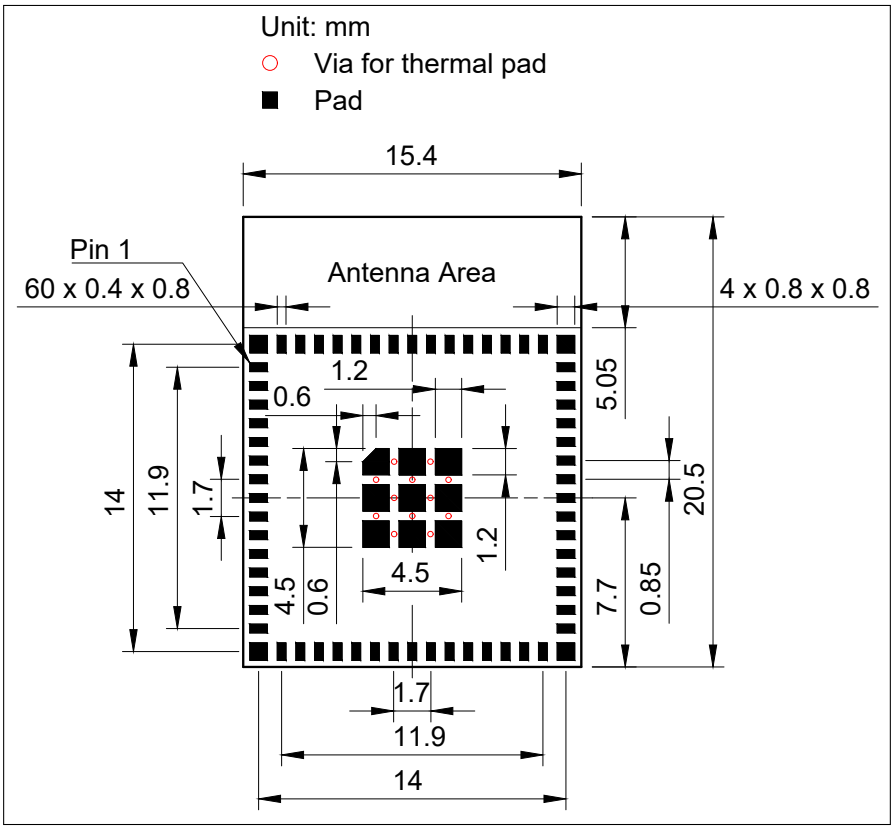

Figure 11: ESP32-S3-MINI-1 Recommended PCB Land Pattern

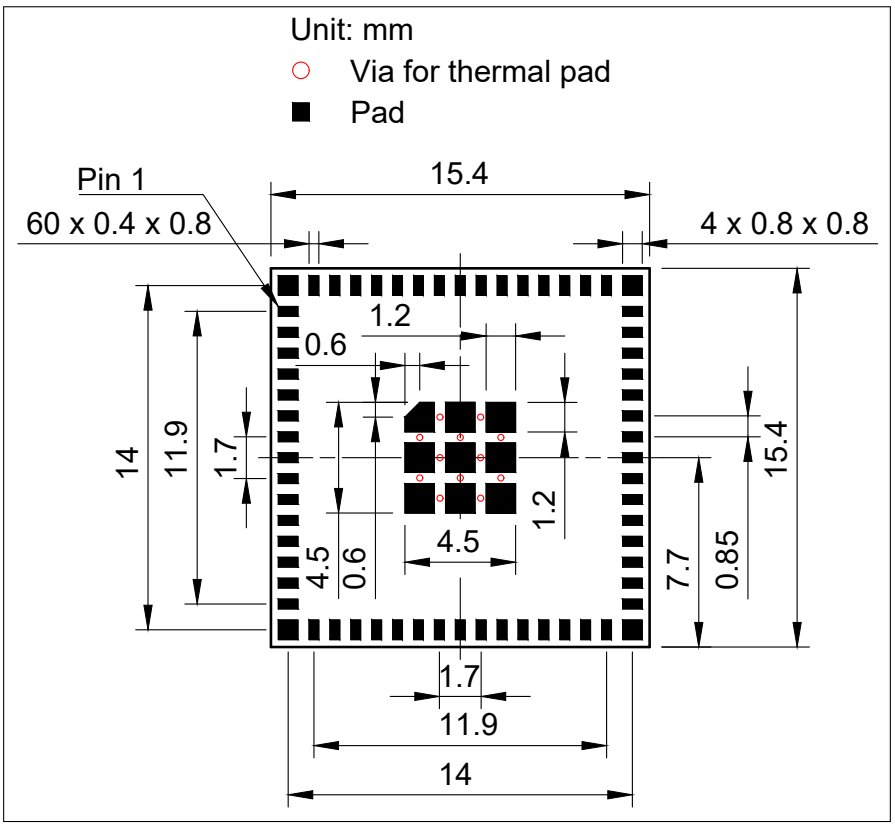

Figure 12: ESP32-S3-MINI-1U Recommended PCB Land Pattern

11.2 Module Placement for PCB Design

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

For details about module placement for PCB design, please refer to *ESP32-S3 Hardware Design Guidelines* > Section *Positioning a Module on a Base Board*.

12 Product Handling

12.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and 60%RH. If the above conditions are not met, the module needs to be baked.

12.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

12.3 Reflow Profile

Solder the module in a single reflow.

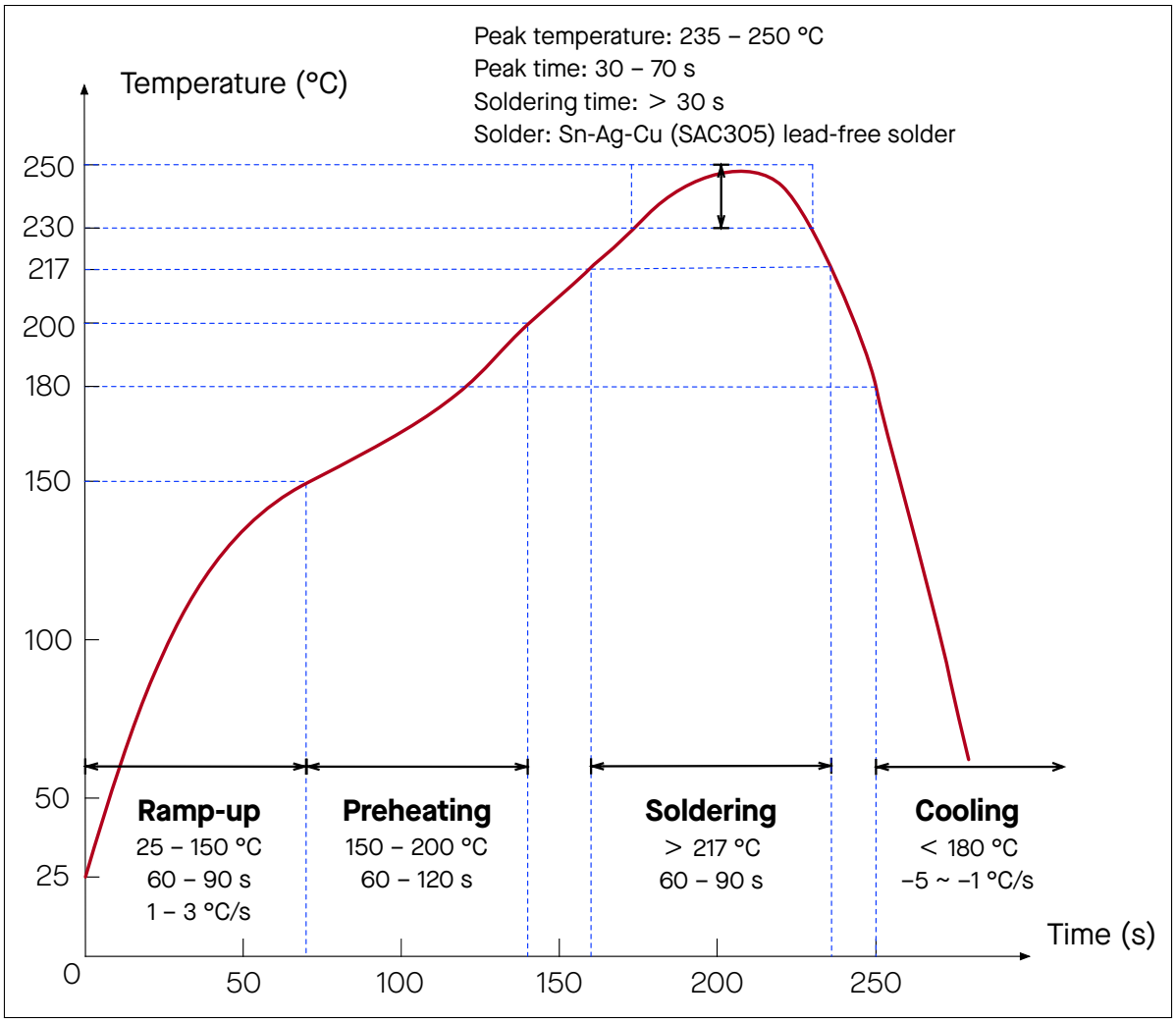

Figure 13: Reflow Profile

12.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

Related Documentation and Resources

Related Documentation

- ESP32-S3 Series Datasheet – Specifications of the ESP32-S3 hardware.
- ESP32-S3 Technical Reference Manual – Detailed information on how to use the ESP32-S3 memory and peripherals.
- ESP32-S3 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-S3 into your hardware product.
- ESP32-S3 Series SoC Errata – Descriptions of known errors in ESP32-S3 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S3 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-S3
- *ESP32-S3 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-S3
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S3 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S3 Series SoCs* – Browse through all ESP32-S3 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S3
- *ESP32-S3 Series Modules* – Browse through all ESP32-S3-based modules.
  https://espressif.com/en/products/modules?id=ESP32-S3
- *ESP32-S3 Series DevKits* – Browse through all ESP32-S3-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-S3
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Revision History

Date	Version	Release notes
2025-06-10	v1.4	• Added a note about the pin mapping between the chip and the in-package flash/PSRAN in Section 2 *Block Diagram*
2024-11-14	v1.3	• Added flash memory program/erase cycle and data retention details in the table note of Table 1 *ESP32-S3-MINI-1 and ESP32-S3-MINI-1U Series Comparison* and added a reference to the chip revision information in the following note in Section 1.2 *Series Comparison* • Updated Section 1.3 *Applications* • Restructured the previous Section *Strapping Pins* as Section 4 *Boot Configurations* • Added Section 5.2 *Peripheral Description* • Divided Section *Electrical Characteristics* into Section 6 *Electrical Characteristics* and Section 7 *RF Characteristics* with updated formatting and wording • Divided Section *Physical Dimensions and PCB Land Pattern* into Section 10 *Physical Dimensions* and 11 *PCB Layout Recommendations* and added Section 11.2 *Module Placement for PCB Design* • Added the 3D model link of ESP32-S3-MINI-1U in Section 11.1 *PCB Land Pattern* • Updated Figure 13 *Reflow Profile* • Other minor updates to formatting and wording
2023-11-24	v1.2	• Removed the table note about ESP32-S3FH4R2 sample status from Table 1 *ESP32-S3-MINI-1 and ESP32-S3-MINI-1U Series Comparison* and added the second table note • Updated Section 4.1 *Chip Boot Mode Control* • Updated the module schematics in Section 8 *Module Schematics* • Updated the physical dimensions figure in Section 10.1 *Module Dimensions* • Updated the recommended PCB land pattern figure in Section 11.1 *PCB Land Pattern* • Other minor updates

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Date	Version	Release notes
2023-03-07	v1.1	• Remove module variants ESP32-S3-MINI-1-H4R2 and ESP32-S3-MINI-1U-H4R2 • Update the descriptions and Table 1 *ESP32-S3-MINI-1 and ESP32-S3-MINI-1U Series Comparison* in Section 1.2 *Series Comparison* • Update Section *Strapping Pins* • Update Section 6.4 *Current Consumption Characteristics* • Update the minimum value of RF transmit power in Section 7.2.1 *Bluetooth LE RF Transmitter (TX) Characteristics* • Update descriptions in Section 9 *Peripheral Schematics* • Add descriptions in Section 11.1 *PCB Land Pattern* • Update Section 12.4 • Other minor updates
2022-05-24	v1.0	• Update information about flash and PSRAM on the title page and in Section 1.1 • Add certification and test information • Add information of new module variants and their ambient operating temperature versions in Table 1 • Add the second note in Table 2 • Update Section *Strapping Pins* • Add notes in Table 13 • Update Bluetooth LE RF data • Update module schematics in Section 8 • Other minor updates
2021-11-16	v0.6	Overall update for chip revision 1
2021-03-30	v0.1	Preliminary release, for chip revision 0

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