64-bit PowerPC Microprocessors Memory Management

-- Gang Zhang

-- Yang Luan

Abbreviations

EA	Effective Address	64-bit
VA	Virtual Address	80-bit
PA	Physical Address	62-bit
SDR1	Storage Description Register 1	
MSR	Machine State Register	

PR[49]: Privilege level

If set, run in user mode

IR[58] / DR [59]: Instruction address translation / Data address translation

If set, Instruction/Data address translation is enabled

Feature Category	64-Bit Imple
	Conventional
Address ranges	2^{64} bytes of effective address
	2^{n} where $65 \leq n \leq 80$ bytes of virtual address
	$\leq 2^{m}$ ($m \leq 62$) bytes of physical address
Page size	4 Kbytes Some large page sizes (2^{p} where $13 \leq p \leq 28$)
Segment size	256 Mbytes
Block address translation	Not applicable
	Not applicable
Memory protection	Segments selectable as no-execute
	Pages selectable as user/supervisor and read-only
	Blocks selectable as user/supervisor and read-only
Page history	Referenced and changed bits defined and main-tained
Page address translation	Translations stored as PTEs in hashed page tables in memory
	Page table size determined by size programmed into SDR1 register
TLBs	Instructions for maintaining optional TLBs
Segment descriptors	Stored as STEs (explicit or implicit segment tables)
	Instructions for maintaining SLBs

Memory Addressing Overview

- PowerPC processors support two types of address translation:

Real addressing mode

EA = PA

Page address translation

translates the EA to VA then to PA.

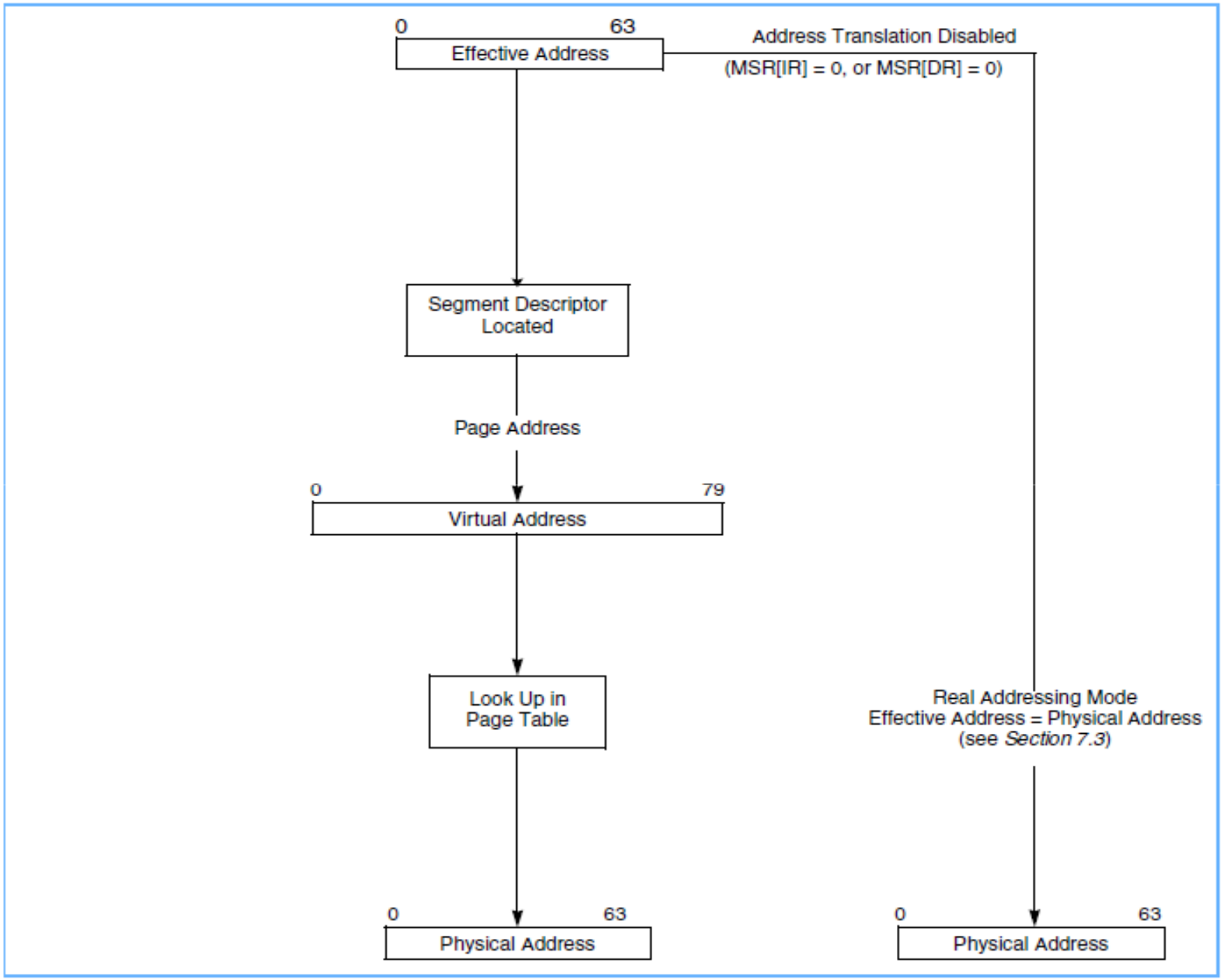
Real Addressing Mode

MSR[IR] = 0 or MSR[DR] = 0

- EA is treated as PA.
- Bypass all memory protection checks.
- Processor would set MSR[IR] = 0 and MSR[DR] = 0 after exceptions occur. Must explicitly enable translation if needed.
- Attempts to access PA not physically present will cause a machine check exception

Page address translation

- The page translation proceeds in the following two steps:
- 1. From effective address to the virtual address, and
- 2. From virtual address to physical address.

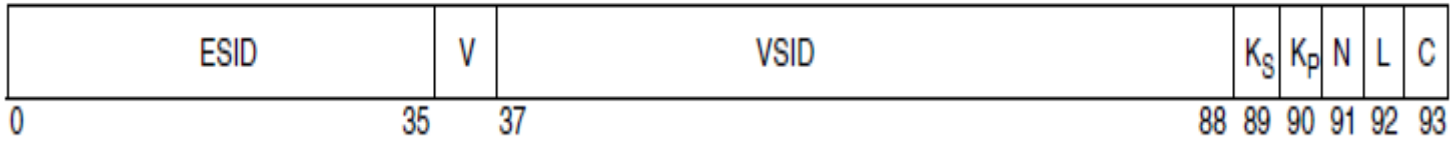

0
63
Effective Address
Address Translation Disabled
(MSR[IR] = 0, or MSR[DR] = 0)
Segment Descriptor Located
Page Address
0
79
Virtual Address
Look Up in Page Table
Real Addressing Mode
Effective Address = Physical Address
(see Section 7.3)
0
63
Physical Address
0
63
Physical Address

EA to VA

- Segment Lookaside Buffer (SLB)

  Each SLB entry maps one ESID (Effective Segment ID) to one VSID (Virtual Segment ID).

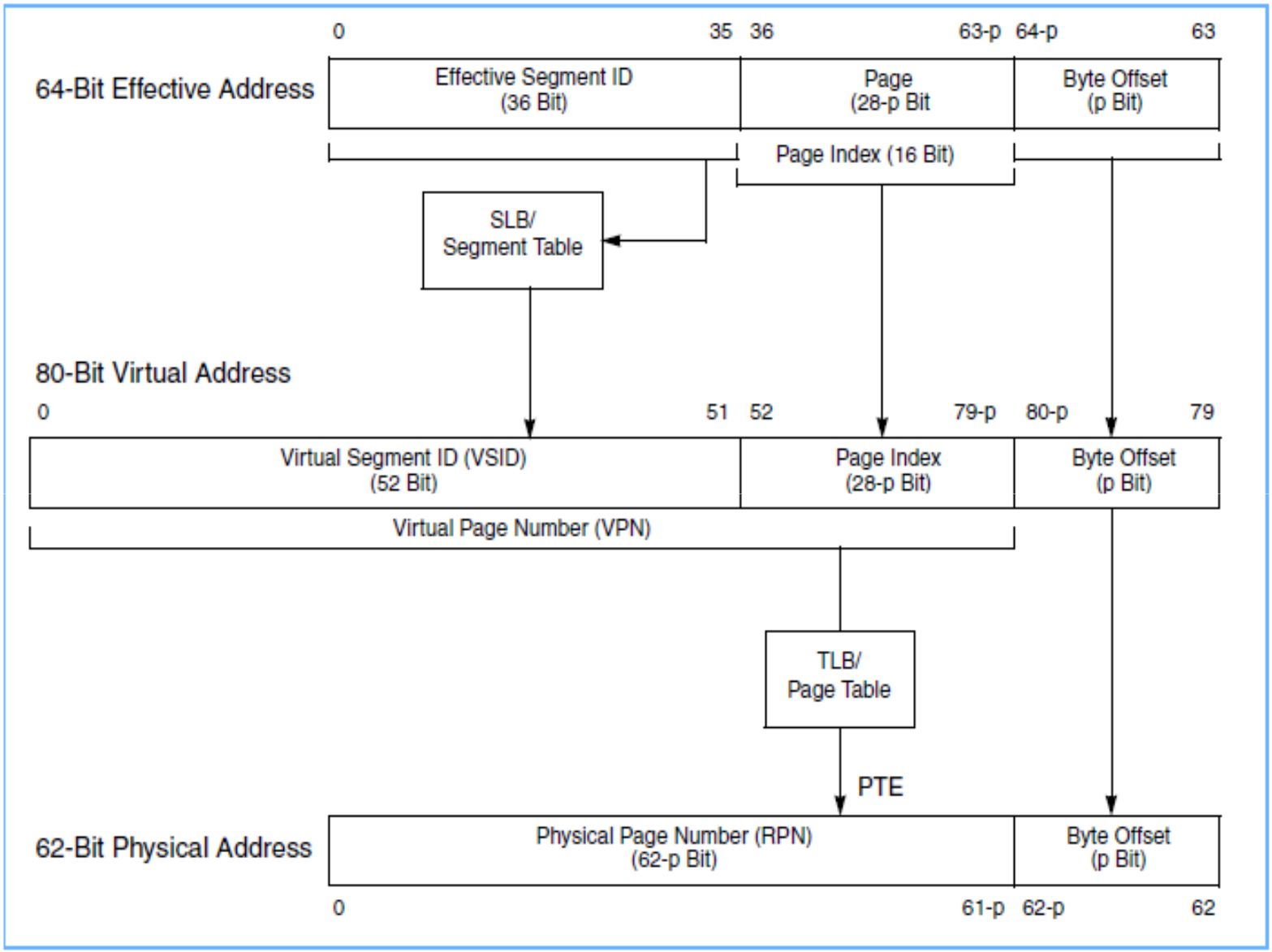
SLB entry format



- SLB Search

  Success if

  SLBE[V] = 1 and SLBE[ESID] = EA[0-35]

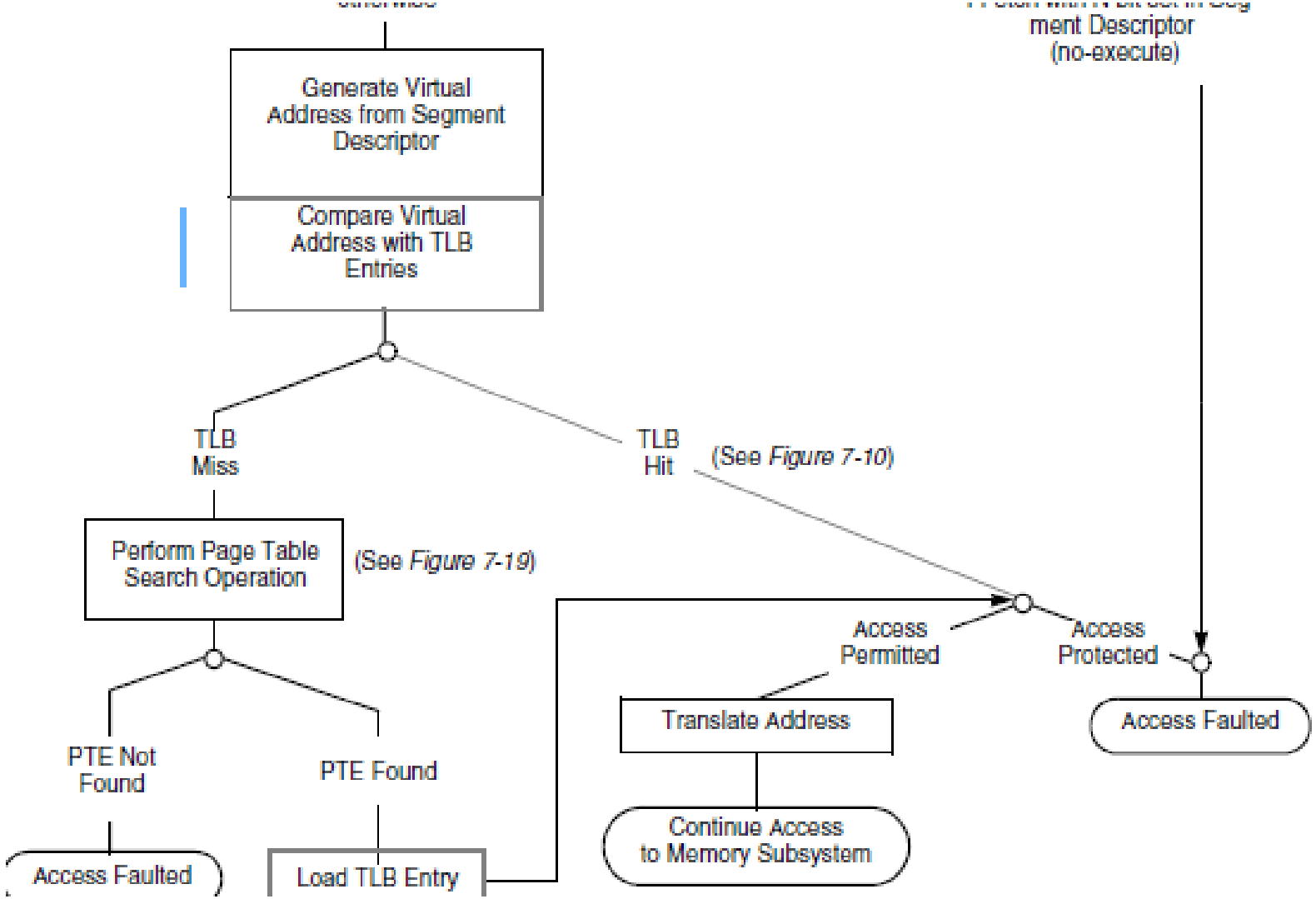

0
35
36
63-p
64-p
63
64-Bit Effective Address
Effective Segment ID
(36 Bit)
Page
(28-p Bit
Byte Offset
(p Bit)
Page Index (16 Bit)
SLB/
Segment Table
80-Bit Virtual Address
0
51
52
79-p
80-p
79
Virtual Segment ID (VSID)
(52 Bit)
Page Index
(28-p Bit)
Byte Offset
(p Bit)
Virtual Page Number (VPN)
TLB/
Page Table
PTE
62-Bit Physical Address
Physical Page Number (RPN)
(62-p Bit)
Byte Offset
(p Bit)
0
61-p
62-p
62

VA to PA

Translation Lookaside Buffer (TLB)

- Holds PTEs that have recently been used.
- Prior to searching the page table.
- Needs to keep consistency with the page table.
- Not required in 64-bit PowerPC architecture.

VA to PA cont.


ment Descriptor
(no-execute)
Generate Virtual Address from Segment Descriptor
Compare Virtual Address with TLB Entries
TLB Miss
TLB Hit
(See Figure 7-10)
Perform Page Table Search Operation
(See Figure 7-19)
Access Permitted
Access Protected
Translate Address
Access Faulted
PTE Not Found
PTE Found
Continue Access to Memory Subsystem
Access Faulted
Load TLB Entry

VA to PA cont.

- Hashed Page Tables

  If the PTE we search is not resident in a TLB.
- Page table entry groups (PTEG)

  The page table contains a number of PTEGs.

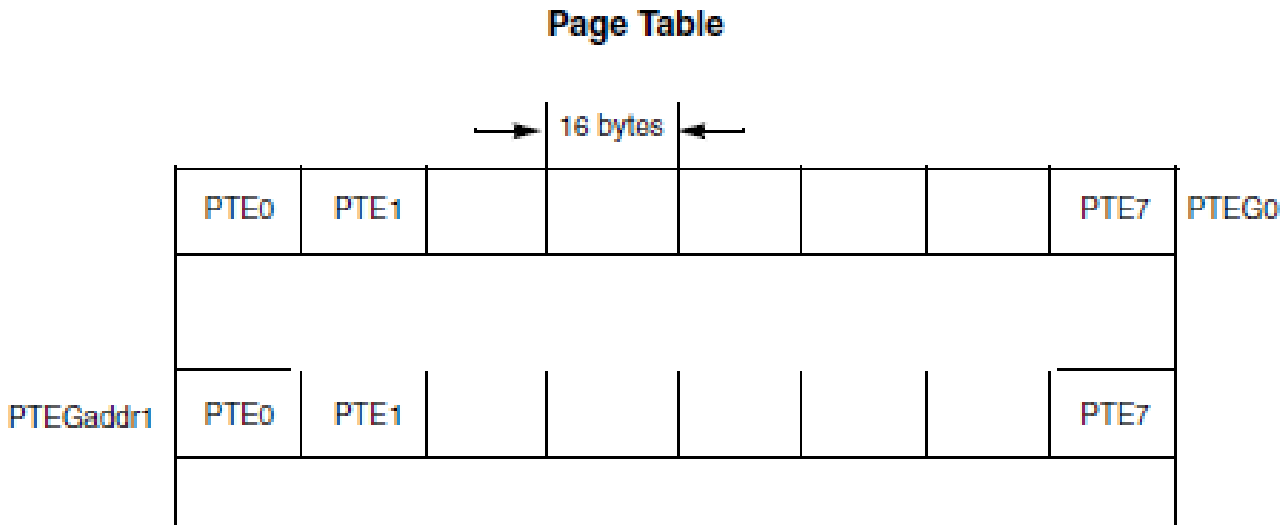
  A PTEG contains eight page table entries (PTE).
- Page table Entry (PTE)

  A PTE can reside in two possible PTEGs, primary and secondary.

VA to PA cont.

- Locate PTEG

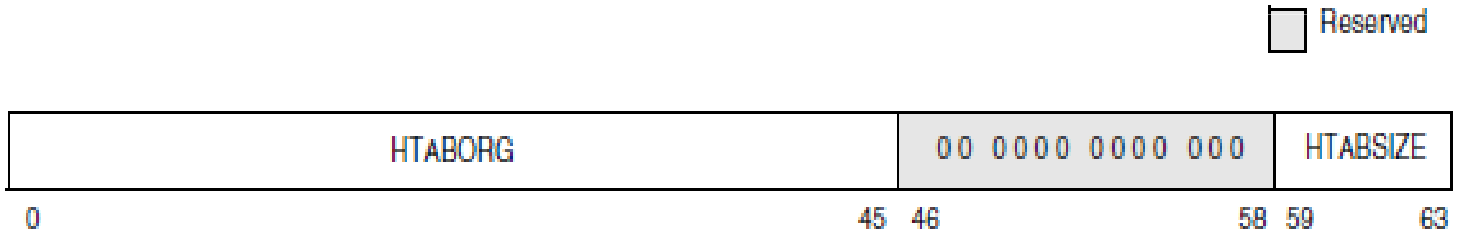
  The address of PTEG is derived from the **HTABORG** field of the SDR1 register and **output of hashing function** of VA.



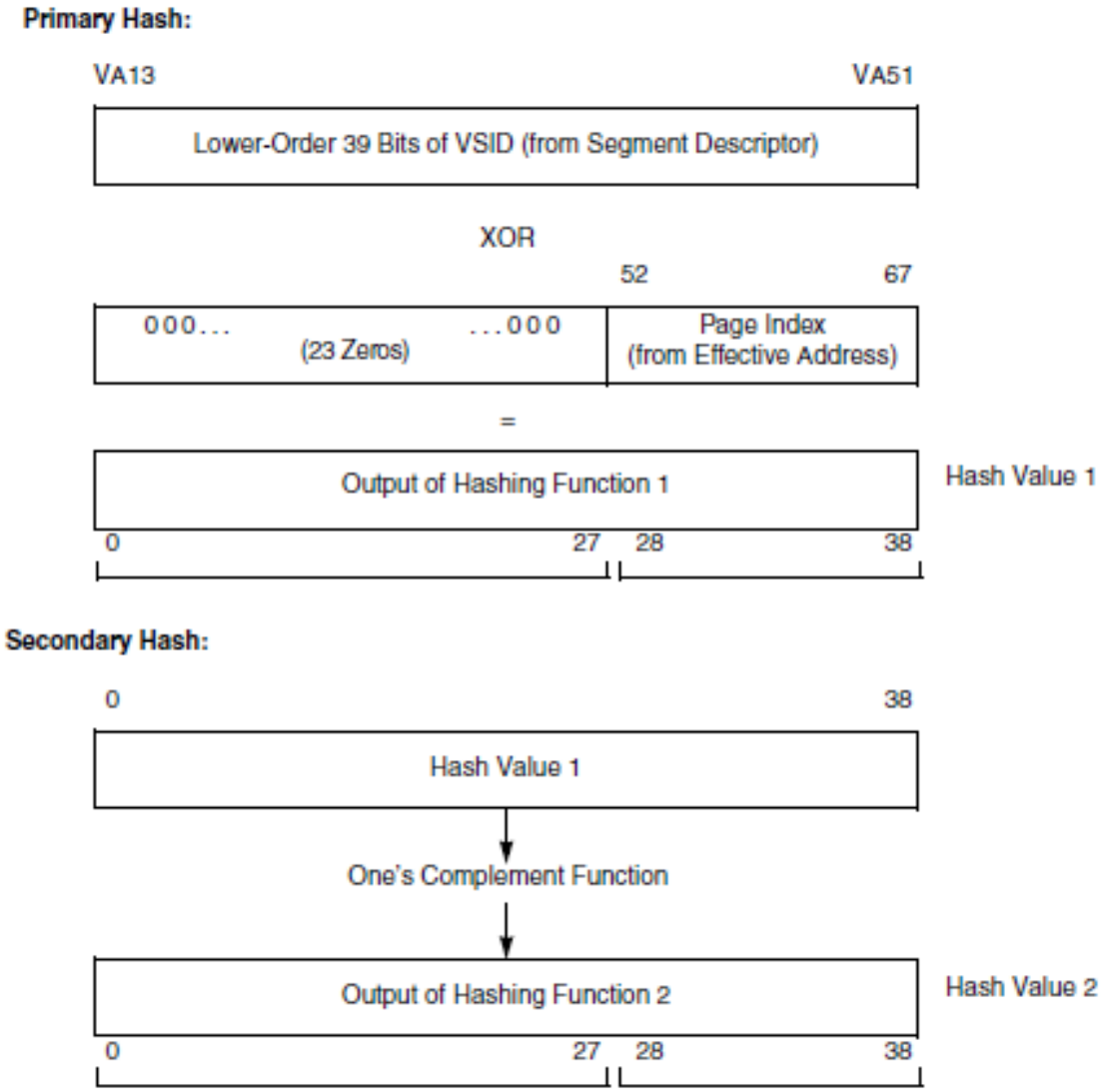
VA to PA cont.

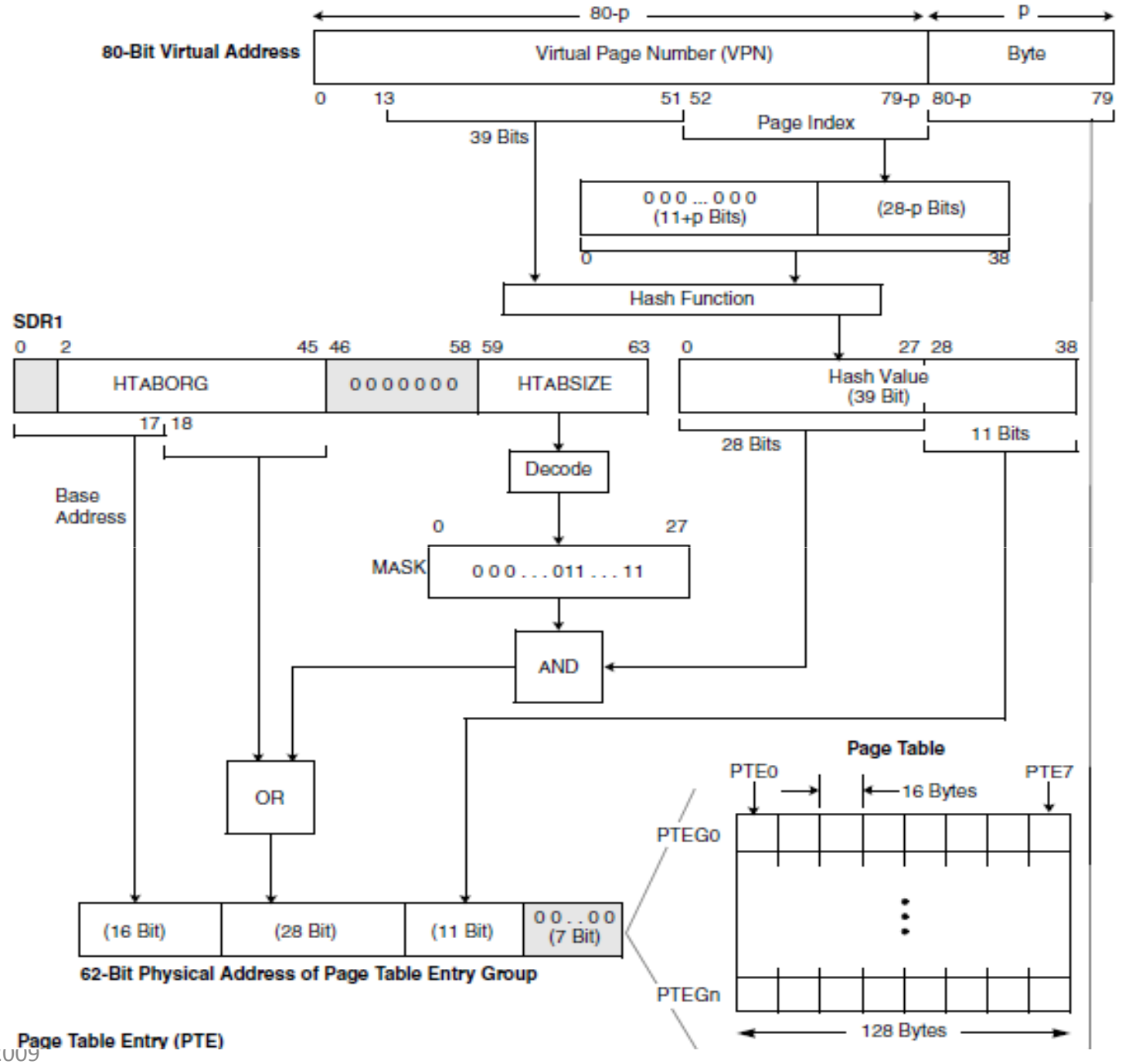
- Storage Description Register (SDR1)

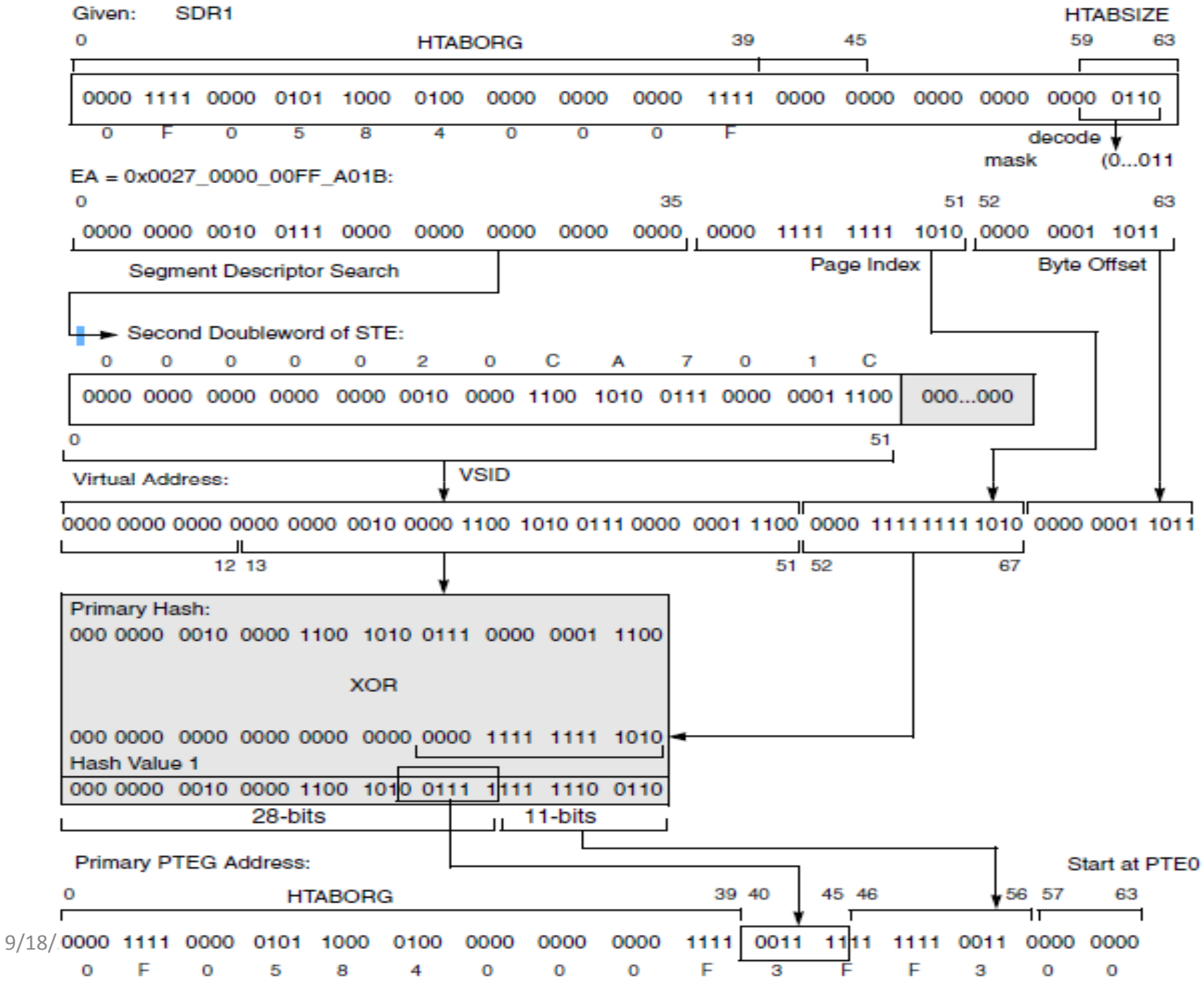
  SDR1 defines the **physical base address** of page table and the size of the table.



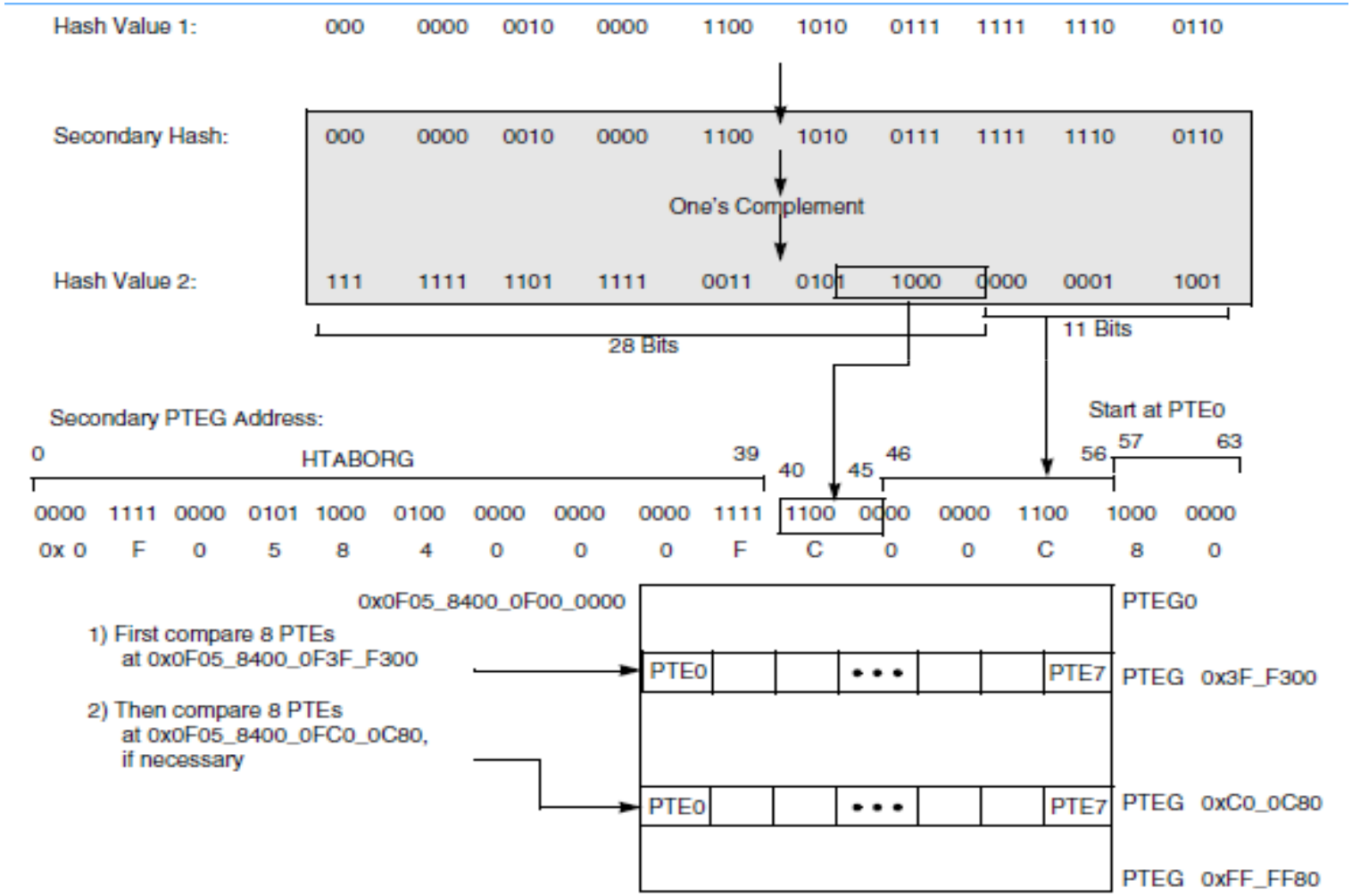
VA to PA cont. (Hashing function)




80-p
p
80-Bit Virtual Address
Virtual Page Number (VPN)
Byte
0
13
51 52
79-p 80-p
79
Page Index
39 Bits
0 0 0 ... 0 0 0
(11+p Bits)
(28-p Bits)
0
38
Hash Function
SDR1
0 2
45 46
58 59
63
HTABORG
0 0 0 0 0 0 0
HTABSIZE
0
27 28
38
Hash Value
(39 Bit)
17 18
28 Bits
11 Bits
Decode
Base
Address
0
27
MASK
0 0 0 . . . 0 1 1 . . . 1 1
AND
OR
Page Table
PTE0
16 Bytes
PTE7
PTEG0
PTEGn
(16 Bit)
(28 Bit)
(11 Bit)
0 0 . . 0 0
(7 Bit)
62-Bit Physical Address of Page Table Entry Group
128 Bytes
Page Table Entry (PTE)

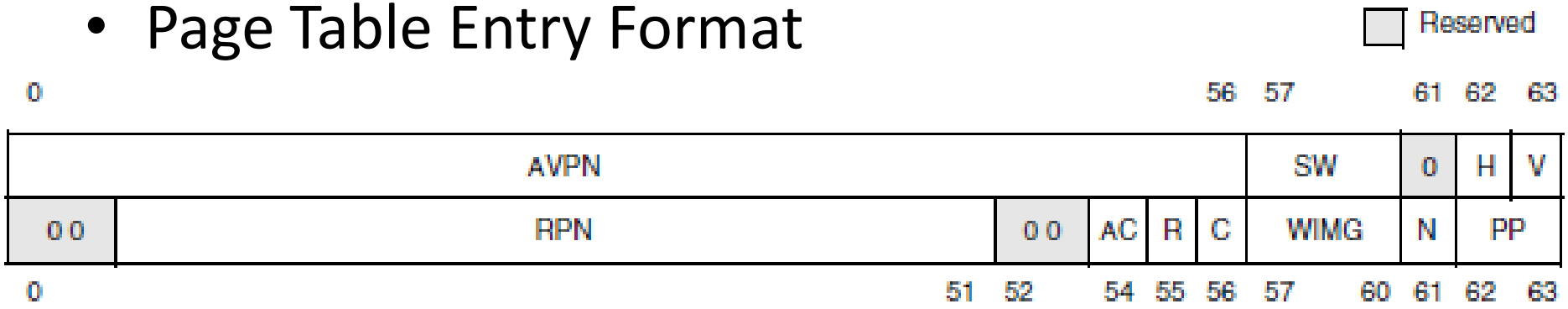

Given: SDR1
HTABSIZE
0
HTABORG
39
45
59
63
0000 1111 0000 0101 1000 0100 0000 0000 0000 1111 0000 0000 0000 0000 0000 0110
0 F 0 5 8 4 0 0 0 F
decode
mask (0...011
EA = 0x0027_0000_00FF_A01B:
0
35
51
52
63
0000 0000 0010 0111 0000 0000 0000 0000 0000 0000 1111 1111 1010 0000 0001 1011
Segment Descriptor Search
Page Index
Byte Offset
Second Doubleword of STE:
0 0 0 0 0 2 0 C A 7 0 1 C
0000 0000 0000 0000 0000 0010 0000 1100 1010 0111 0000 0001 1100 000...000
0
51
Virtual Address:
VSID
0000 0000 0000 0000 0000 0010 0000 1100 1010 0111 0000 0001 1100 0000 1111 1111 1010 0000 0001 1011
12 13
51 52
67
Primary Hash:
000 0000 0010 0000 1100 1010 0111 0000 0001 1100
XOR
000 0000 0000 0000 0000 0000 0000 1111 1111 1010
Hash Value 1
000 0000 0010 0000 1100 1010 0111 1111 1110 0110
28-bits
11-bits
Primary PTEG Address:
Start at PTE0
0
HTABORG
39 40
45 46
56 57
63
0000 1111 0000 0101 1000 0100 0000 0000 0000 1111 0011 1111 1111 0011 0000 0000
0 F 0 5 8 4 0 0 0 F 3 F F 3 0 0

VA to PA cont. (Secondary Hash fun.)



VA to PA cont. (PTE)

- Page Table Entry Format



- Page Table Entry Search

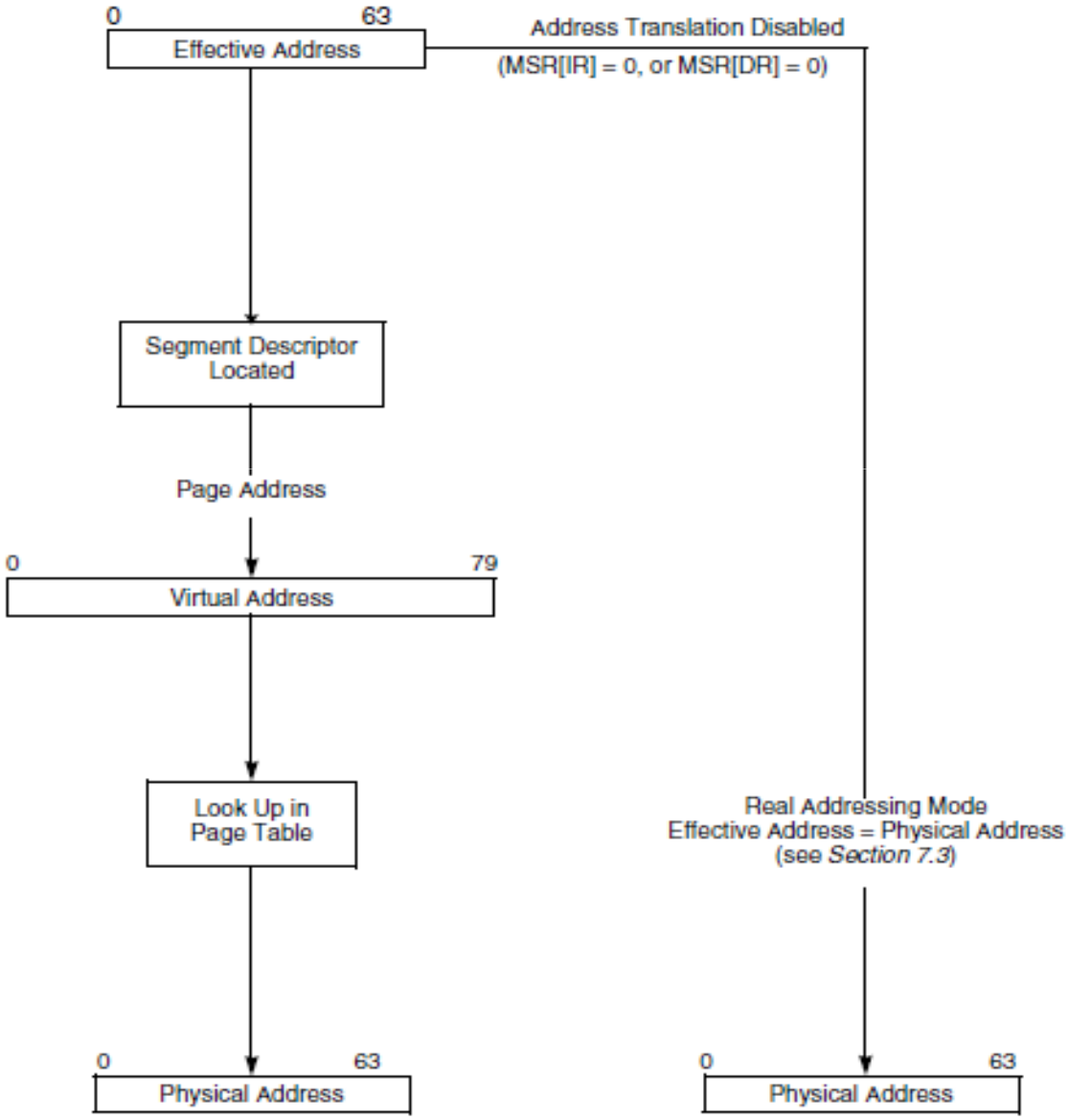
  PTE[H] = 0 for primary PTEG; PTE[H] = 1 for secondary PTEG

  PTE[V] = 1

  PTE[VSID] = VA[0-51]

  PTE[API] = VA[52-56]

Summary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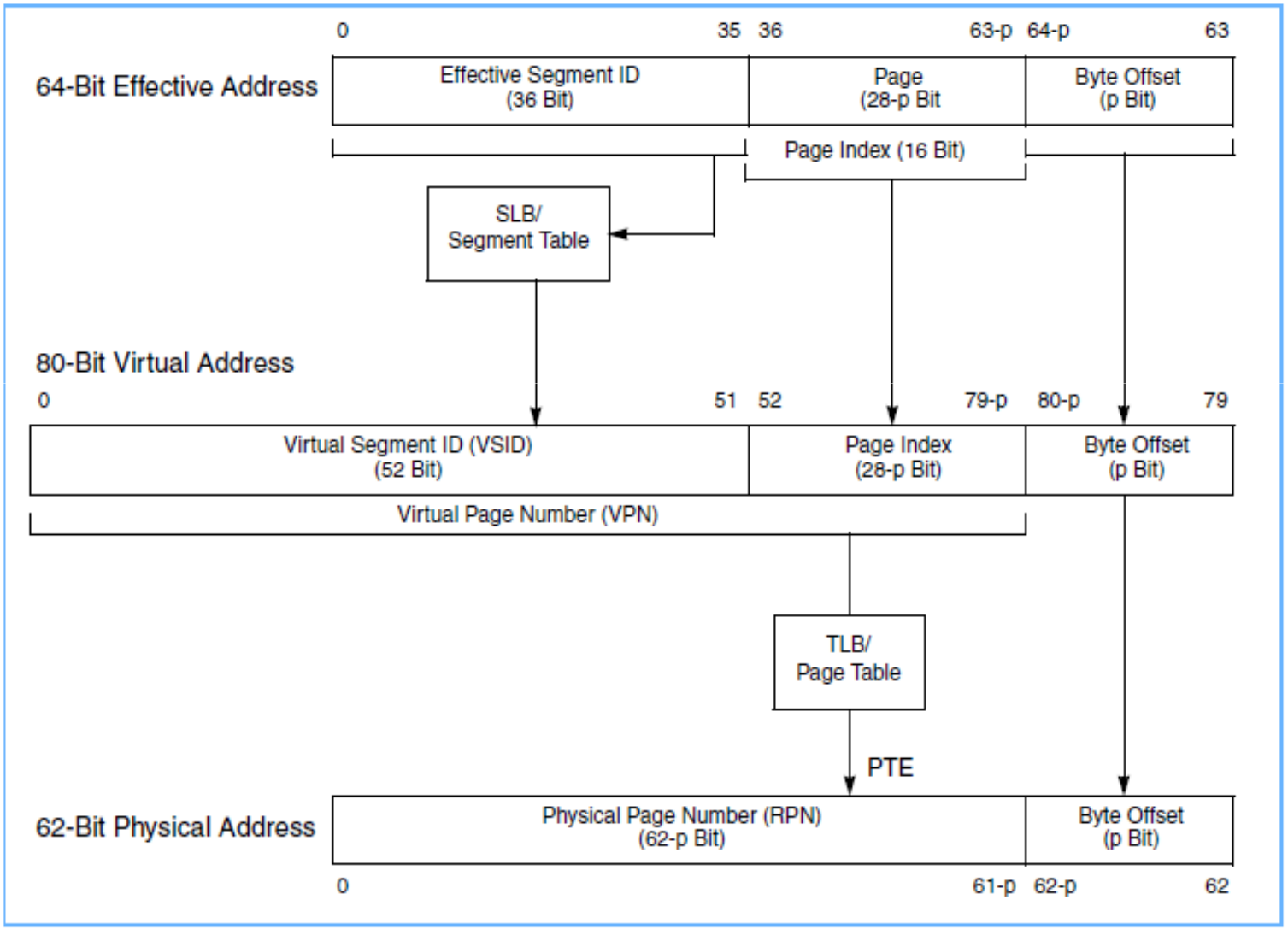
63
Effective Address
Address Translation Disabled
(MSR[IR] = 0, or MSR[DR] = 0)
Segment Descriptor Located
Page Address
0
79
Virtual Address
Look Up in Page Table
0
63
Physical Address
Real Addressing Mode
Effective Address = Physical Address
(see Section 7.3)
0
63
Physical Address

Summary


0
35
36
63-p
64-p
63
64-Bit Effective Address
Effective Segment ID
(36 Bit)
Page
(28-p Bit
Byte Offset
(p Bit)
Page Index (16 Bit)
SLB/
Segment Table
80-Bit Virtual Address
0
51
52
79-p
80-p
79
Virtual Segment ID (VSID)
(52 Bit)
Page Index
(28-p Bit)
Byte Offset
(p Bit)
Virtual Page Number (VPN)
TLB/
Page Table
PTE
62-Bit Physical Address
Physical Page Number (RPN)
(62-p Bit)
Byte Offset
(p Bit)
0
61-p
62-p
62

Reference

- “Programming Environments Manual for 64-Bit Microprocessors” Chapter 7.

Thanks!