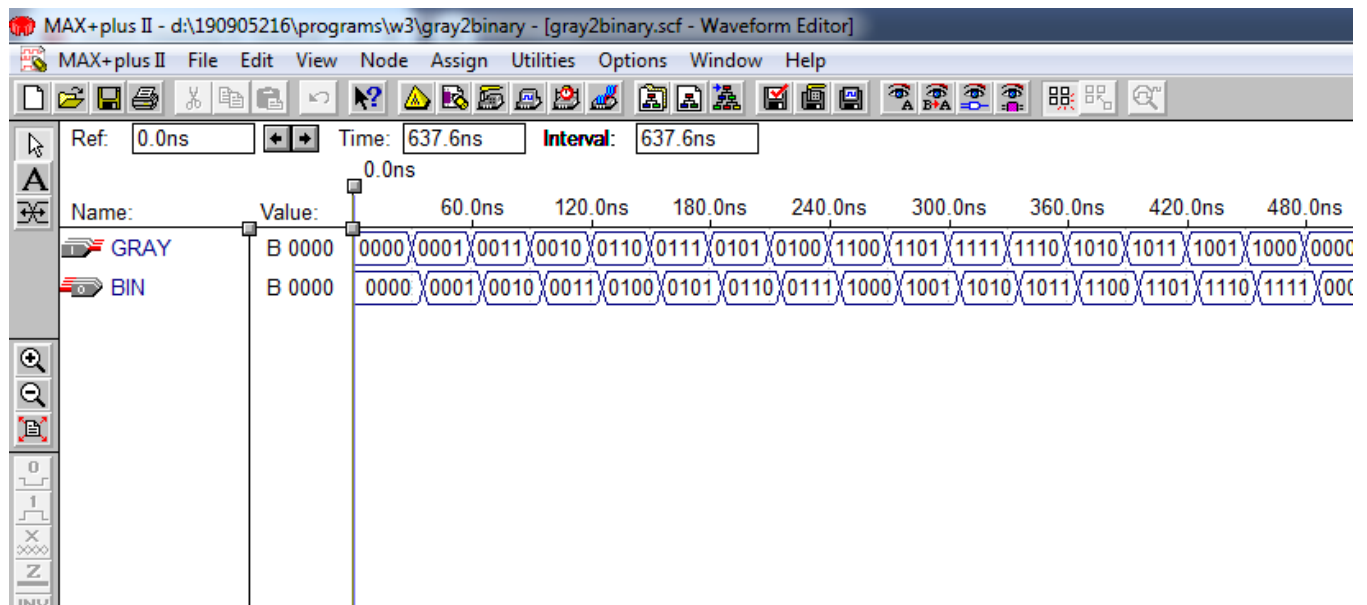


Week 3:

Q1. Gray Code to Binary Code

```
module gray2binary(GRAY, BIN);  
  
    parameter n=4;  
  
    input[n-1:0] GRAY;  
  
    output [n-1:0] BIN;  
  
    reg [n-1:0] BIN;  
  
    integer k;  
  
    always @(GRAY)  
  
        begin BIN[n-1] = GRAY[n-1];  
  
        for(k = n-2; k >= 0; k = k-1)  
  
            BIN[k] = BIN[k+1]^GRAY[k];  
  
        end  
  
endmodule
```

Waveform:

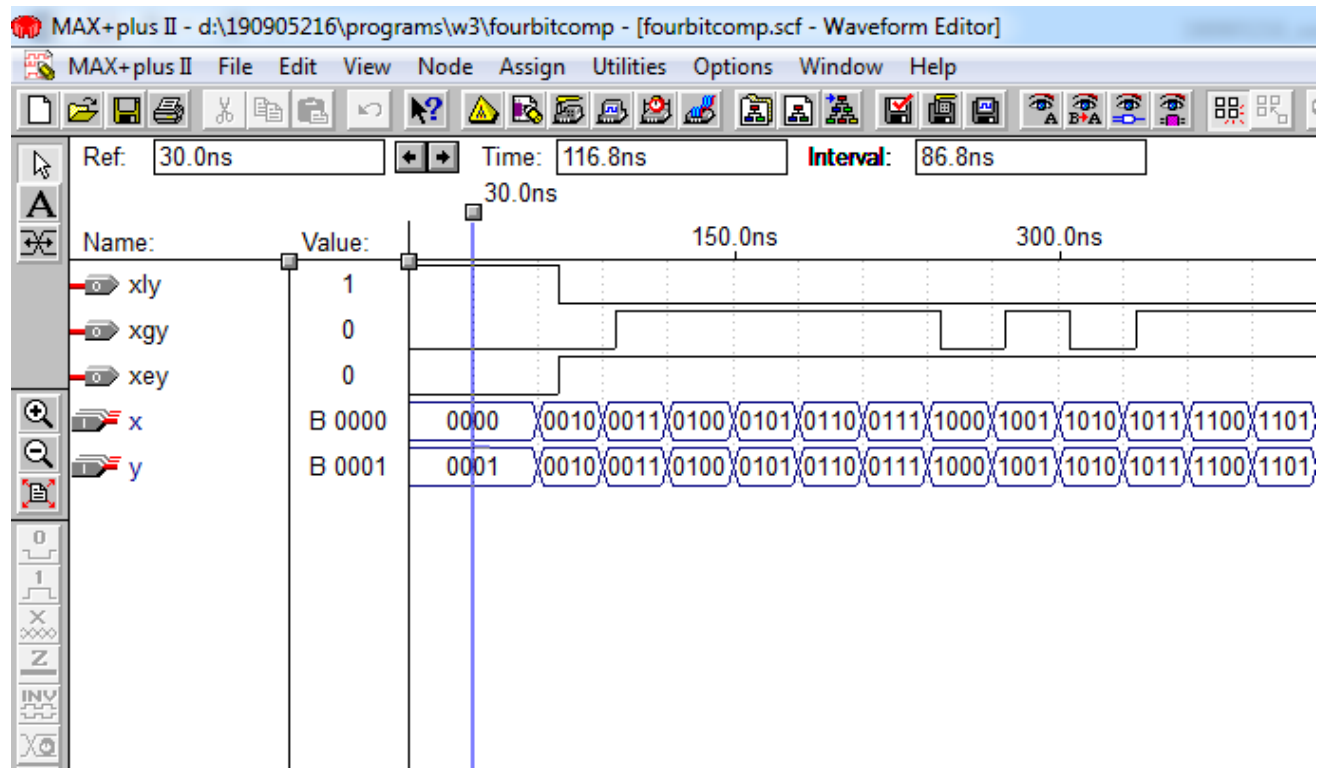


Q2: 4 bit comparator using 2 bit comparator

```
module fourbitcomp(x,y,xly,xgy,xey);  
input [3:0] x,y;  
output xly,xgy,xey;  
wire l1,l2,g1,g2,e1,e2;  
twobitcomp stage0(x[0],y[0],x[1],y[1],l1,g1,e1);  
twobitcomp stage1(x[2],y[2],x[3],y[3],l2,g2,e2);  
assign xey = e1 & e2;  
assign xgy = g2 | (e2&g1);  
assign xly = l2 | (e2&l1);  
endmodule
```

```
module twobitcomp(x0,y0,x1,y1,l,g,e);  
input x0,y0,x1,y1;  
output l,g,e;  
wire i,j;  
assign j = ~(x1^y1);  
assign i = ~(x0^y0);  
assign e = i&j;  
assign g = (x1&~y1) | (j&x0&y0);  
assign l = ~(g | e);  
endmodule
```

Waveform for 4-bit comparator:



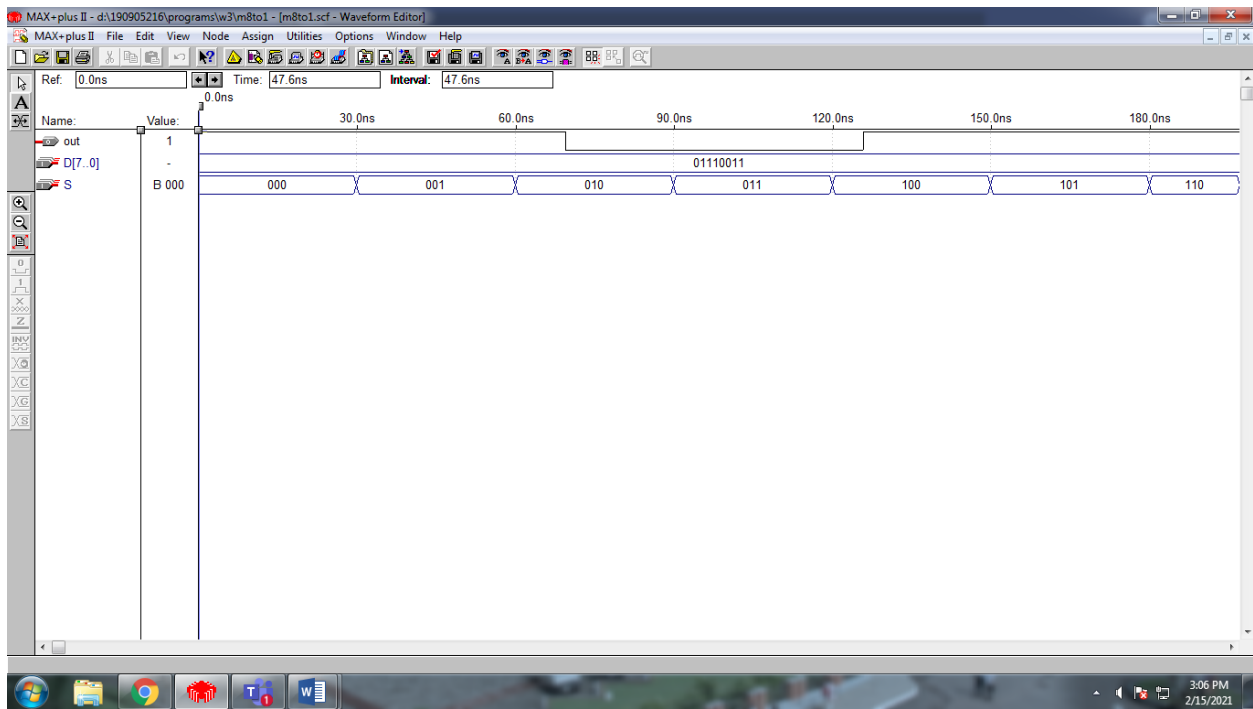
PTO->

Q3: Part 1

8 to 1 Mux:

```
module m8to1(D, S, out);  
input [7:0] D;  
input [2:0] S;  
wire [7:0] D;  
wire [2:0] S;  
output out;  
reg out;  
always@(D or S)  
begin  
case(S)  
0: out=D[0];  
1: out=D[1];  
2: out=D[2];  
3: out=D[3];  
4: out=D[4];  
5: out=D[5];  
6: out=D[6];  
7: out=D[7];  
endcase  
end  
endmodule
```

Waveform for 8 to 1 Mux:



PTO->

Q3: Part 2

2 to 1 Mux:

```
module m2to1( D0, D1, S, Y);
```

```
input D0, D1, S;
```

```
wire D0, D1;
```

```
output Y;
```

```
reg Y;
```

```
always @(D0 or D1 or S)
```

```
begin
```

```
if(S)
```

```
Y= D1;
```

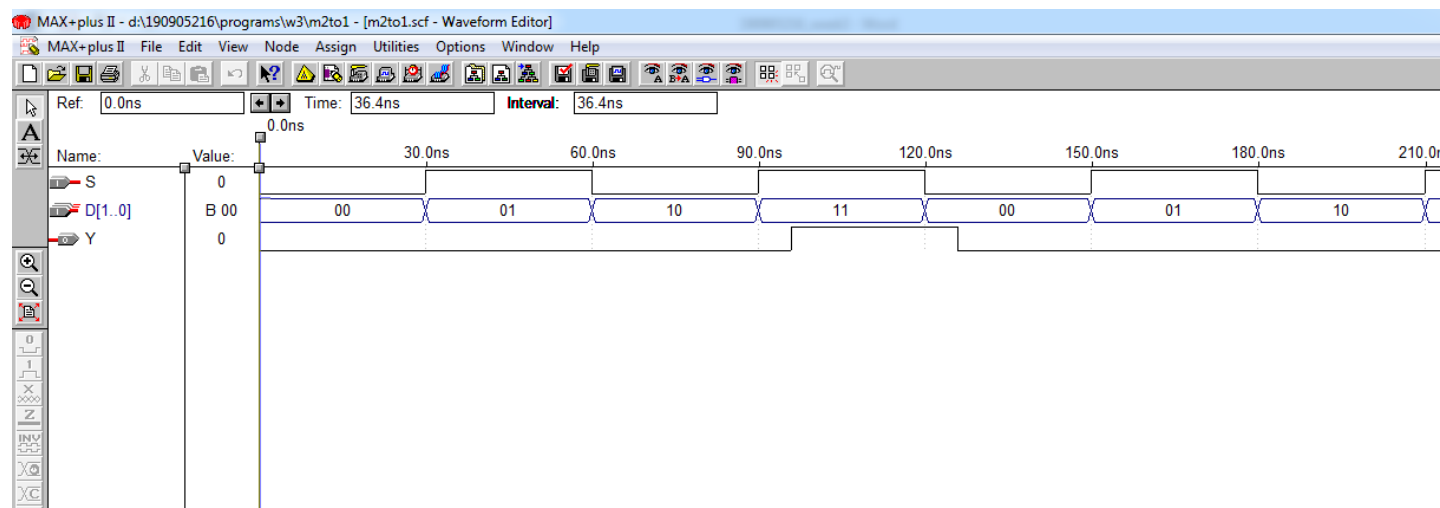
```
else
```

```
Y=D0;
```

```
end
```

```
endmodule
```

Waveform of 2 to 1 Mux:



16 to 1 Mux:

```
module m161(out, D, S);  
input [15:0] D;  
input [3:0] S;  
output out;  
reg out;  
wire [15:0] D;  
wire [3:0] S;  
wire [1:0] x;  
m81 m1(x[0], D[7:0], S[2:0]);  
m81 m2(x[1], D[15:8], S[2:0]);  
m21 m3(out, x[0], x[1], S[3]);  
endmodule
```

```
module m21(out, D0, D1, S);  
input D0, D1, S;  
wire D0, D1;  
output out;  
reg out;  
always @(D0 or D1 or S)  
begin  
if(S)  
out= D1;  
else  
out=D0;  
end  
endmodule
```

```
module m81(out, D, S);  
input [7:0] D;  
input [2:0] S;  
wire [7:0] D;  
wire [2:0] S;  
output out;  
reg out;  
always@(D or S)  
begin  
case(S)  
0: out=D[0];  
1: out=D[1];  
2: out=D[2];  
3: out=D[3];  
4: out=D[4];  
5: out=D[5];  
6: out=D[6];  
7: out=D[7];  
endcase  
end  
endmodule
```


Waveform for a 16 to 1 Mux

