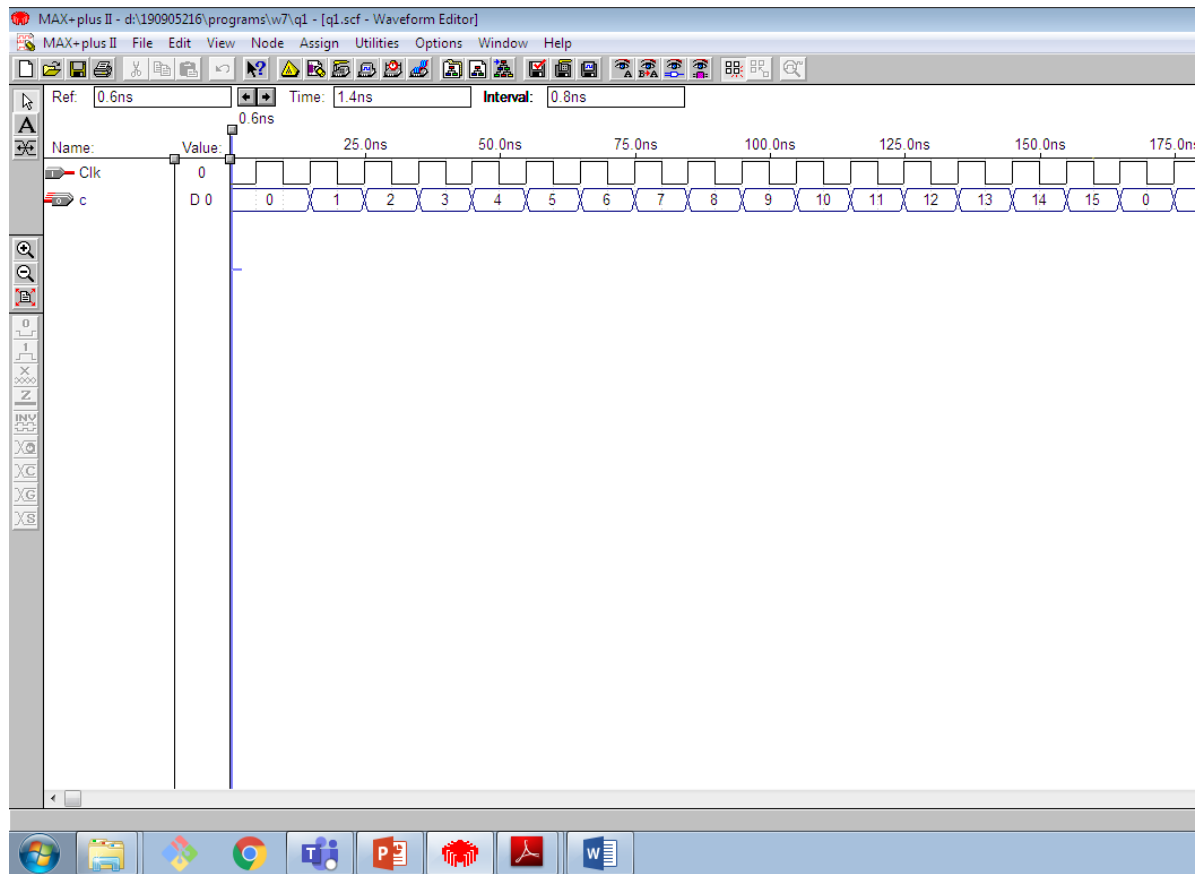


## 190905216\_Week7

**Q1:**

```
module tf(Q, T, Clk);  
input T, Clk;  
output Q;  
reg Q;  
always @ (negedge Clk)  
begin  
if(!T)  
Q <= Q;  
else  
Q <= ~Q;  
end  
endmodule
```

```
module q1(Clk, c);  
input Clk;  
output [3:0] c;  
tf stage0 (1, Clk, c[0]);  
tf stage1 (1 && c[0], Clk, c[1]);  
tf stage2 (1 && c[0] && c[1], Clk, c[2]);  
tf stage3 (1 && c[0] && c[1] && c[2], Clk, c[3]);  
endmodule
```



Waveform for 4 bit synchronous up counter

**Q2:**

```
module tf(T, Clk, Q);  
input T, Clk;  
output Q;  
reg Q;  
always @ (negedge Clk)  
begin  
if(!T)  
Q <= Q;  
else  
Q <= ~Q;  
end  
endmodule
```

```
module q2(Clk, ctrl, c);  
input Clk, ctrl;  
output [2:0] c;  
wire a, b;  
tf stage0 (1, Clk, c[0]);  
assign a = (ctrl && c[0]) || (~ctrl && ~c[0]);  
tf stage1 (a, Clk, c[1]);  
assign b = (ctrl && c[0] && c[1]) || (~ctrl && ~c[0] && ~c[1]);  
tf stage2 (b, Clk, c[2]);  
endmodule
```

