Lab 0: DFF and Counter

Kinner Parikh

September 6, 2022

CMPEN 331 - 001

1 Code

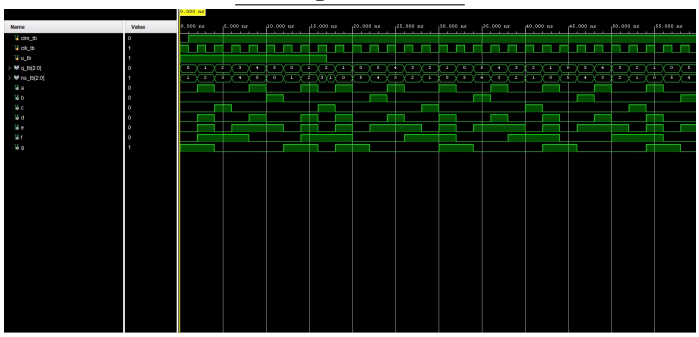
```
‘timescale 1ns / 1ps
// D-Flip Flop -> Author: provided
module dff3(input [2:0] ns, input clrn, input clk, output reg [2:0] q);
    always @ (posedge clk)
        begin
            if (clrn == 1) begin
                q <= ns;
            end
            else begin
                q <= 3’b000;
            end
        end
endmodule

// COUNTER -> Author: provided
module counter(input [2:0] q, input u, output reg [2:0] ns,
       output reg a, output reg b, output reg c, output reg d,
       output reg e, output reg f, output reg g );
   always @(*)
        begin
            if (u == 1) begin
                if (q == 3’b101) begin
                    ns <= 3’b000;
                end
                else begin
                    ns <= q + 1;
                end
            end
            else begin
                if (q == 3’b000) begin
                    ns <= 3’b101;
                end
                else begin
                    ns <= q - 1;
                end
            end
        case(q)
            3’b000: begin
                g=1’b1;  f=1’b0;  e=1’b0;  d=1’b0;
                c=1’b0;  b=1’b0;  a=1’b0;
```

```
            end
            3'b001: begin
                g=1'b1;  f=1'b1;  e=1'b1;  d=1'b1;
                c=1'b0;  b=1'b0;  a=1'b1;
            end
            3'b010: begin
                g=1'b0;  f=1'b1;  e=1'b0;  d=1'b0;
                c=1'b1   b=1'b0;  a=1'b0;
            end
            3'b011: begin
                g=1'b0;  f=1'b1;  e=1'b1;  d=1'b0;
                c=1'b0;  b=1'b0;  a=1'b0;
            end
            3'b100: begin
                g=1'b0;  f=1'b0;  e=1'b1;  d=1'b1;
                c=1'b0;  b=1'b0;  a=1'b1;
            end
            3'b101: begin
                g=1'b0;  f=1'b0;  e=1'b1;  d=1'b0;
                c=1'b0;  b=1'b1;  a=1'b0;
            end
        endcase
   end
endmodule
```

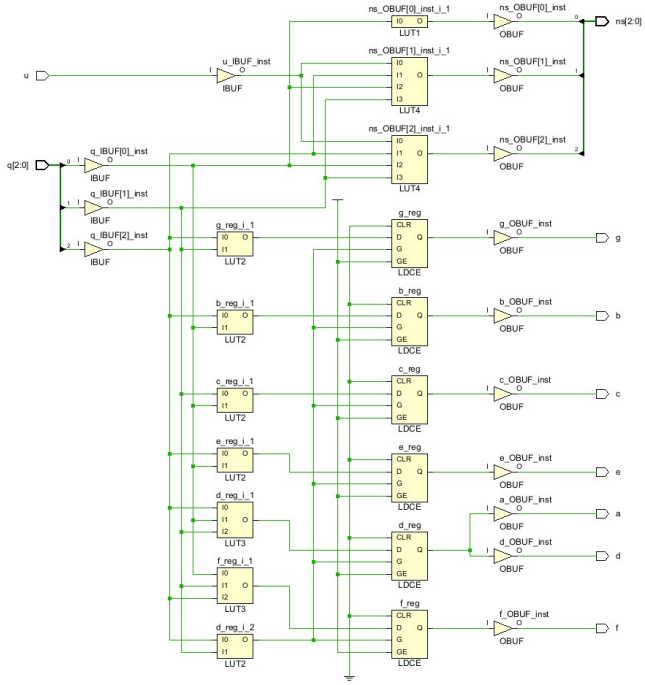
```
‘timescale 1ns / 1ps

// TESTBENCH -> Author: provided
module testbench();
    reg clrn_tb;
    reg clk_tb;
    reg u_tb;
    wire [2:0] q_tb;
    wire [2:0] ns_tb;
    wire a,b,c,d,e,f,g;
    dff3 dff3_tb(ns_tb, clrn_tb, clk_tb, q_tb);
    counter counter_tb(q_tb, u_tb, ns_tb, a, b, c, d, e, f, g);
    initial begin
        clrn_tb = 0;
        clk_tb = 1;
        u_tb = 1;
        #1 clrn_tb = 1;
        #16 u_tb = 0;
    end
    always begin
        #1;
        clk_tb = ~clk_tb;
    end
endmodule
```

2 Images

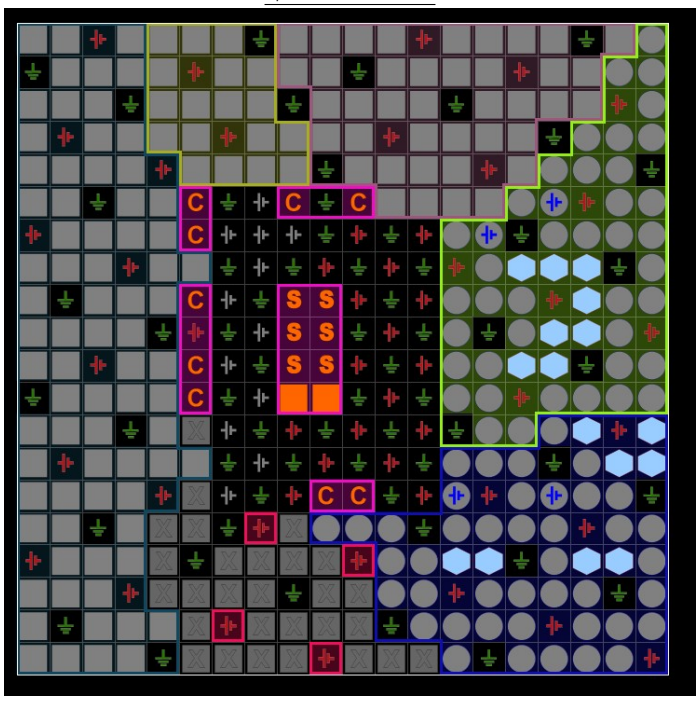
Timing Waveform



Schematic



I/O Planning



Floor Planning