

# Introduction to System-on-Chip

COE838/EE8221 Systems-on-Chip Design  
<http://www.ee.ryerson.ca/~courses/COE838/>

**Dr. Gul N. Khan**

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**Electrical and Computer Engineering**  
**Ryerson University**

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## Overview

- Course Management
- Introduction to SoC
- SoC Applications
- On-Chip Interconnections
- Bus-based and NoC based SoC Interconnects

Introductory Articles on SoC available at the course webpage

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# COE838/EE8221: Systems-on-Chip Design

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**Consultation Hours: Thursday 12:15-2:15PM or by Appointment**

**Department of Electrical and Computer Engineering  
Ryerson University**

# Lectures, Labs and Projects

## Half Notes

- Students need to take notes and also require text-reference books and some research articles identified by the instructor.

## Labs and Project

- Aimed at concept reinforcement and practical experience.

**Lectures, Labs, Projects and other support material will be available at the course website:**

<http://www.ee.ryerson.ca/~courses/coe838/>

## Assessment and Evaluation

Labs: 15%

Project: 15%

Midterm Exam: 25% (Thursday: February 13, 2020  
during lecture hours in TRS3149)

Final Exam: 45%

# Course Text/Reference Books and other Material

## Text and Other Books

1. M. Wolf, **Computer as Components: Principles of Embedded Computing System Design**, 3rd or 4th edition Morgan Kaufmann-Elsevier Publishers 2012, 2016 ISBN 978-0-12-388436-7, ISBN 97801280538741.
2. Michael J. Flynn, Wayne Luk, **Computer System Design: System on Chip**, John Wiley and Sons Inc. 2011, ISBN 978-0-470-64336-5
3. **SystemC: From the Ground Up**, 2nd Edition, D.C. Black, J Donovan, B. Bunton, A. Keist, Springer 2010, ISBN 978-0-387-69958-5.
4. **On-Chip Communication Architectures, System on Chip Interconnect**, S. Pasricha and N. Dutt, Morgan Kaufmann-Elsevier Publishers 2008, ISBN 978-0-12-373892-9.
5. **Embedded Core Design with FPGAs**, Z. Navabi, McGraw-Hill 2007, ISBN 978-0-07-147481-8 ISBN 0-07-147481-1.

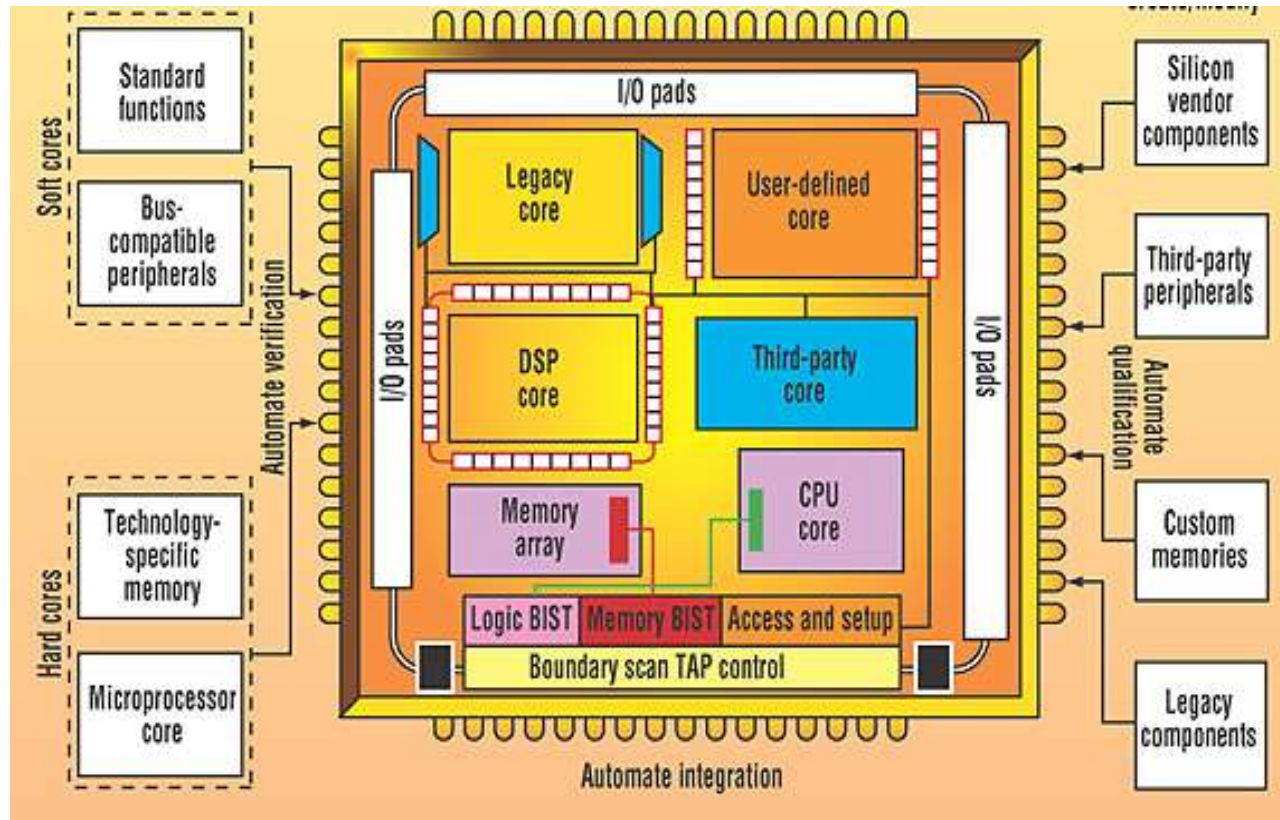
*Some Articles, Embedded Processors and other Data Sheets* are available at the Course Website: <http://www.ee.ryerson.ca/~courses/coe838/>

# Main Lecture Topics

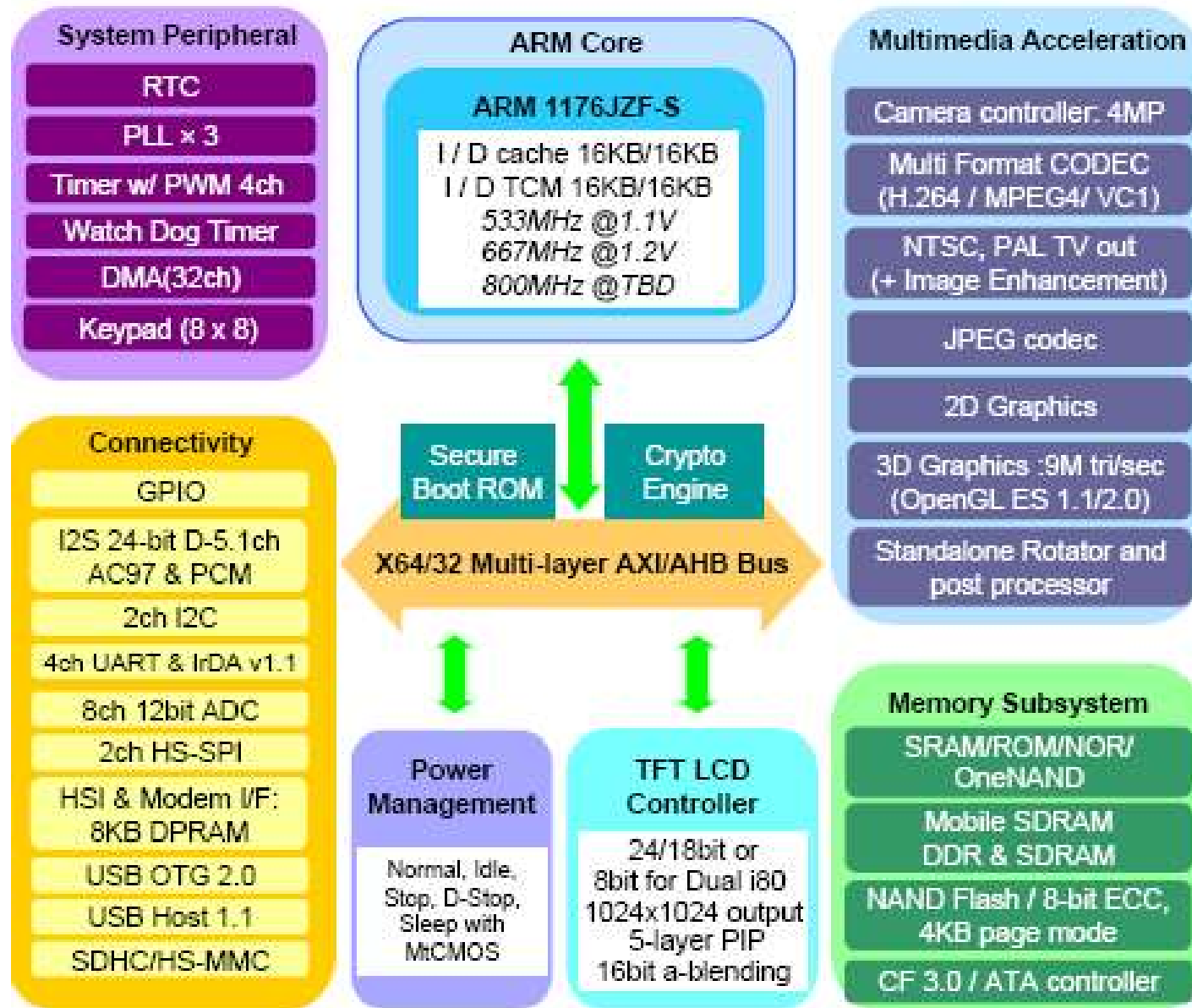
1. Introduction to System on Chip (SoC)
  - \* An SoC Design Approach
2. SystemC and SoC Design:
  - \* Co-Specification, System Partitioning, Co-simulation, and Co-synthesis
  - \* SystemC for Co-specification and Co-simulation
3. Hardware-Software Co-Synthesis, Accelerators based SoC Design
4. Basics of Chips and SoC ICs:
  - \* Cycle Time, Die Area-and-Cost, Power,
  - \* Area-time-Power Tradeoffs and Chip Reliability
5. System-on-Chip and SoPC (System on Programmable Chips)
6. SoC CPU/IP Cores
  - \* ARM Cortex A9, NIOS-II, OpenRISC, Leon4 and OpenSPARC
7. SoC Interconnection Structures: Bus-based Interconnection
  - \* AMBA Bus, IBM Core Connect, Avalon, Interconnection Structures
8. Network on Chip - NoC Interconnection and NoC Systems
9. Multi-core and MPSoC Architectures
10. SoC Application Case Studies (time permitting)

# System on a Chip

- An IC that integrates multiple components of a system onto a single chip.
- MPSoC addresses performance requirements.



# Samsung S3C6410 Platform



# S3C6410 System-on-Chip

- A 16/32-bit RISC low power, high performance micro-processor
- Applications include mobile phones, Portable Navigation Devices and other general applications.
- Provide optimized H/W performance for the 2.5G and 3G communication services,
- Includes many powerful hardware accelerators for motion video processing, display control and scaling. An
- Integrated Multi Format Codec (MFC) supports encoding and decoding of MPEG4/H.263, H.264.
- Many hardware peripherals such as camera interface, TFT 24-bit LCD controller, power management, etc.



# S3C6410 based Mobile Processor

Navigation  
System

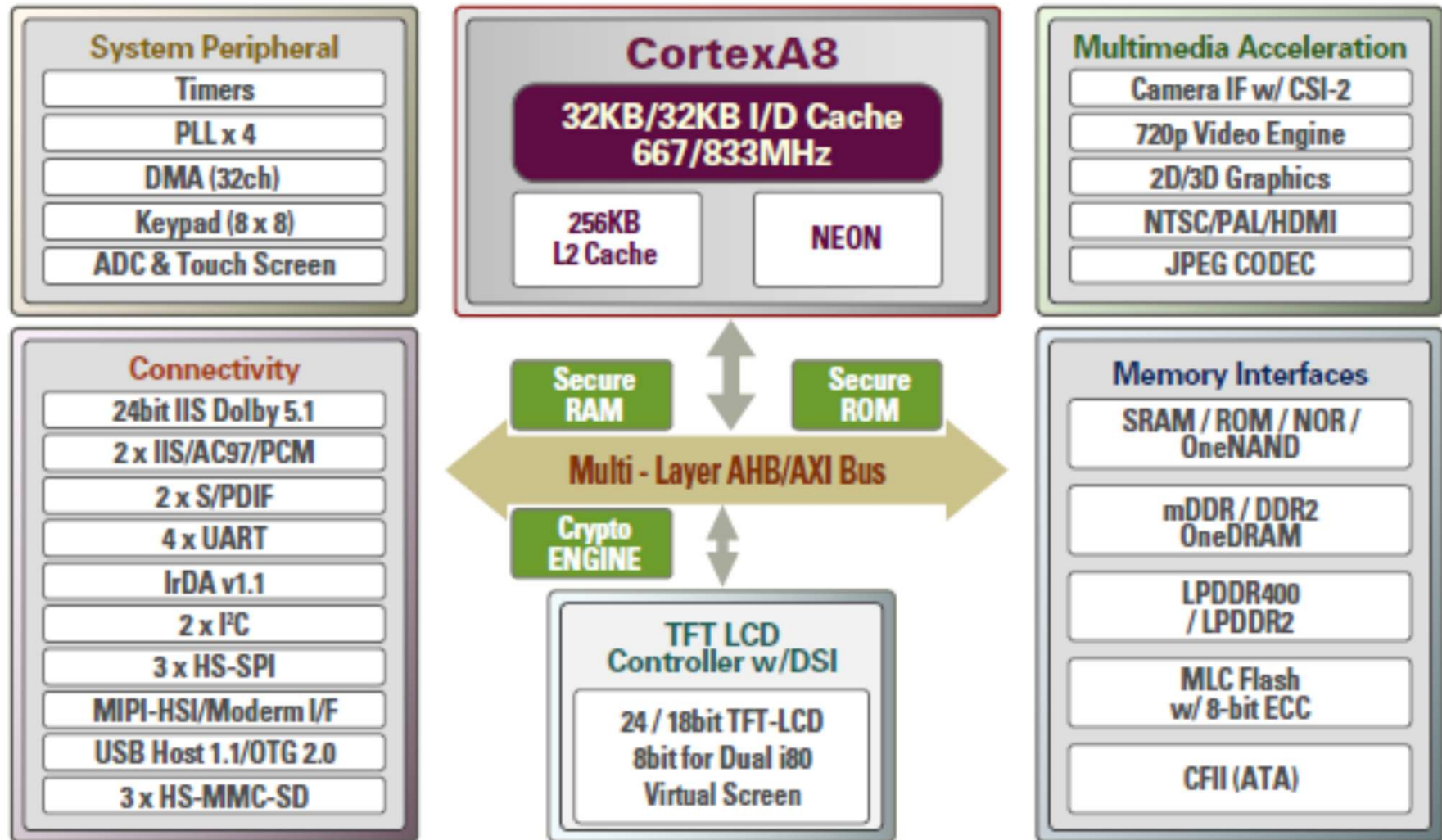


iPhone based  
on  
ARM1176JZ  
S3C6410



# Samsung S5PC100 SoC

## used in iPhone 3GS



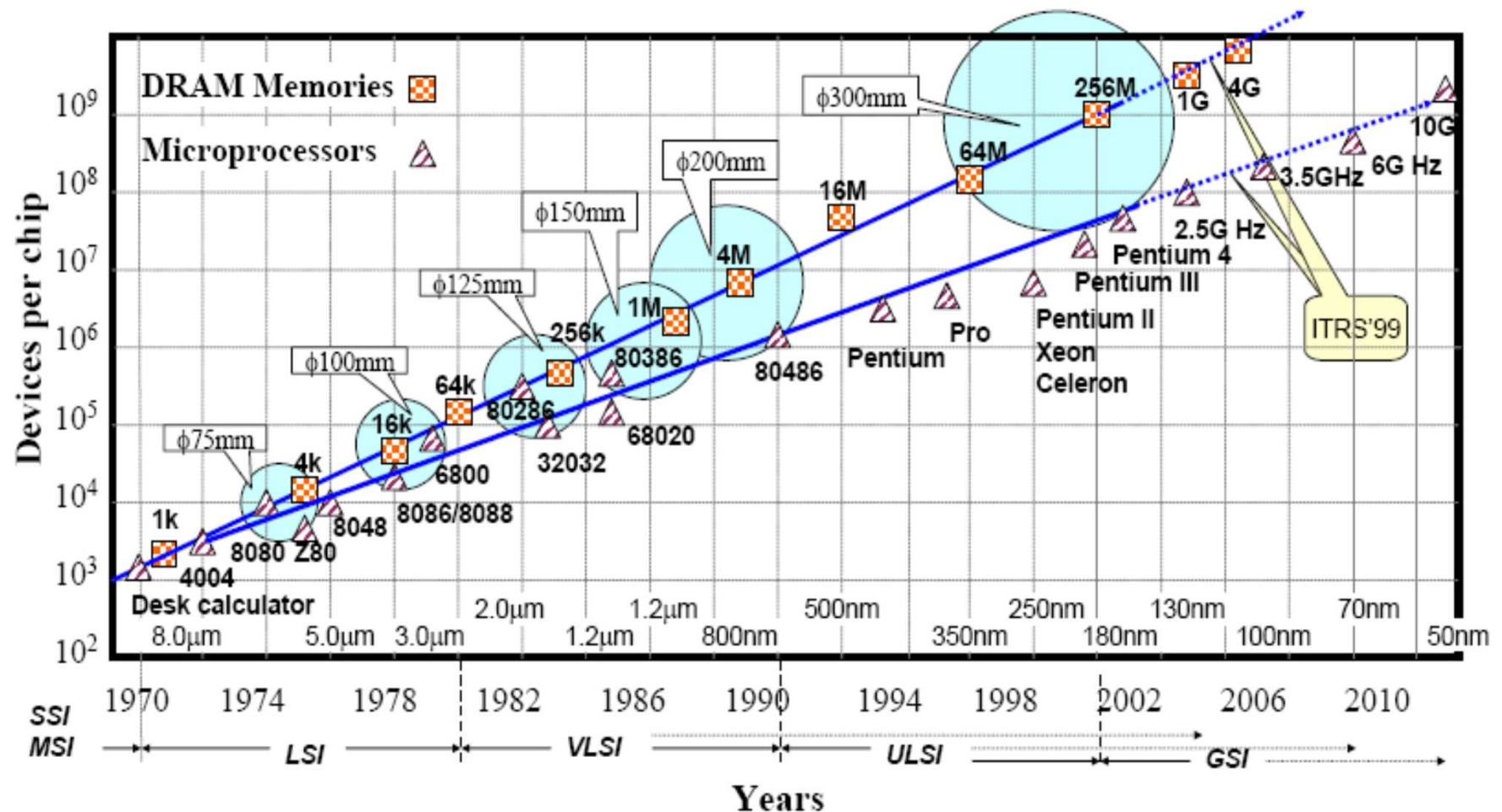
# S5PC100 Samsung SoC

S5PC100 has various functionalities:

- Wireless communication, Personal navigation, Camera
- Portable gaming, Video player and Mobile TV into one device.
- S5PC100 has a 32-bit ARM Cortex A8 RISC microprocessor that operates up to 833MHz.
- 64/32-bit internal bus architecture
- Used in iPhone 3GS and iPod touch 3<sup>rd</sup> generation.



# Moore's Law



...the performance of an IC, including the number components on it, doubles every 18-24 months with the same chip price ... - Moore - 1960



# Technology Past Roadmap

Year of Technology Node	1999	2002	2005	2008	2011	2014
Technology	180nm	130nm	100nm	70nm	50nm	35nm
DRAM /introduction	1G	2~4G	8G	-	64G	-
Transistors/chip ( $\mu$ P) ( <i>M</i> )	110	220~441	882	2,494	7,053	19,949
Chip size ( $\mu$ P) ( <i>mm</i> <sup>2</sup> )	450	450~567	622	713	817	937
Number of signal I/O ( $\mu$ P)	768	1,024	1,024	1,280	1,408	1,472
Power/Ground I/O ( $\mu$ P)	1,536	2,018	2,018	2,560	2,816	2,944
On-chip local clock (MHz) (high performance)	1,250	2,100	3,500	6,000	10,000	13,500
On-chip across-chip clock (MHz) (high performance)	1,200	1,600	2,000	2,500	3,000	3,600
Off-chip speed (MHz) (high perf., peripheral buses)	480	885	1,035	1,285	1,540	1,800
Power (W) H.P./H.H.	90/1.4	130/2.0	160/2.4	170/2.0	174/2.2	183/2.4
Power supply (V) H.P./H.H.	1.8/1.5	1.5/1.2	1.2/0.9	0.9/0.6	0.6/0.5	0.6/0.3
Metal levels # ( $\mu$ P/SoC)	7/6	8/7	9/8	9/9	10/10	10/10

H.P: High performance  $\mu$ P - MicroProcessor

H.H: Hand Held Devices

# Evolution: Boards to SoC

## **Evolution:**

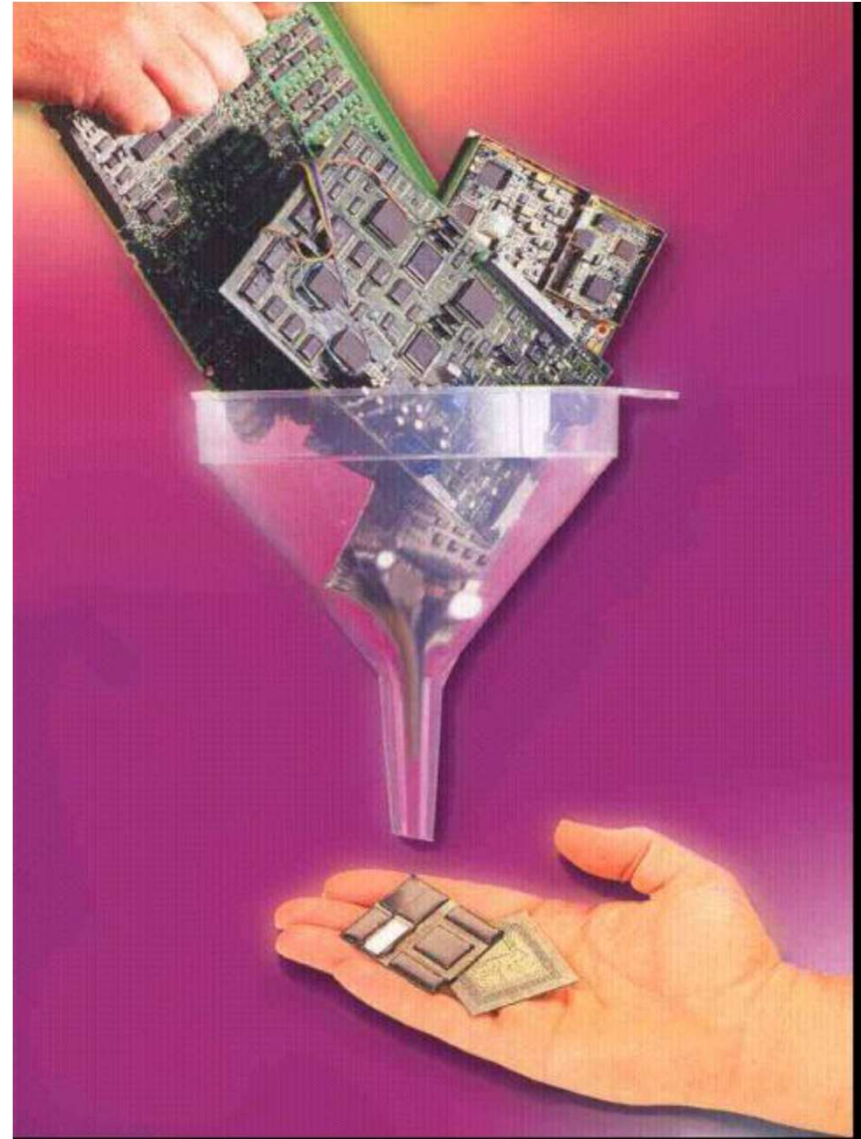
- IP based design
- Platform-based design

## **Some Challenges**

- HW/SW Co-design
- Integration of analog (RF) IPs
- Mixed Design
- Productivity

## **Emerging new technologies**

- Greater complexity
- Increased performance
- Higher density
- Lower power dissipation



# What is System-on-Chip

SoC: More of a System not a Chip

- \* In addition to IC, SoC consists of software and interconnection structure for integration.

SoC may consists of all or some of the following:

- Processor/CPU cores
- On-chip interconnection (busses, network, etc.)
- Analog circuits
- Accelerators or application specific hardware modules
- ASICs Logics
- Software – OS, Application, etc.
- Firmware

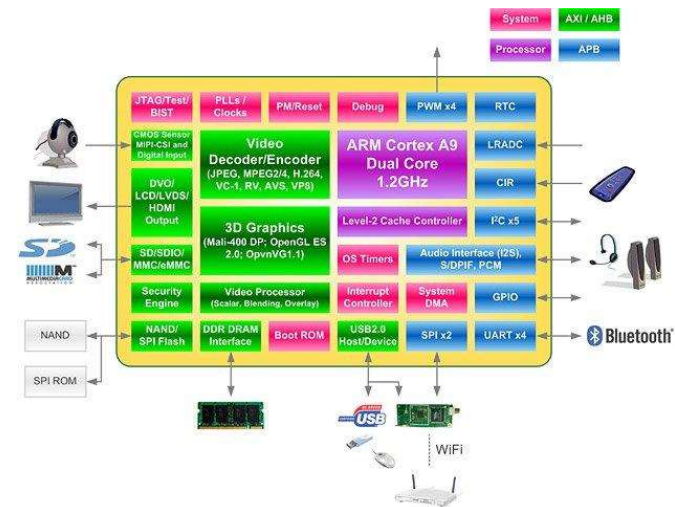
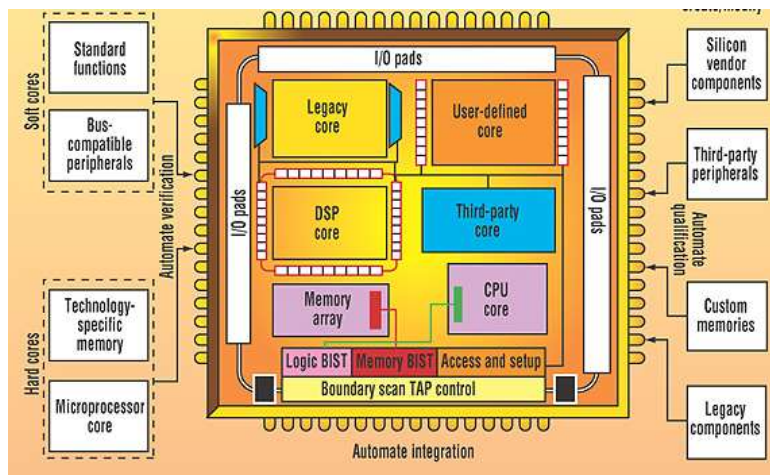
# System on a Chip

## On-Chip Components?

A processor or multiple processors

\* Including DSPs, microprocessors, microcontrollers

Cores (IPs): On-chip memory, accelerators, peripherals (i.e. USB, ETH, etc.), PLLs, power management, etc.

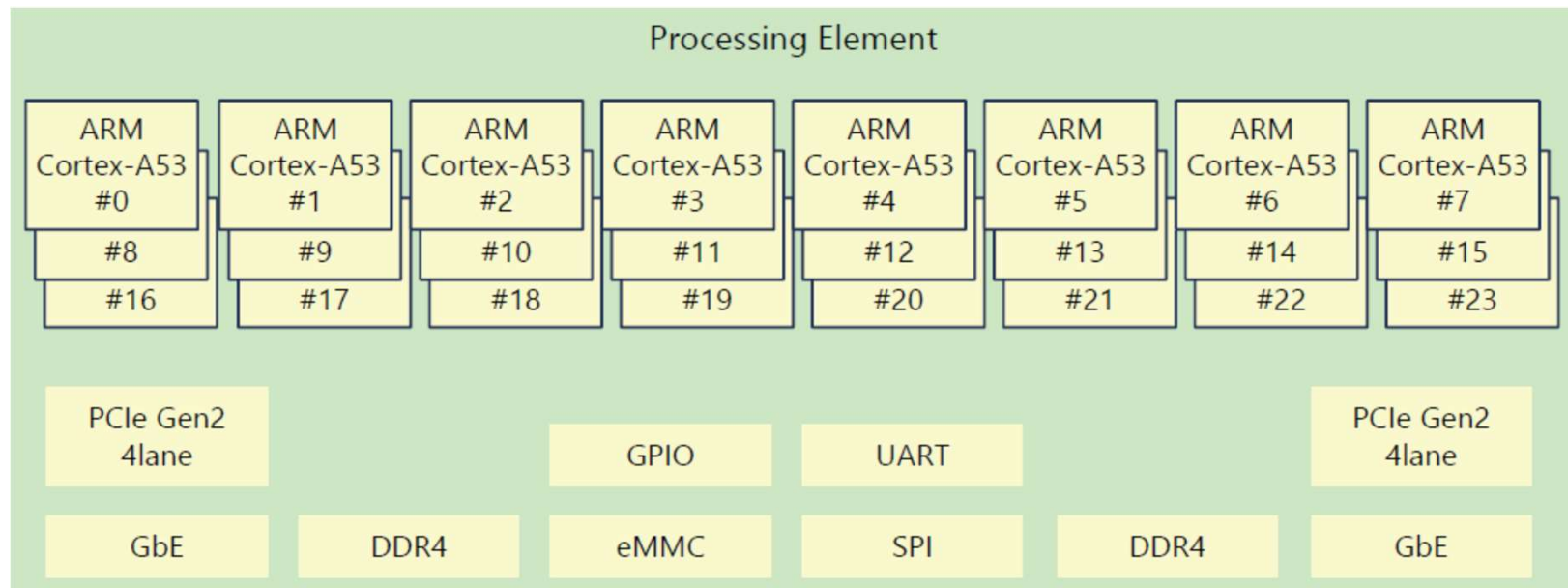




# SC2A11: Multi-core Processor

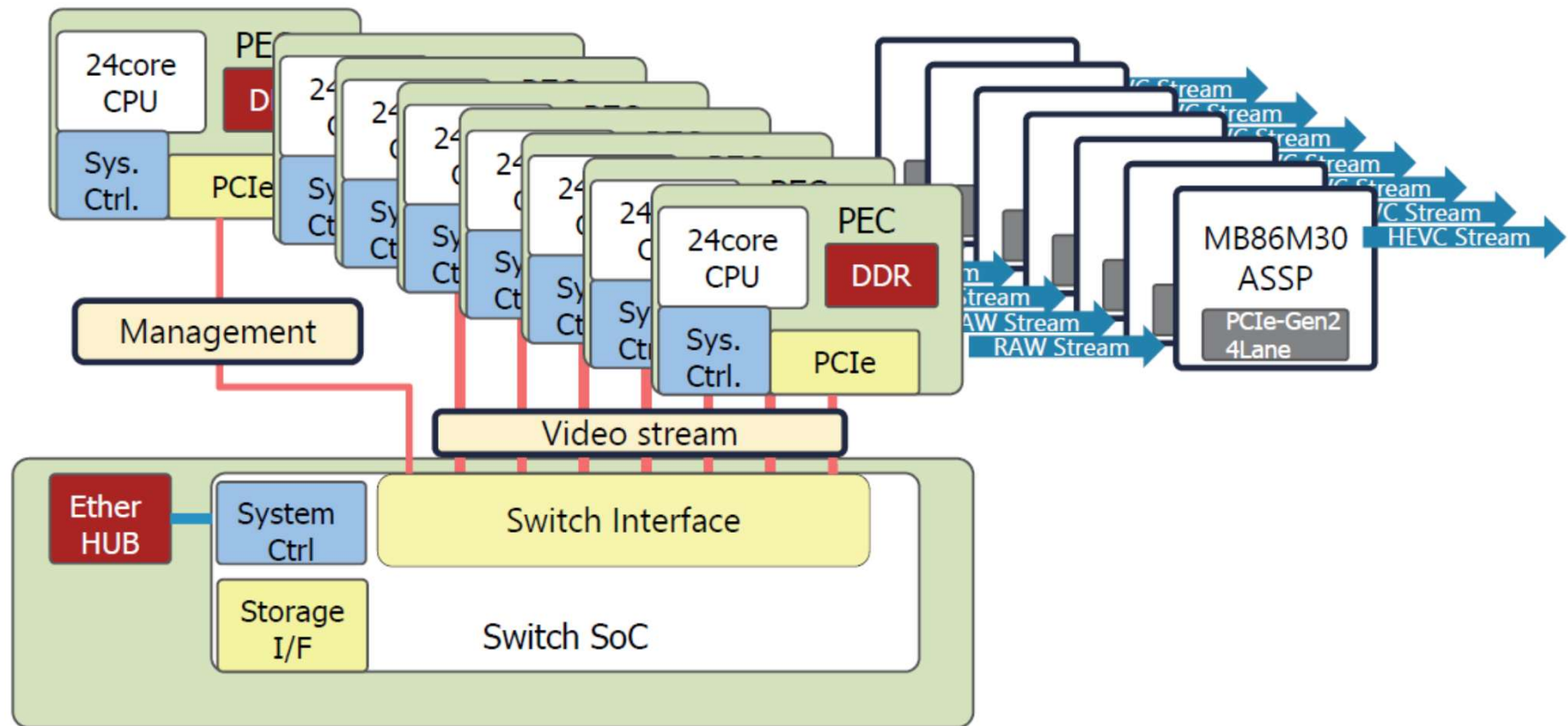
A multi-core processor SoC with 24-cores of ARM Cortex-A53.

SC2A11 suitable for low-power server systems. It can also suit to edge computing to process data at the edge of the cloud.



# SC2A11-Media Transcoder System

- High energy-efficiency processor element is realized with multi-core configuration of ARM Cortex-A53.
- Large amount of Video data can be processed faster in memory.

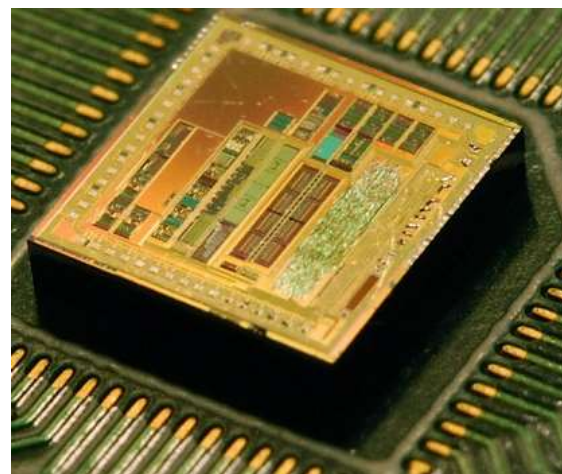
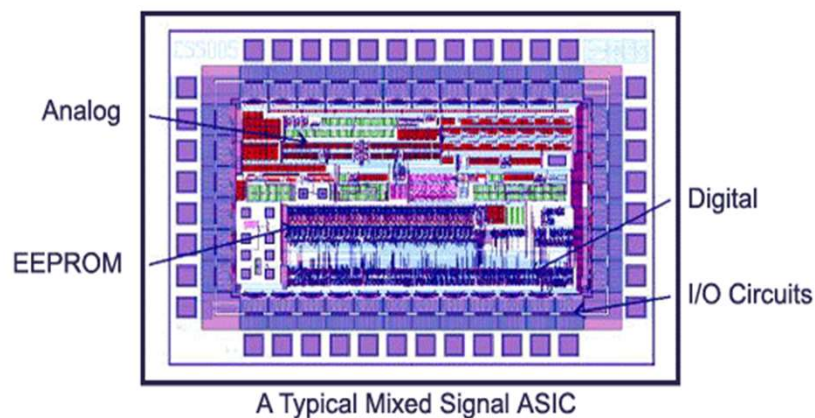


# ASIC to System-on-Chip

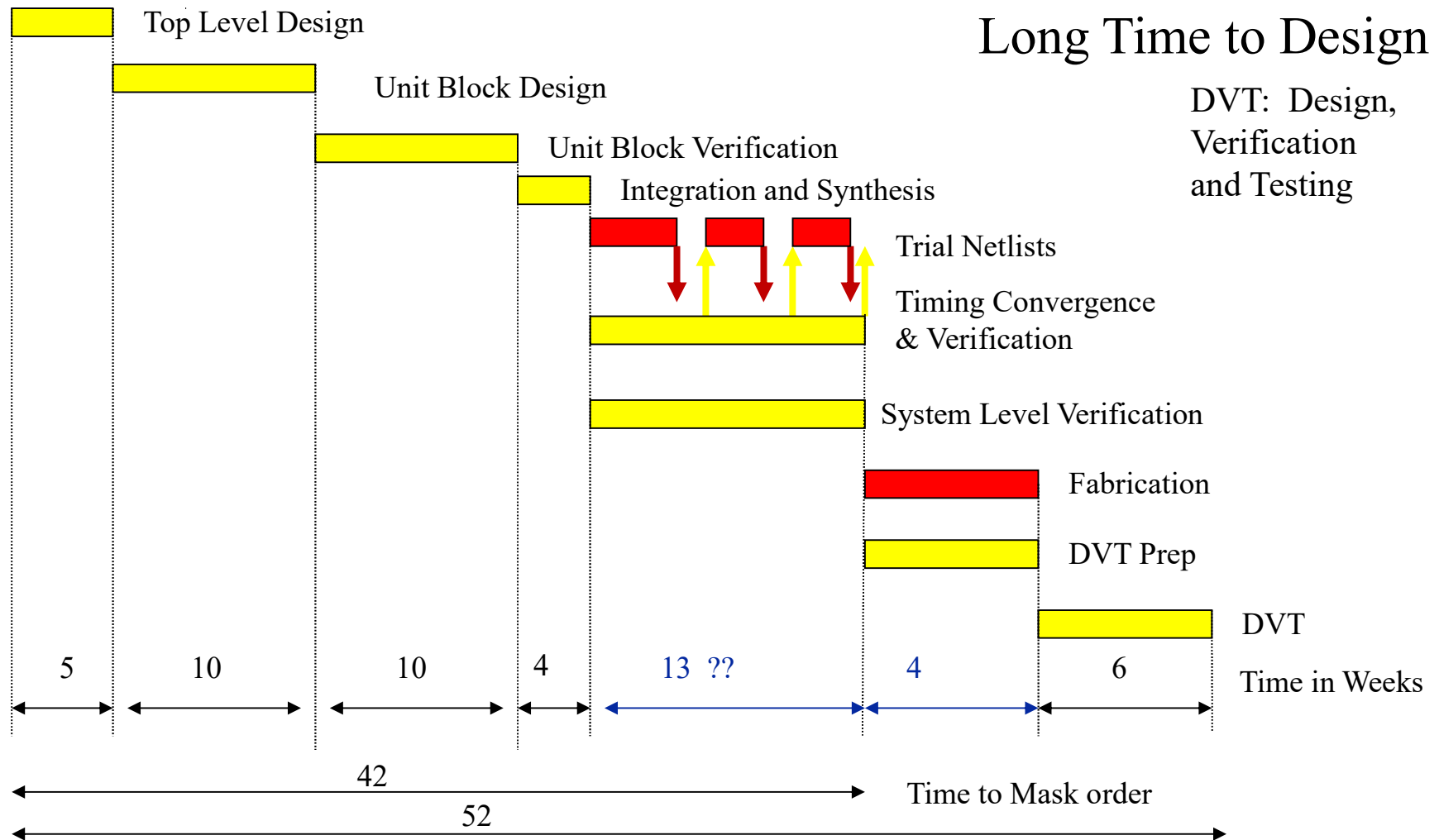
**ASICs:** Application Specific ICs are close to SoC designed to perform a specific function for embedded and other applications.

- \* ASIC vendors supply libraries for each technology they provide. Mostly, these libraries contain pre-designed/verified logic circuits.

- \* SOC is an IC designed by combining multiple stand-alone VLSI designs to provide a functional IC for an application. It composes of pre-designed models of complex functions e.g. cores (IP block, virtual components, etc.) that serve various embedded applications.



# ASIC Design Flow

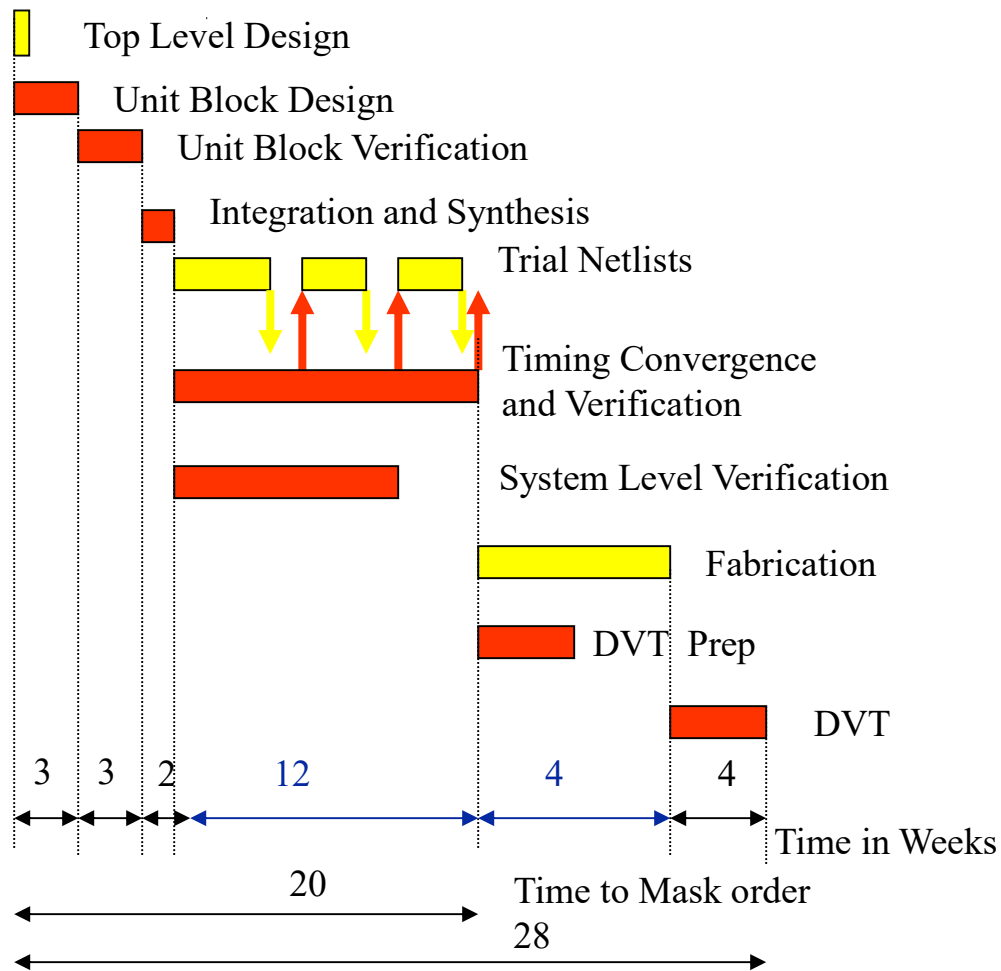


# System-on-Chip Design Flow

- Specify: What does the customer really want?
  - Architect:
    - \* Find the most cost and performance effective architecture to implement it?
    - \* Which existing components can we adapt & re-use?
  - Evaluate: What is the performance impact of a cheaper architecture?
  - Implement: What can we generate automatically from libraries and customization?
- Use separate computation, communication, etc.

# SoC Design Flow

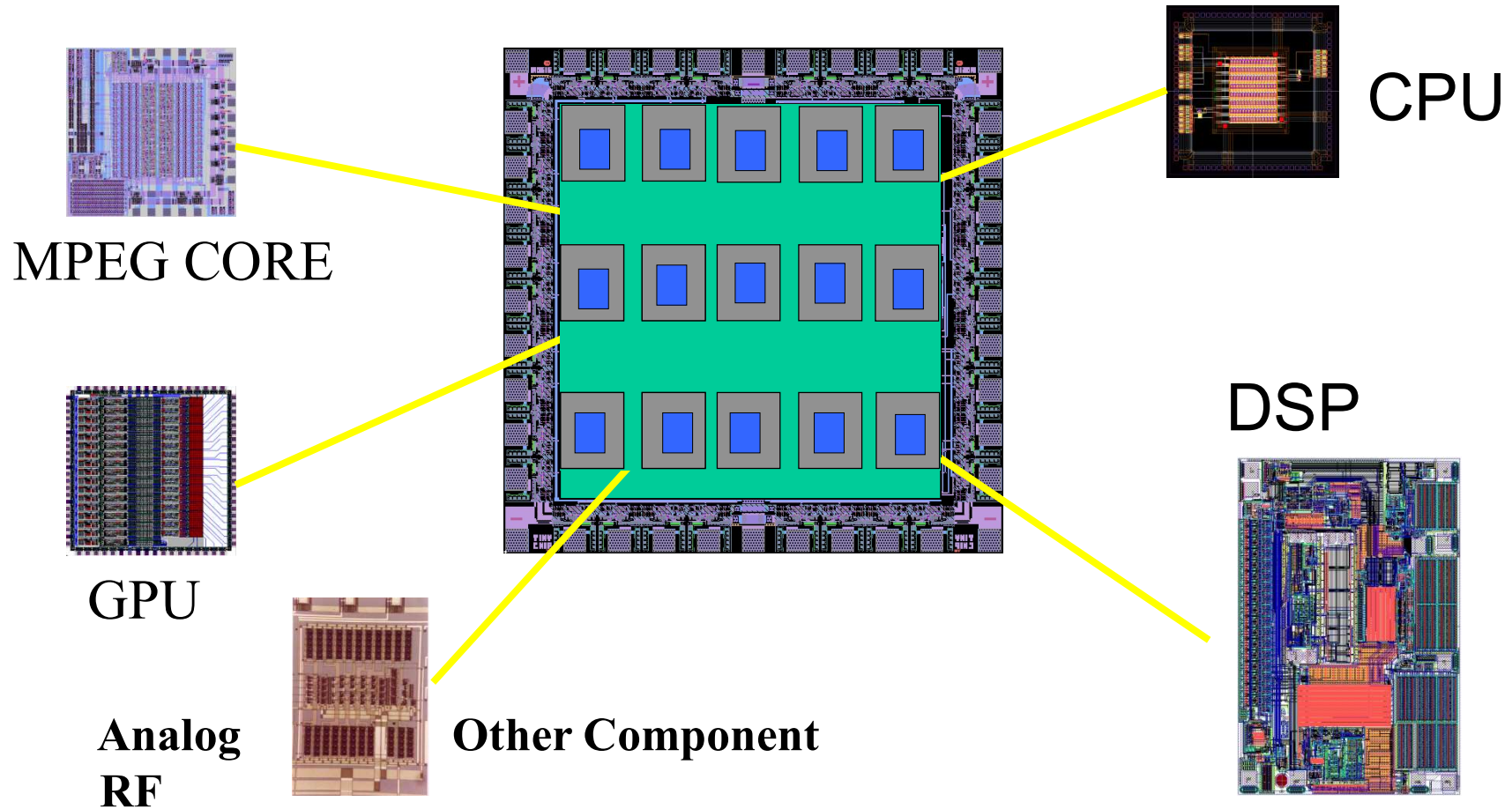
## SoC Typical Design Steps



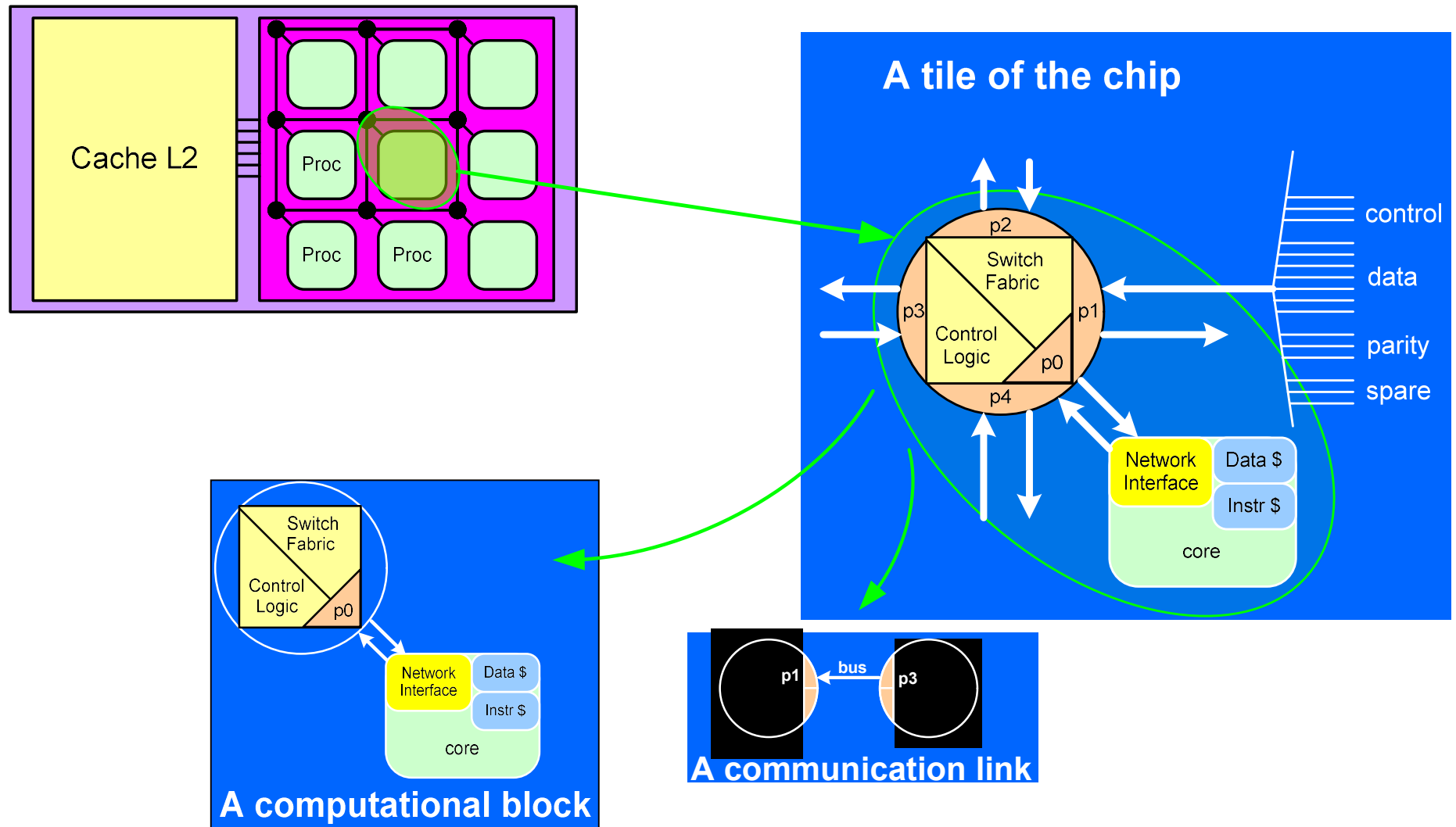
- Due to Chip Complexity and lower IC area, it is difficult to reduce **Placement, Layout** and **Fabrication** steps time.
- There is need to reduce the time of other steps before **Placement, Layout** and **Fabrication** steps.
- One should consider Chip Layout issues up-front.



# System-on-Chip



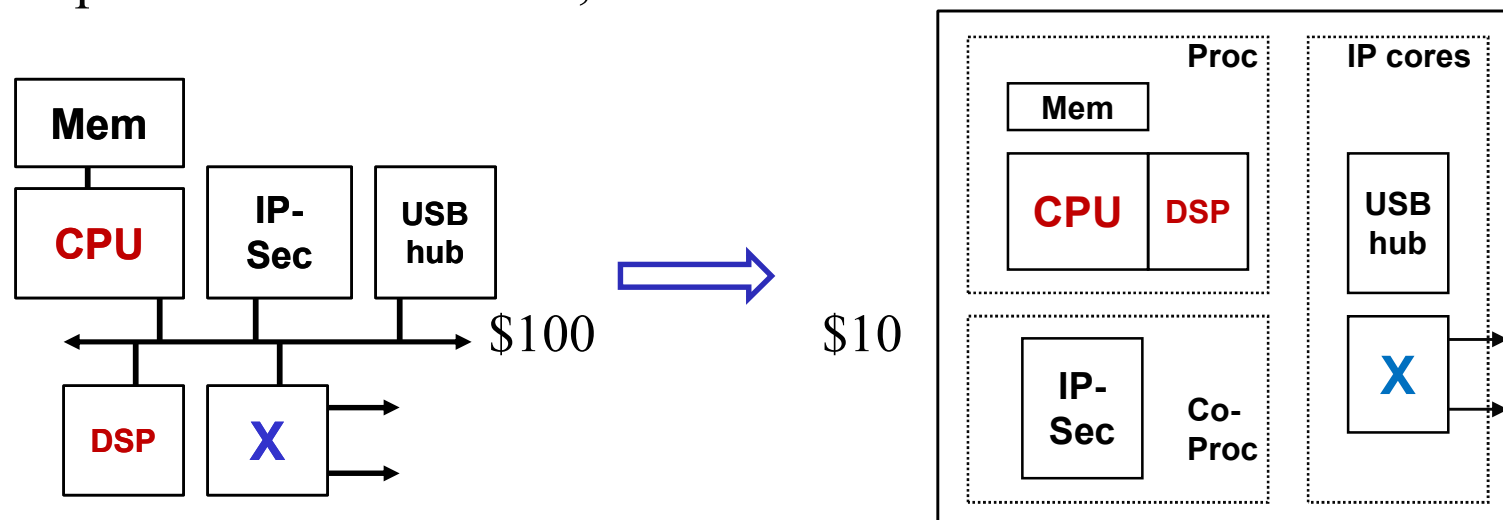
# SOC Structure





# SOC: System on Chip

- SOC cannot be considered as a large ASIC
  - Architectural approach involving significant design reuse
  - Addresses the cost and time-to-market problems
- SOC design is significantly more complex
  - Need cross-domain optimizations
  - IP reuse will increase productivity, but not enough
  - Even with extensive IP reuse, many of the ASICs design problems will remain, and more ...



# SOC Applications

- SOC Design include embedded processor cores, and a significant software component, which leads to additional design challenges.
- An SOC is a system on an IC that integrates software and hardware Intellectual Property (IP) using more than one design methodology.
- The designed system on a chip is application specific.

## Typical applications of SOC:

- Consumer devices.
- Networking and communication.
- Biomedical Devices.
- Other segments of electronics industry.

Microprocessor, Media processor,  
GPS controllers, Cellular/Smart  
phones, ASICs, HDTV, Game  
Consoles, PC-on-a-chip

# IP: Intellectual Property Cores

IP cores can be classified into three types:

**Hard IP** cores are hard layouts using physical design libraries. The integration of hard IP cores is simple and easy. However, they are technology dependent and lack flexibility.

**Soft IP** cores are generally in VHDL/Verilog code providing functional descriptions of IPs. These cores are flexible and reconfigurable. However, these soft IP cores must be synthesized and verified by the user before integrating them.

**Firm IP** cores provide the advantage of both balancing the high performance and optimization properties of hard IPs along with the flexibility of soft IPs. These cores are provided in the form of netlists to specific physical libraries after synthesis.

# Some IP Examples

Category	Intellectual Property
Processor	ARM7, ARM9, and ARM10, ARC
Application-Specific DSP	ADPCM, CELP, MPEG-2, MPEG-4, Turbo Code, Viterbi, Reed Solomon, AES
Mixed Signal	ADCs, DACs, Audio Codecs, PLLs, OpAmps, Analog MUX
I/Os	PCI, USB, 1394, 1284, E-IDE, IRDA
Miscellaneous	UARTs, DRAM Controller, Timers, Interrupt Controller, DMA Controller, SDRAM Controller, Flash Controller, Ethernet 10/100 MAC

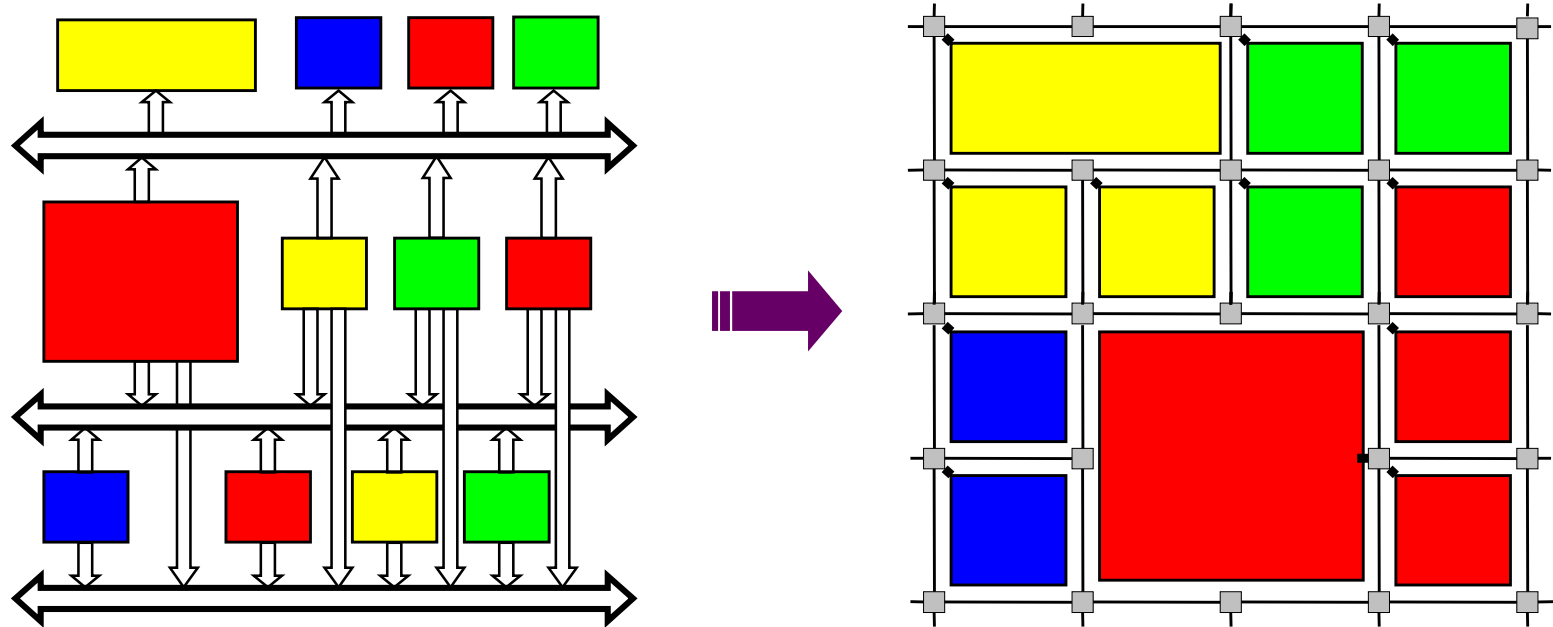
# Multi-Core (Processor) System-on-Chip

Inter-node communication between CPU/cores can be performed by message passing or shared memory.

Number of processors in the same chip-die increases at each node (CMP and MPSoC).

- **Memory sharing will require: Shared Bus**
  - \* Large Multiplexers
  - \* Cache coherence
  - \* Not Scalable
- **Message Passing: NOC: Network-on-Chip**
  - \* Scalable
  - \* Require data transfer transactions
  - \* Overhead of extra communication

# Buses to Networks



- Architectural paradigm shift: Replace wire spaghetti by network
- Usage paradigm shift: Pack everything in packets
- Organizational paradigm shift
  - Confiscate communications from logic designers
  - Create a new discipline, a new infrastructure responsibility

# MPSoC

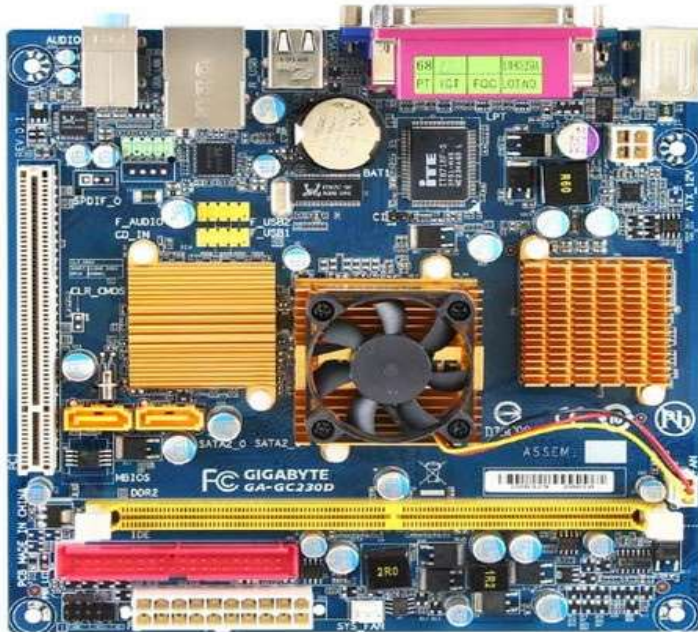
MPSoC is a system-on-chip and it contains multiple instruction-set processors (CPUs).

- A typical MPSoC is a **heterogeneous multiprocessor** where several different types of processing elements (PEs).
- The memory system may also be heterogeneously distributed around the machine, and the interconnection structure between the PEs and the memory may also be heterogeneous.
- MPSoCs often have large memory. The application device can have embedded memory on-chip, and may rely on off-chip commodity memory.

# SOC: System on Chip

Several CPUs are now actually considered as SoCs!

- CPUs now contain the CPU itself, along with integrated graphics processors, PCI express, memory controllers etc. all on a single die



PC Motherboard – CPU with support ICs

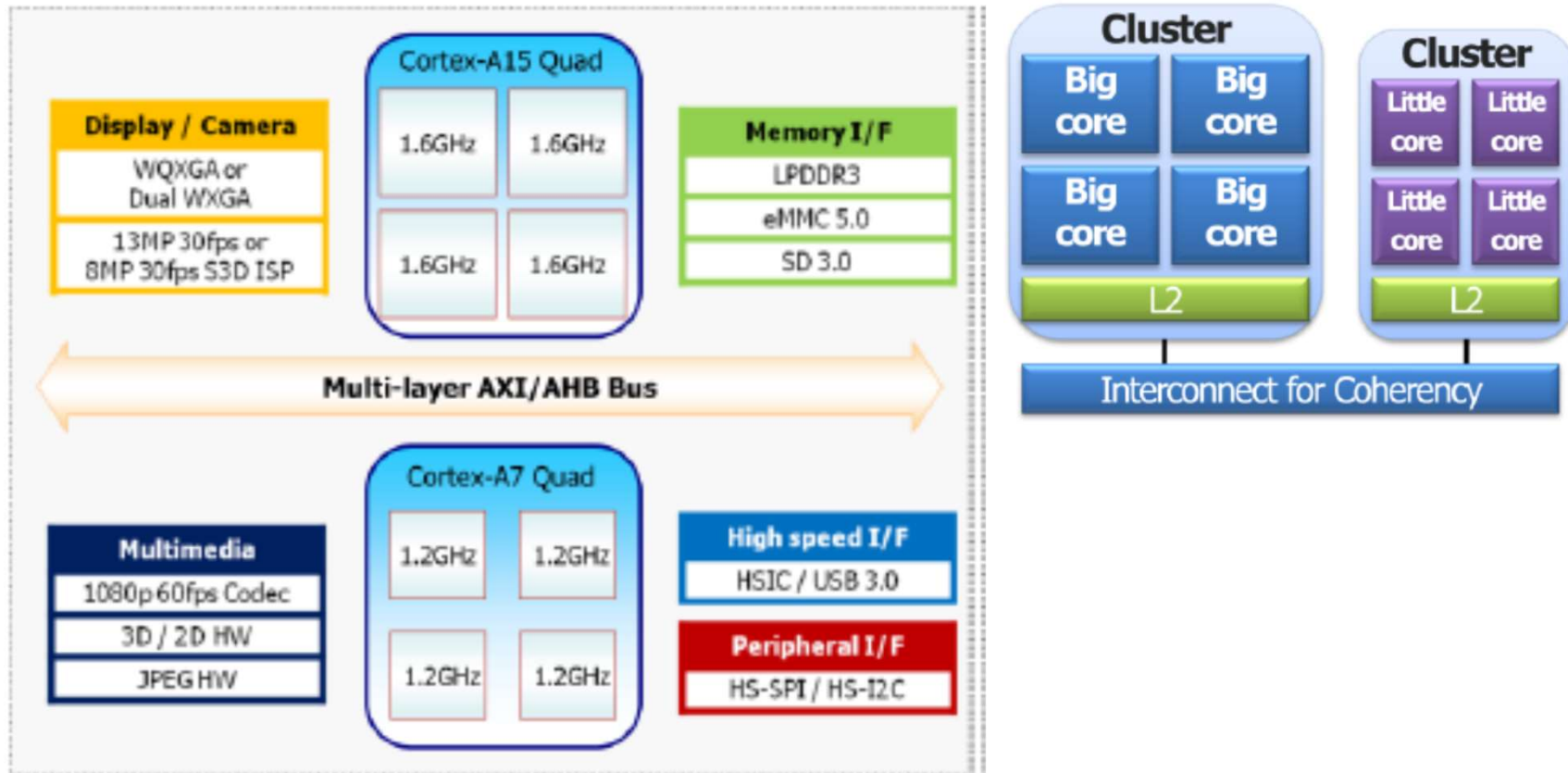
Advantages?  
Disadvantages?



ipad3's CPU SoC Circuit → A5



# Exynos 5410 Octa Processor SoC



Octa core CPU, big.LITTLE processing  
3D graphics – fast/efficient operation for smartphone/tablets.  
12.8 GB/s memory bandwidth, 1080p 60 fps video.

# Where are we heading?

- Introduction to System on Chip - An SoC Design Approach.
- SystemC for SoC Design: Co-Specification and Simulation.
- Hardware-Software Co-synthesis and Accelerator based SoCs.
- Basics of Chips and SoC ICs.
- Hardware-Software Co-synthesis and Accelerator based SoCs
- SoC CPU/IP Cores: ARM Cortex A9
- SoC Interconnection Structures: Bus-based Interconnection
- NoC: Network on Chip
- Multi-core and MPSoC (Multiprocessor SoC) Architectures
- SoC Case Studies (if time permits)