




COMPUTER SYSTEM

LAB 02

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Part 1:

Input A	Input B	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000

0101	0100	1001	
0101	0101	1010	
0101	0110	1011	
0101	0111	1100	

0101	1000	1101	
0101	1001	1110	
0101	1010	1111	
0101	1011	0000	

0101	1100	0001	
0101	1101	0010	
0101	1110	0011	
0101	1111	0011	

Part 2

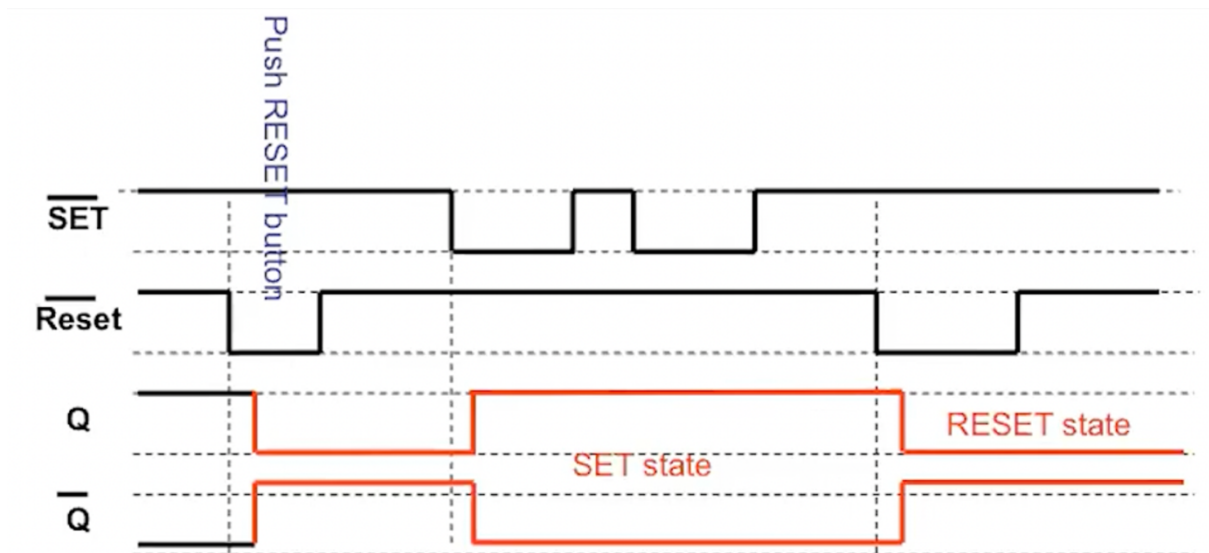
Set	Reset	Q	Q'
0	0	Unchanged	Unchanged
0	1	1	0
1	1	1	0
1	0	Indeterminate	Indeterminate

Question 11:

- One of the output will be turning off as they cannot be on or off at the same time exception from when both are 0 as they are in the illegal state.

Question 12:

- Nothing will change as this works as the lever.



Source: Online Lecture Tutorial.

Clock	Pin	Q	Q'
0	0	Unchanged	Unchanged
0	1	Unchanged	Unchanged
1	1	1	0
1	0	0	1

15.

- With only one input and a not gate to assure the complementary nature of the input, a D flip flop ensures that the input is synchronous by only permitting change when the pulse is up. The flip flop's state is preserved while the clock's pulse is absent. The input and the flip of states are identical.

16.

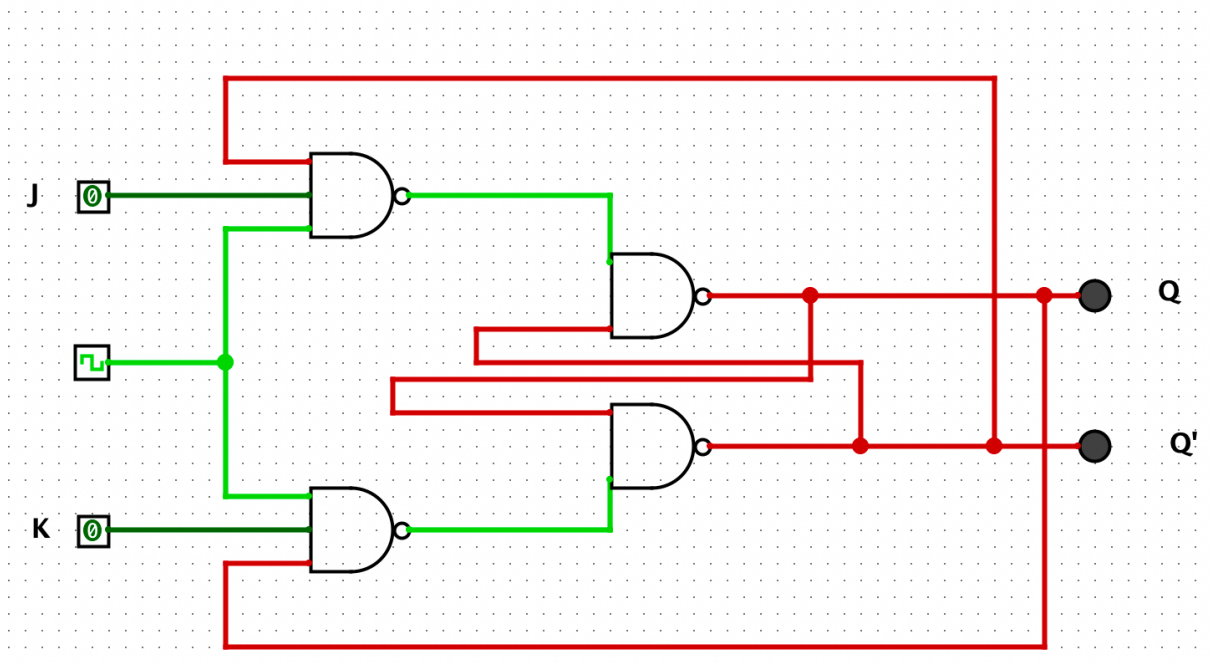
- Synchronizing the input is the clock's job. Till the clock's pulse is up, the status is not altered.

17.

- Because it has a clock to synchronise the input, the D flip flop is more stable than the RS flip flop.

Clock	Pin	Q	Q'
0	0	Unchanged	Unchanged
0	1	Unchanged	Unchanged
1	1	1	0
1	0	0	1

JK Flip Flop



J	K	Q (When Clocked)	Q' (When Clocked)
0	0	Unchanged	Unchanged
0	1	0	1
1	1	1	0
1	0	Toggle	Toggle

20.

- For J and K, we don't need to use two inputs; instead, we merely use one input, feeding it through the first two NAND gates, either of which is then supplied into the NAND gate.

21.

- When both J and K inputs are connected to a single input, the device can function as a toggle. Because the J K Flip Flop will toggle when they are both 1.