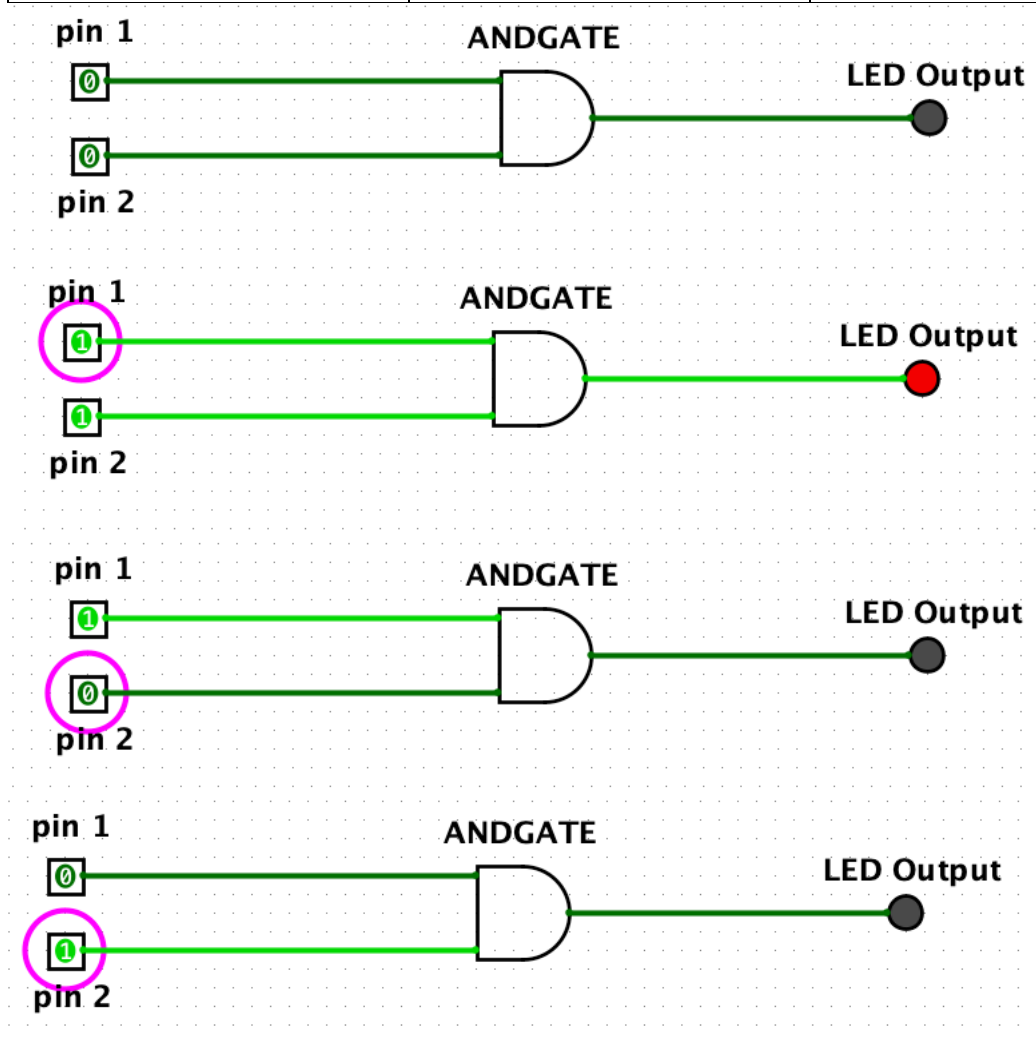COMPUTER SYSTEM

LAB 01

TRAN DUC ANH DANG

103995439
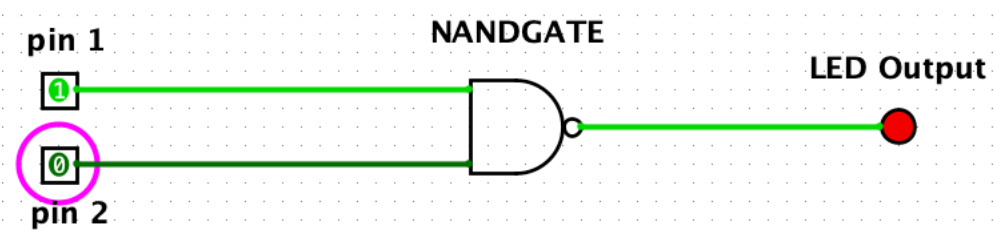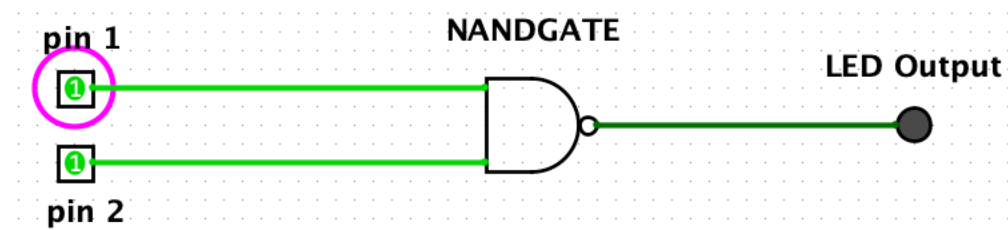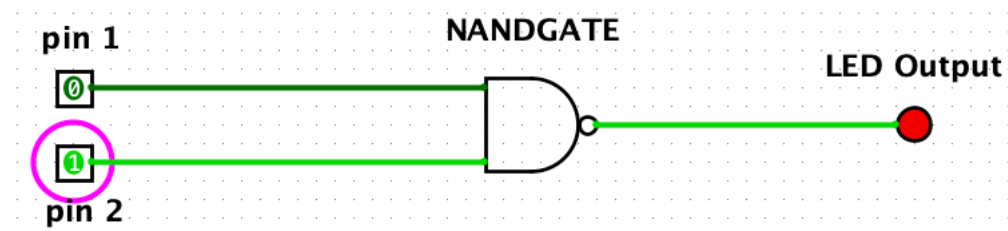
AND GATE Output Observed Results:

Pin 1	Pin 2	Output
0	0	0
0	1	0
1	1	1
1	0	0

NAND GATE Output Observed Results:

Pin 1	Pin 2	Output
0	0	1
0	1	1
1	1	0
1	0	1

pin 1

NANDGATE

LED Output

[0]

[0]

pin 2

pin 1

NANDGATE

LED Output

[0]

[1]

pin 2

pin 1

NANDGATE

LED Output

[1]

[1]

pin 2

pin 1

NANDGATE

LED Output

[1]

[0]

pin 2
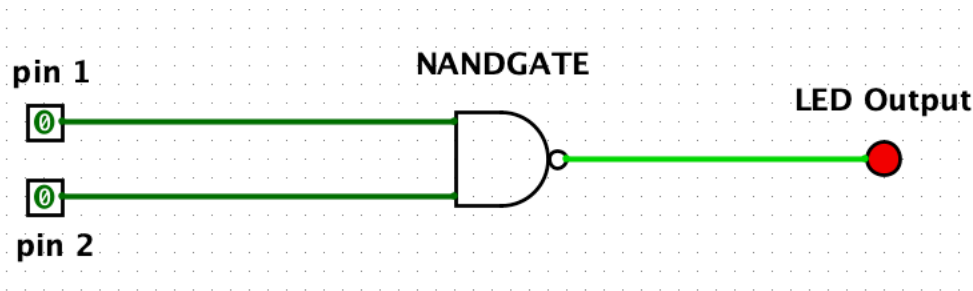
HALF-ADDER Output Observed Results:

In1	In2	Sum Output	Carry Output
0	0	0	0
0	1	1	0
1	1	0	1
1	0	1	0

HALF-ADDER

In 1

0

In 2

0

SUM Output

CARRY Output

HALF-ADDER

In 1

0

1

In 2

SUM Output
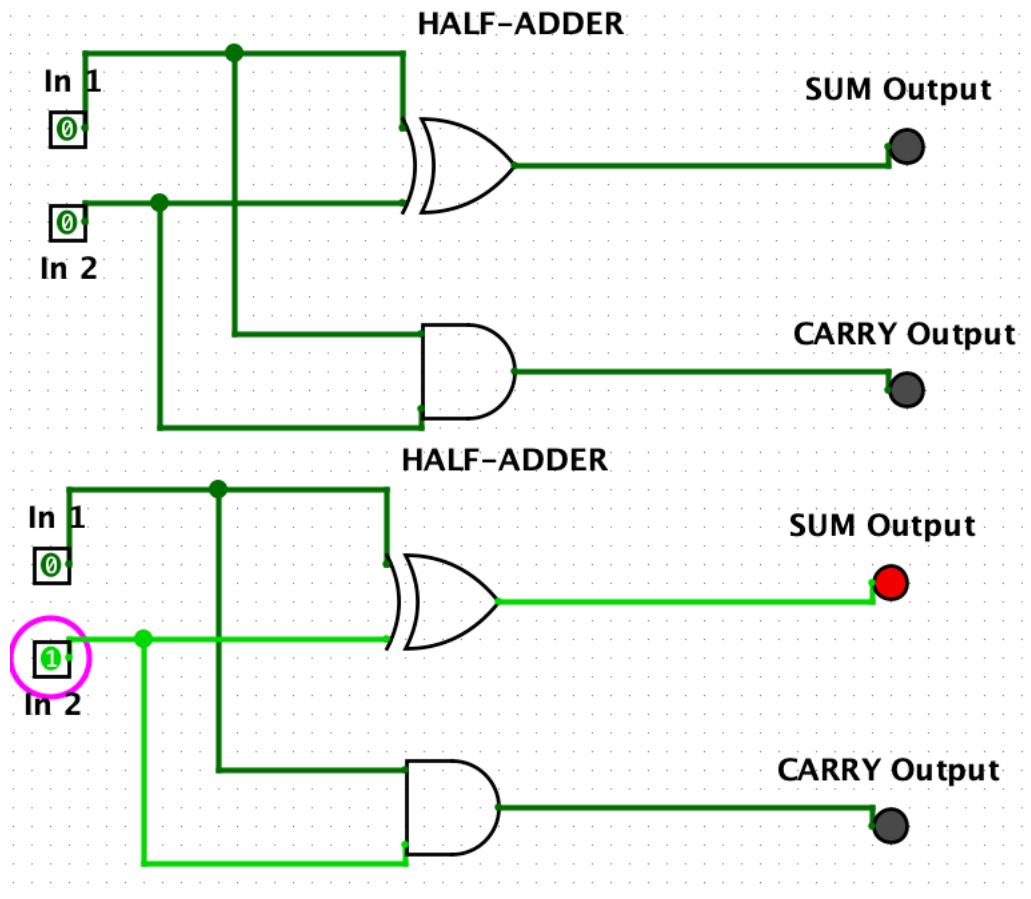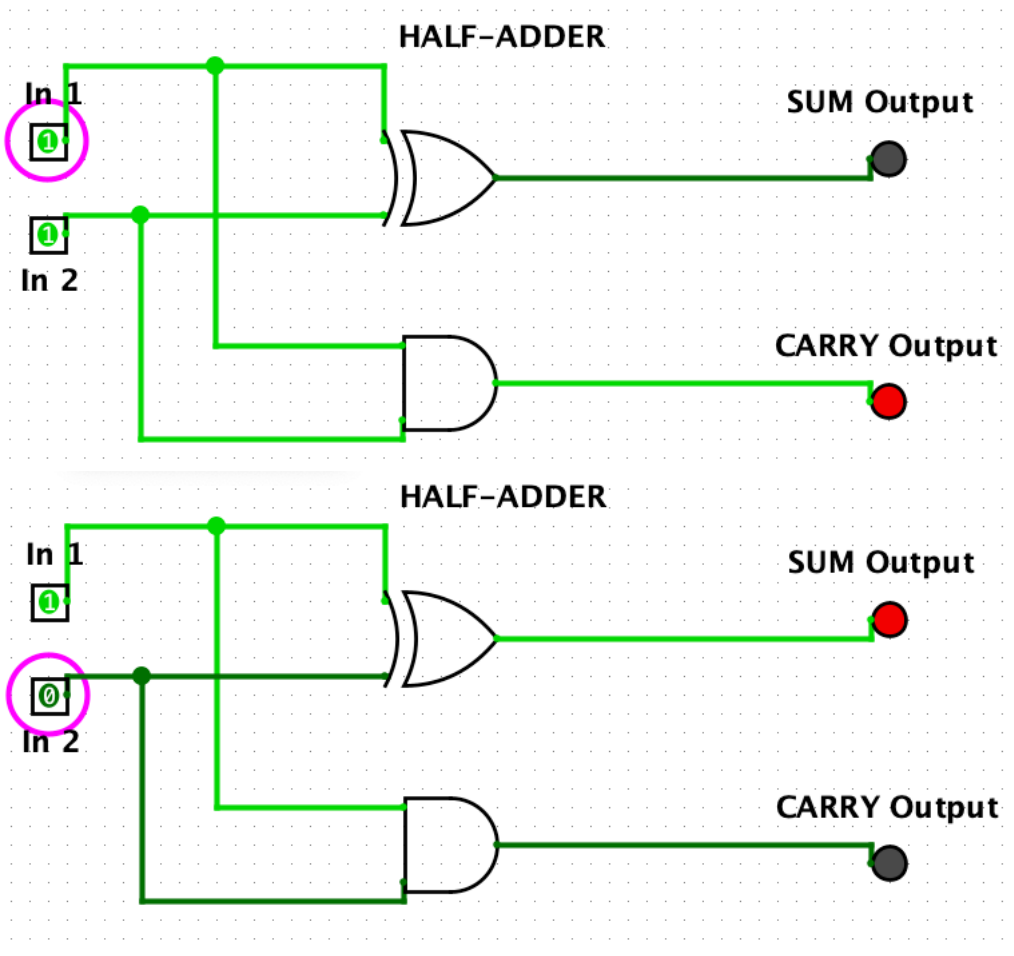
CARRY Output

FULL-ADDER Output Observed Results:

In1	In2	Carry In	Sum Output	Carry Output
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

FULL-ADDER

In 1 [0]
In 2 [0]
Carry In [0]

SUM Output
CARRY Output

FULL-ADDER

In 1 [0]
In 2 [1]
Carry In [0]

SUM Output
CARRY Output

FULL-ADDER

In 1 [1]
In 2 [0]
Carry In [0]

SUM Output
CARRY Output

FULL-ADDER

In 1 [1]

In 2 [1]

Carry In [0]

SUM Output

CARRY Output

FULL-ADDER

In 1 [0]

In 2 [0]

Carry In [1]

SUM Output

CARRY Output

FULL-ADDER

In 1 [0]

In 2 [1]

Carry In [1]

SUM Output

CARRY Output

FULL-ADDER

In 1 1

In 2 0

Carry In 1

SUM Output

CARRY Output

FULL-ADDER

In 1 1

In 2 1

Carry In 1

SUM Output

CARRY Output