# National University of Computer & Emerging Sciences, Karachi

**Spring-2019 CS-Department**

**MidTerm 2**

**2nd April 2019, 1:00 pm – 2:00 pm**

| Course Code: CS205 | Course Name: Operating Systems |
|---|---|
| Instructor Name / Names: Dr. Hasina Khatoon, Nausheen Shoaib, and Tania Iram | |
| Student Roll No: | Section No: |

Instructions

- Read each question completely before answering it. There are **3 questions on 1 page**.
- In case of any ambiguity, you may make assumptions. But your assumptions should not contradict any statement in the question paper.
- All the answers must be solved according to the sequence given in the question paper.

**Time**: 60 minutes. **Max Marks:** 60

***Q1:*** Answer the following questions briefly: [**21 marks**]

i. List the steps taken in translating virtual address to physical address without the use of TLB.
ii. Differentiate between hard and soft real-time systems.
iii. How does internal fragmentation of memory take place? Which memory management technique may have external fragmentation?
iv. Why is there a need for *page replacement* in virtual memory environment?
v. Differentiate between user and kernel level threads, giving the pros and cons of each.
vi. How many memory accesses are required to access data in a three-level page table implementation? Explain your answer.

***Q2 (a)*** Consider a virtual memory of 4 GBytes, a page size of 4Kbytes and $2^{20}$ pages of logical address space. The physical memory comprises of 64 Mbytes. **[8]**

(i) How many bits are required in the virtual address?
(ii) How many bits are required in the physical address?
(iii) Give the logical address (in binary or hexadecimal) for offset of 16 on page No. 20.
(iv) How many entries are there if an inverted page table is used?

***Q2(b)*** Calculate the physical addresses for each of the following logical addresses, using the segment table given below: [10]

| Segment No | Limit | Base |
|---|---|---|
| 0 | 2000 | 50000 |
| 1 | 1000 | 40000 |
| 2 | 1500 | 20000 |
| 3 | 1200 | 10000 |
| 4 | 500 | 30000 |

**i. 3: 1000**
**ii. 4: 900**
iii. **2: 300**
iv. **0: 2000**

***Q3(a).*** Calculate the effective memory access time if the hit ratio of the TLB is 97% and time to search the TLB is 20nsec. The memory access time 110 nsec and there is a single level page table. [6**]**

***Q3(b)*** Give the number of page faults for the following reference string using FIFO and LRU page replacement algorithms. Assume that there are four page frames available using demand paging. [15]

**1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6**