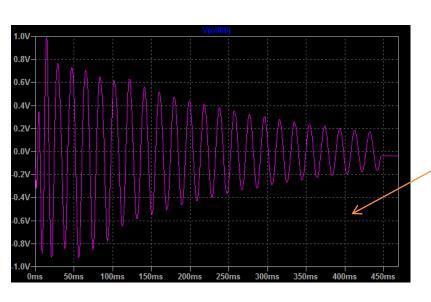
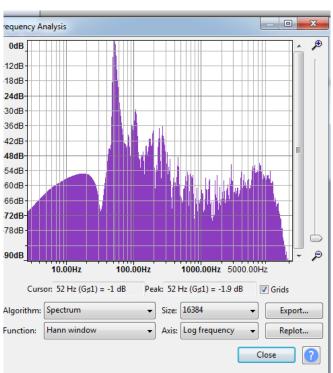
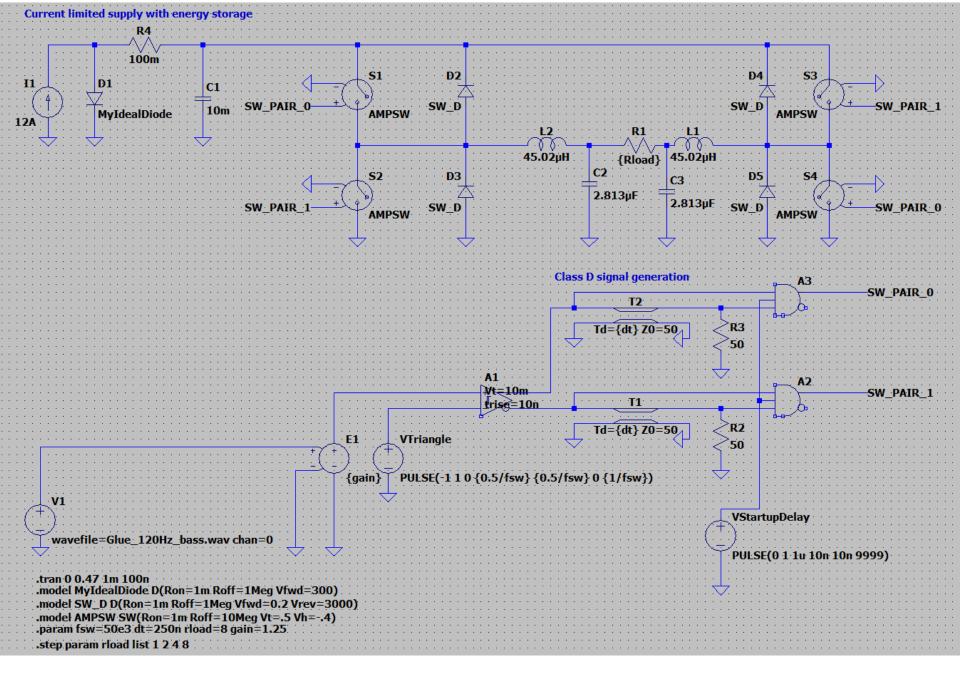


Fundamental = 52 Hz Minimum time between hits = 0.7s



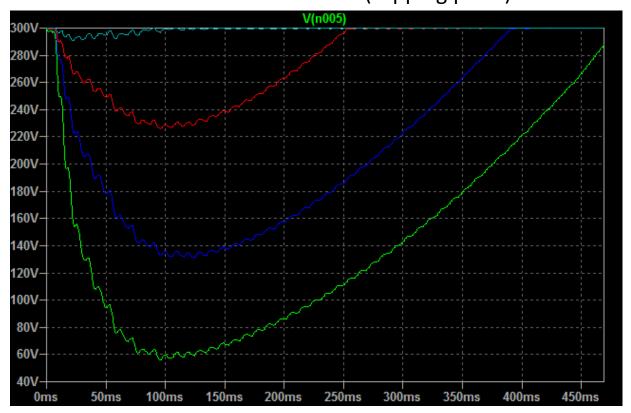
Imported into LTSPICE after 120Hz 4<sup>th</sup> order LP filter





LT spice simulation of current limited supply with large capacitive storage

Supply voltage sag with different resistive loads  $(8/4/2/1\Omega)$  @ 300V nominal bus. Peak level set to 100% modulation (clipping point).

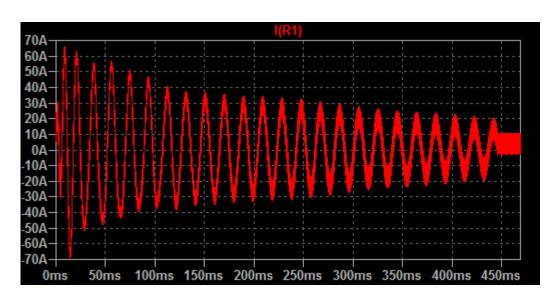


Results indicate running with 300V bus is sane for 8/40hm and amplifier will be essentially distortion free for 80hm at peak output.

Load	Minimum bus voltage	Compression	Recovery time
8	290.8V	-0.27dB	108mS
4	225V	-2.50dB	255mS
2	131V	-7.20dB	NA
1	56V	-14.60dB	NA

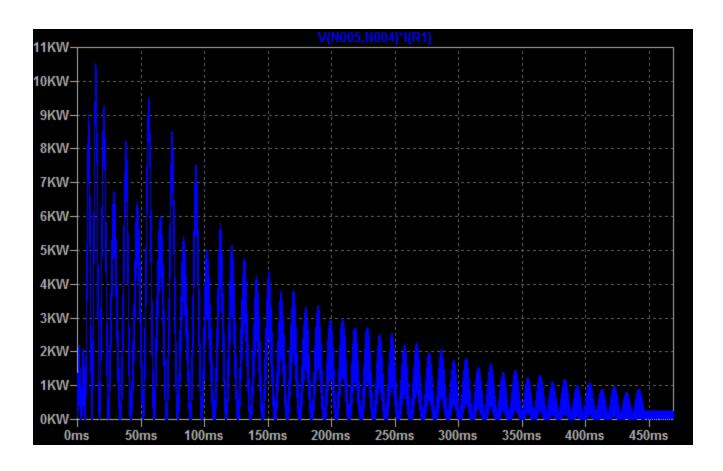
Look ahead limiter will compress input signal to avoid class-D amplifier reaching 100% modulation, the minimum required compression is recorded

## Output current into $4\Omega$ (also approximate capacitor ripple)



RMS capacitor: 80hms 14.365A, 40hms 21.428A

## Power output into 8ohms



## Strategies for dealing with low ohm load (IPAL etc.)

- Reduced dc bus Lowers switching loss if problematic
- Restrict maximum duty cycle lowers effective maximum output amplitude

## Limiter

- DAC drives amplifier (modulator), by monitoring rail voltage we can estimate duty cycle
- Rail voltage changes slowly, LP filter rail voltage and use to estimate duty cycle and use zero attack limiter on duty cycle estimate.
- Maximum duty cycle should be restricted to <0.5 for low ohm loads, depending on output device stress it may also be required to lower bus voltage.
- Hold/release adjustable.
- Additional user peak and long term average limiting