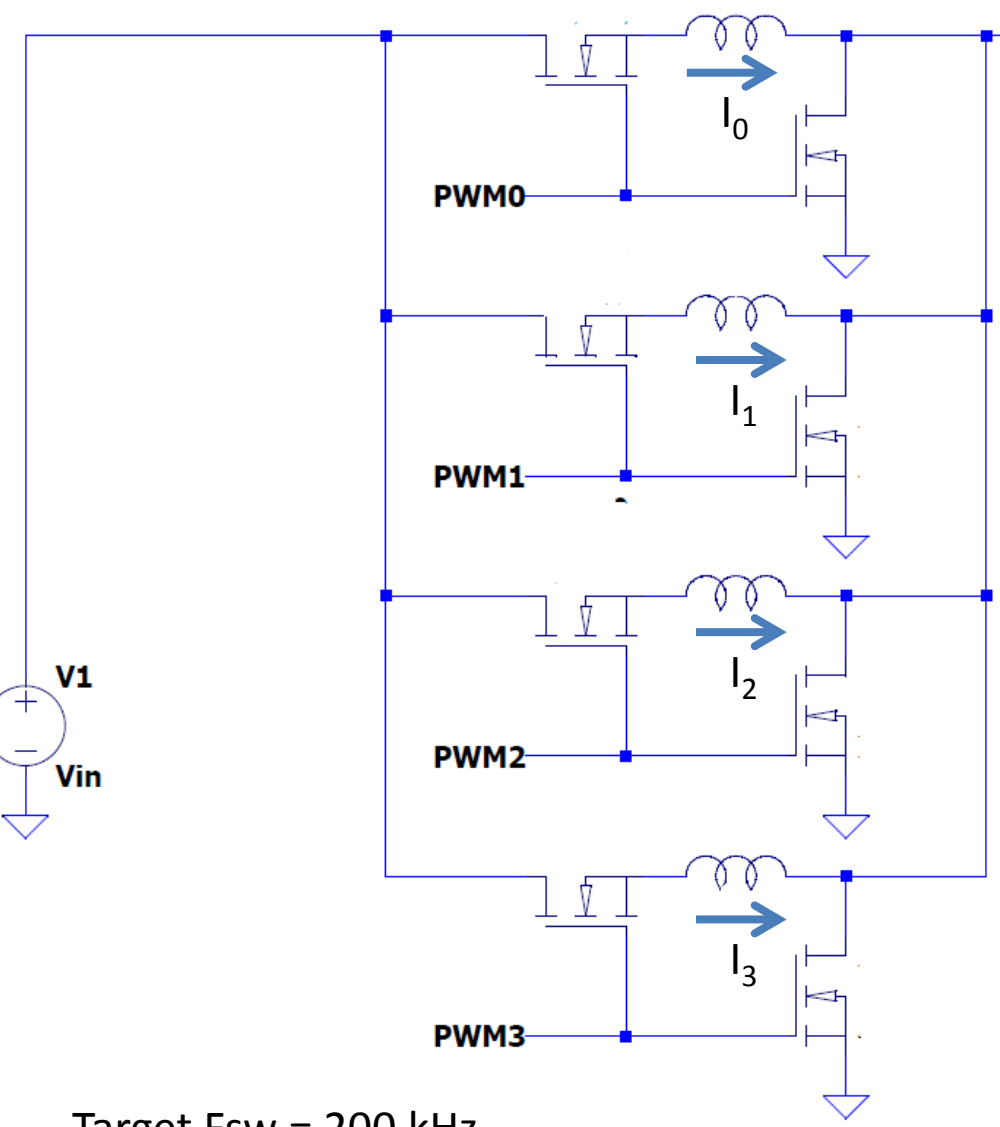


Output capacitor will be very large

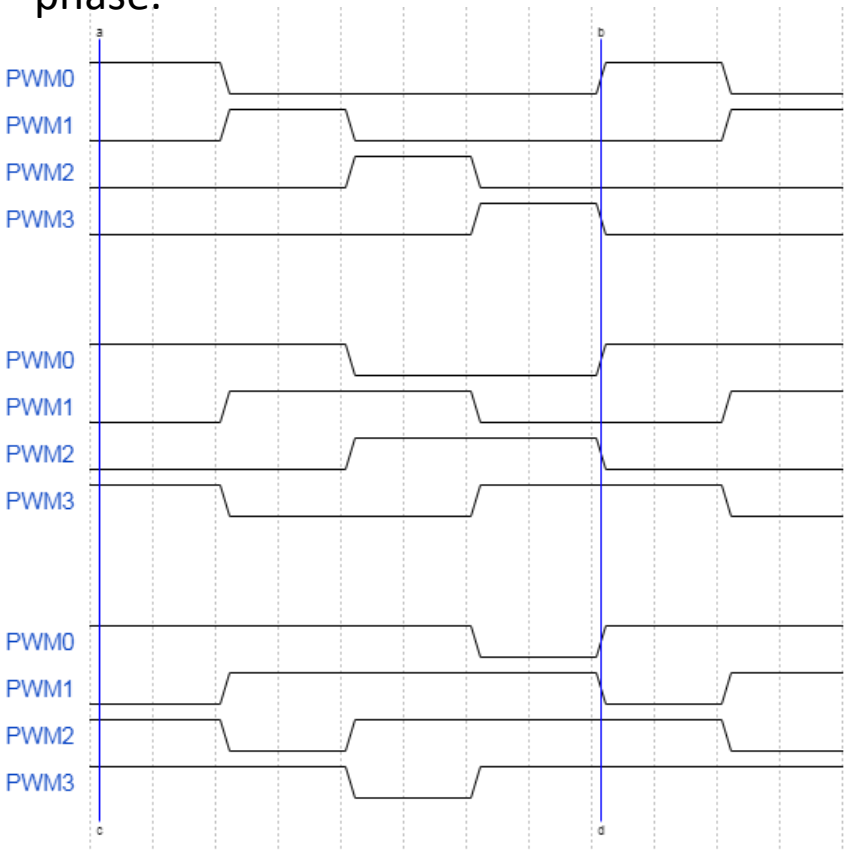
4 Phase buck converter, 4 peak current mode controlled modulators or average current mode control. Inductor currents are sensed, these are output current with some ripple. Output voltage is sensed. Normally the duty cycle will be controlled by the voltage loop, however if the inductor currents approach the current set points the duty cycle becomes controlled by the inductor currents such that the supply current limits. If the output voltage becomes too low when not starting up however this indicates a fault (IE load below 1Ω) and the supply should disable.

Target Fsw = 200 kHz,
effective = 800 kHz

5 Sensed quantities: inductor currents and output voltage. They should be synchronously sampled with the PWM cycle so that switching noise is cancelled

A Single PWM period (T) for PWM0 is shown in the period ab. At the start of the period for non zero duty cycles the PWM output goes high, the greater value of duty cycle (σ) the longer the PWM output is on for. In the case of σ = 1 it would never turn off. However σ > 0.9 should be prohibited as this will cause the bootstrap voltage for the high side MOSFET to not be able to recharge.

Each PWM output has its own separate current loop with the control input ¼ of the total desired maximum output current, this balances the current in the phases. They are different in that point a is shifted in time by 0.25T with respect to the adjacent phase.

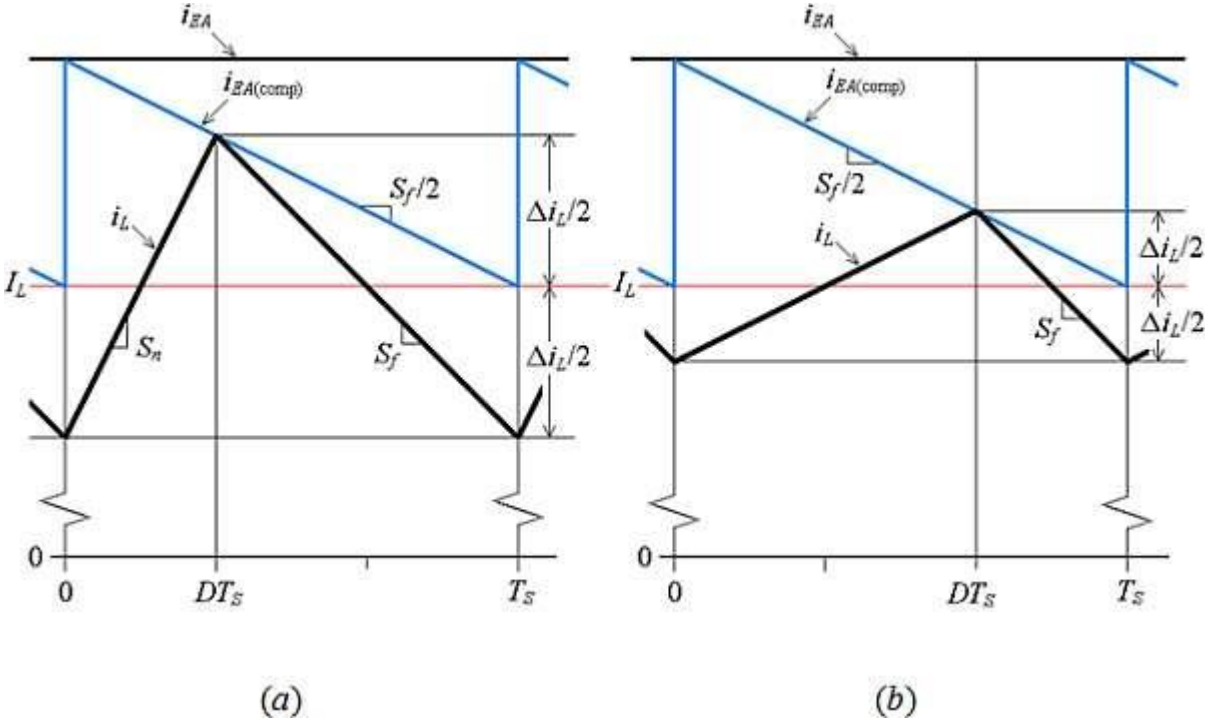


σ = 0.2

σ = 0.5

σ = 0.8

https://www.edn.com/slope-compensation-in-pcmc-dc-dc-converters/ ← good explanation of the inductor currents and how duty cycle affects the measured current



Due to the speed of the converter and that it more accurately reflects the output quantities we probably want average current mode control not peak current mode control. The current sensors have ~1Mhz bandwidth but I will include provision to low pass filter them such that the ADC input is already averaged. Otherwise it would have to be taken into account where in the PWM cycle the sample point is (this may be the better approach).

Considering that duty cycle cannot exceed 0.9 there is a minimum time of 500nS before each PWM cycle begins where the last high state must have ended