Spice Model User Guide

User Guide

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1.   Introduction

Models provided by GaN Systems Inc. are not warranted by GaN Systems Inc. as fully representing all of the specifications and operating characteristics of the semiconductor product to which the model relates. The models describe the characteristics of typical devices. In all cases, the current data sheet information for a given device is the final design guideline and the only actual performance specification.

Although models can be a useful tool in evaluating device performance, they cannot model exact device performance under all conditions, nor are they intended to replace breadboarding for final verification. GaN Systems Inc. therefore does not assume any liability arising from their use. GaN Systems Inc. reserves the right to change models without prior notice.

2.   Definitions and Functions of Model Levels

GaN Systems Inc. provides two different levels of models for GaN E-HEMT transistors. The definition and functions of the model levels are shown in the Table 1 and Table 2, respectively.

Table 1. Definitions of model levels

Suffix	Level	Terminals	Description
_L1	1	G, D, S, SS (if applicable)	General electrical simulations on application/converter level circuits. Focus on simulation speed.
_L3	3	G, D, S, SS (if applicable), Tc, Tj	In addition to L1, L3 also includes the thermal model and package stray inductance.

Table 2. Functions of model levels

Functions	Level 1	Level 3
IV performance as a function of temperature	✓	✓
Voltage-dependent capacitance	✓	✓
Thermal model	✘	✓
Package stray inductance	✘	✓

2.1. Level 1 model

The Level 1 model has either three or four terminals. For those devices with a source sense terminal, a fourth pin SS will be provided as well. Their symbols are shown in Fig. 1. Note that the dual gates or dual source senses are not modelled.
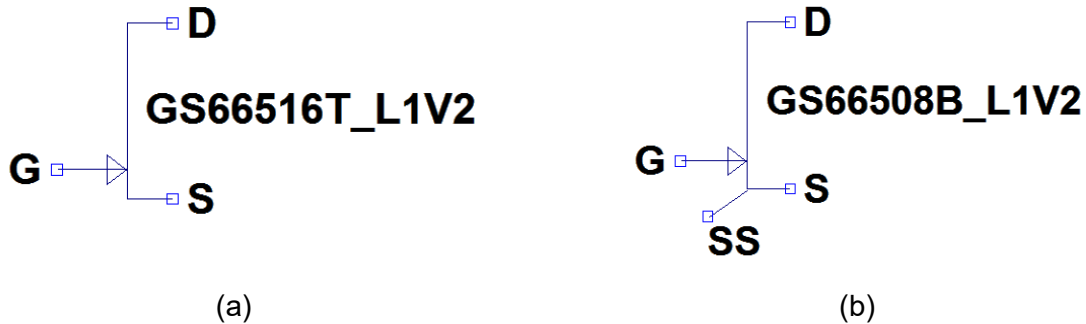

Fig. 1. Level 1 model symbol, (a) without SS terminal, (b) with SS terminal.

For the Level 1 model, as the thermal network is not included, the junction temperature needs to been defined. User can put an additional SPICE Directive command to set the junction temperature as shown in below,

.option temp=85; Set Tj

2.2. Level 3 model

In addition to Level 1 model, the Level 3 model also includes the thermal model and package stray inductance. The device structure with package stray inductance is shown in Fig. 2a. The symbol of Level 3 is shown in Fig. 2b, which has two additional pins. They are the Tc terminal (case temperature) and Tj terminal (junction temperature).
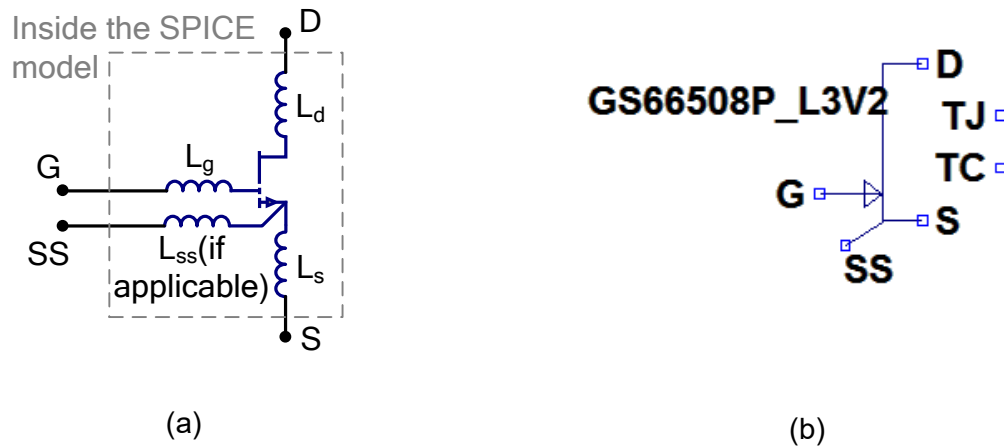
Fig. 2. Level 3 model (a) structure, (b) symbol

The thermal model inside the device model is Cauer model [1]. The junction-to-case thermal resistance is included in the Spice model for each device. Therefore, user only needs to define either a case temperature or an ambient temperature along with adding a case-to-ambient thermal resistance, like heatsink or thermal interface material (TIM). The thermal model structure and the possible connections are shown in Fig. 3. Unlike to Level 1, the TEMP does not need to be defined in the SPICE Directive command for Level 3.

Note: in the thermal model, voltage source indicates temperature in °C and resistor indicates thermal resistance in °C/W.
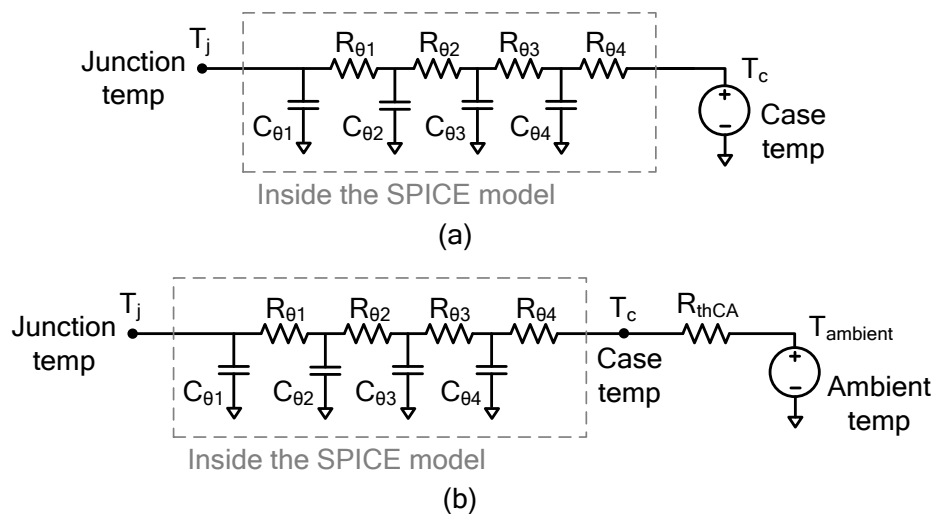
Fig. 3. SPICE Cauer model with (a) case temp as input, (b) case-to-ambient thermal resistance and ambient temp as inputs

A simple boost converter is used as an example shown in Fig. 4. An ambient temperature and heatsink thermal resistance are defined as 25°C and 10 °C/W, respectively. The simulation results are shown in Fig. 5 and Fig. 6. It is clear that the transient junction and case temperatures are risen from the 25°C ambient temperature and then reach to their steady states.
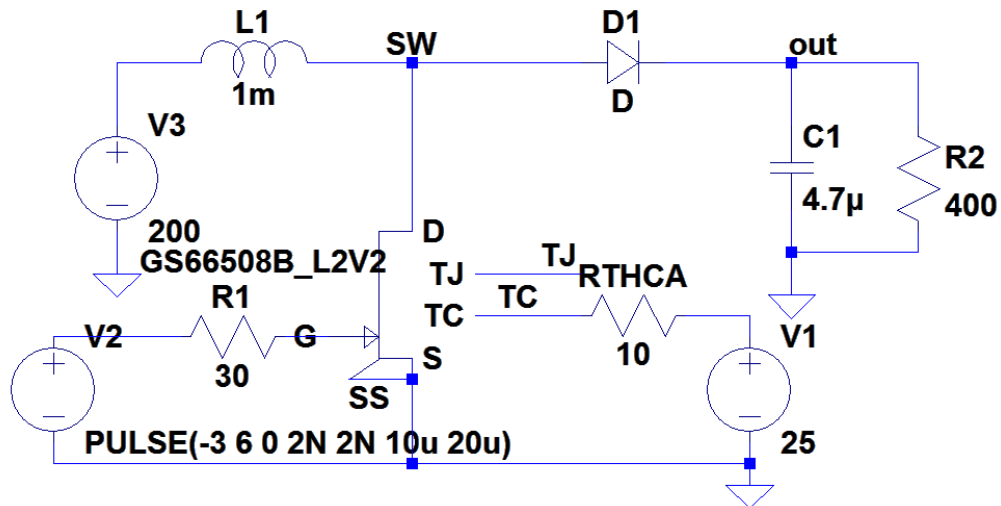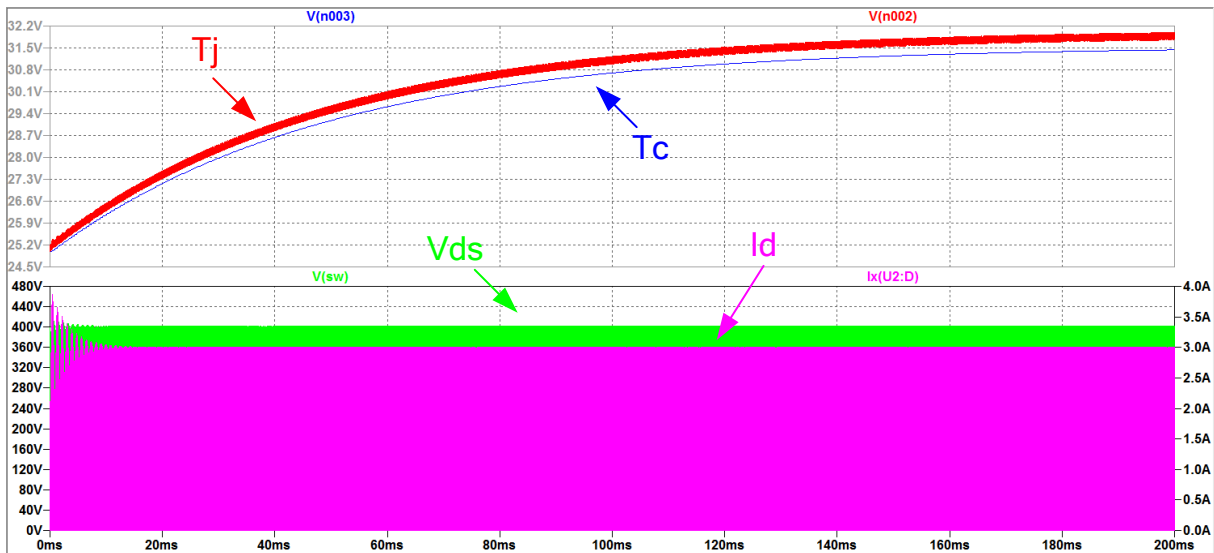

Fig. 4. A boost converter simulation example
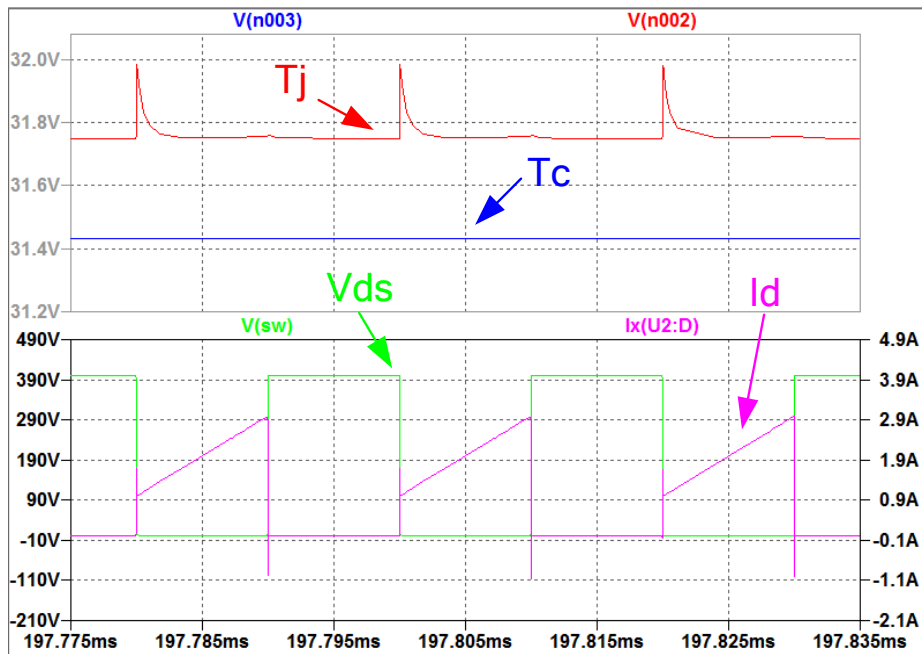

Fig. 5. Simulation waveforms of boost converter

Fig. 6. Zoomed simulation waveforms of boost converter

3. Model Files Setup

3.1. LTspice model files setup

Each of the LTspice model files includes one .lib file and one asy. file. Before implementing the LTspice model-based simulation circuit, the LTspice model files need to be installed into the user's LTspice simulation tool library.

For LTspice model, the path to place the .lib file is shown as below,

This PC → Documents → LTspice → lib → sub

The path to place the .asy file is shown as below,

This PC → Documents → LTspice → lib → sym

Once place the files under the library, please restart the LTspice program. Then the device should be able to be found in the "component" (⊃) section.

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3.2. Pspice model files setup

The Pspice model file is in .lib format. Before implementing the Pspice model-based simulation circuit, the Pspice model files need to be installed into the user's Pspice simulation tool library. A symbol can be created automatically for the users when associating the models and symbols.

4.   Reference

[1] GaN Systems, GN007 Modeling Thermal Behavior of GaNPX® E-HEMTs Using RC Thermal SPICE Models, [Online]. Available: http://www.gansystems.com/whitepapers.php

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