



Application Brief

GaN Switching Loss Simulation using LTSpice

May 23, 2018

- GaN Systems provides Pspice/LTSpice simulation models for GaN Enhancement mode HEMT.
- In this presentation, a half bridge double pulse test circuit in LTSpice is introduced and used as the test bench to evaluate switching performance under different electrical parameters.
- Switching losses were simulated and compared with Lab measurement

Figure 1: Schematic diagram of the power MOSFET switching circuit. The circuit includes two MOSFETs, HSD and DUT, each with a gate driver. The HSD MOSFET is driven by a pulse source V3 and a gate driver circuit with components V4, V5, SW_GDH, SW_GDL, L2, L3, R11, and R12. The DUT MOSFET is driven by a pulse source V2 and a gate driver circuit with components V6, V7, SW_GDH, SW_GDL, L5, L6, R2, and R3. The MOSFETs are connected to a common drain node labeled 'DUT' and a common source node labeled 'S'. The drain node is connected to a load inductor L1 and a load capacitor C1. The source node is connected to a common ground. The circuit is simulated using LTSPICE, with the simulation results showing the drain current I_D and drain-source voltage V_{DS} over time.

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Set up the simulation parameters:

.option temp=25 ; Junction temperature setting, adjust between 25 and 150C

.param VBUS = 400; DC bus voltage
.param ISW = 30; Switching Current
.param RGON = 10; Turn-on Gate Resistor
.param RGOFF = 2; Turn-off Gate Resistor
.param VDRV_P = 6; Turn-on gate voltage
.param VDRV_N = 3; Turn-off negative gate voltage

Switching test parameters

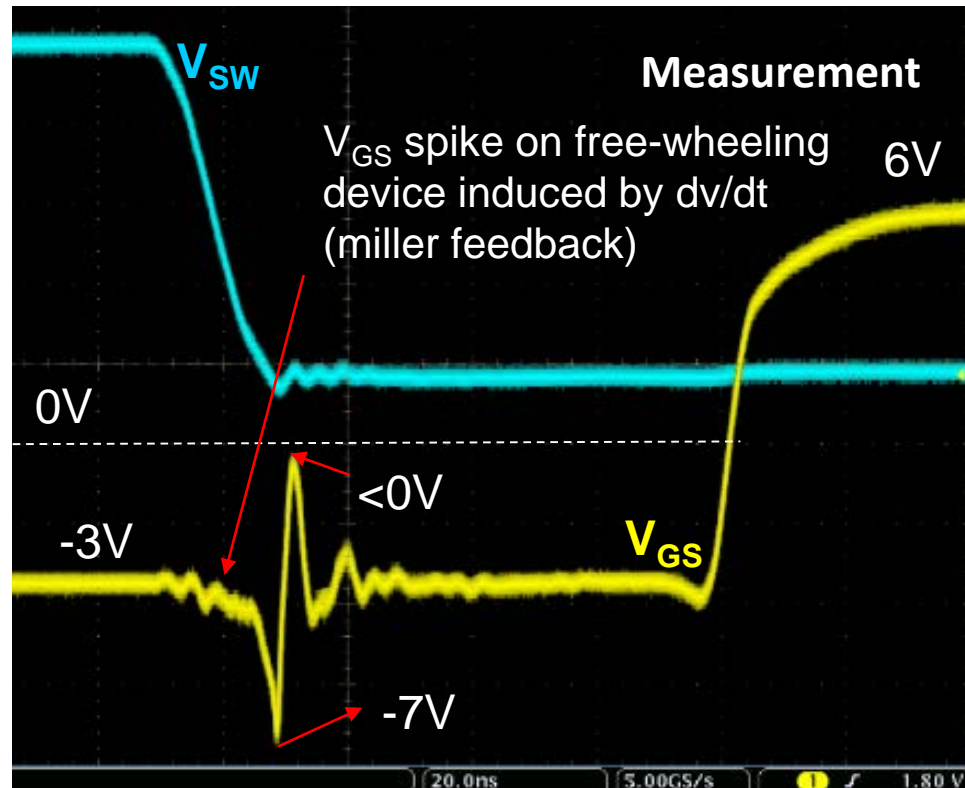
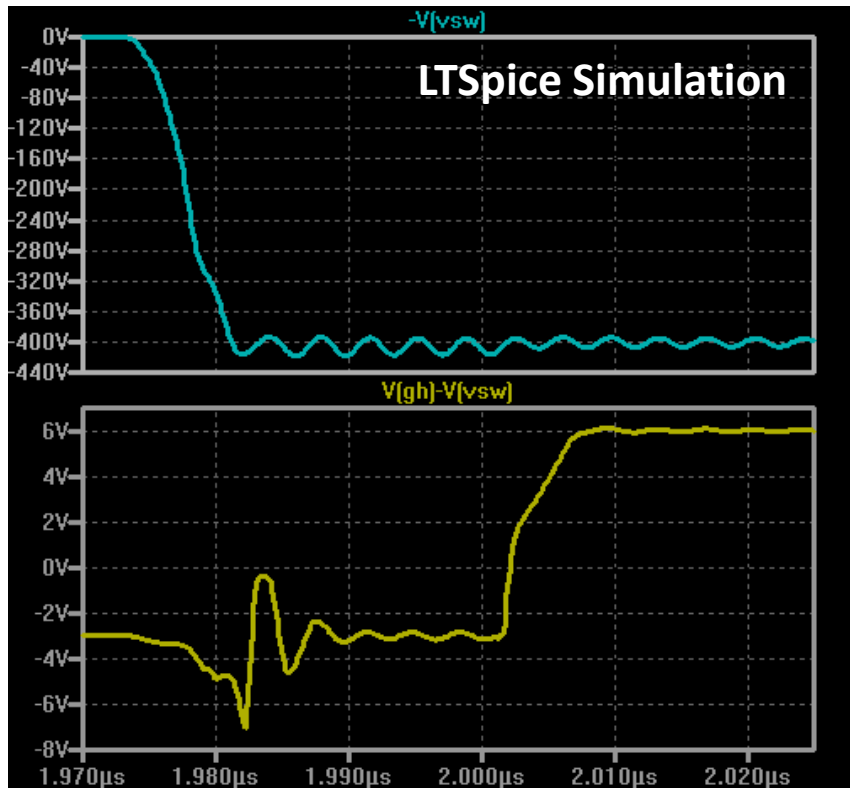
.param DT = 100n; dead time
.param T_ON = 2U; Turn-on period
.param L_DPT = VBUS * (T_ON - 2*DT) / ISW ; calculated L for switching current setting
.param T_P = 2.5U; total period

.param L_GATE = 3N; gate inductance
.param LS_EX = 10p; external source inductance
.param L_DS = 3N; power loop inductance

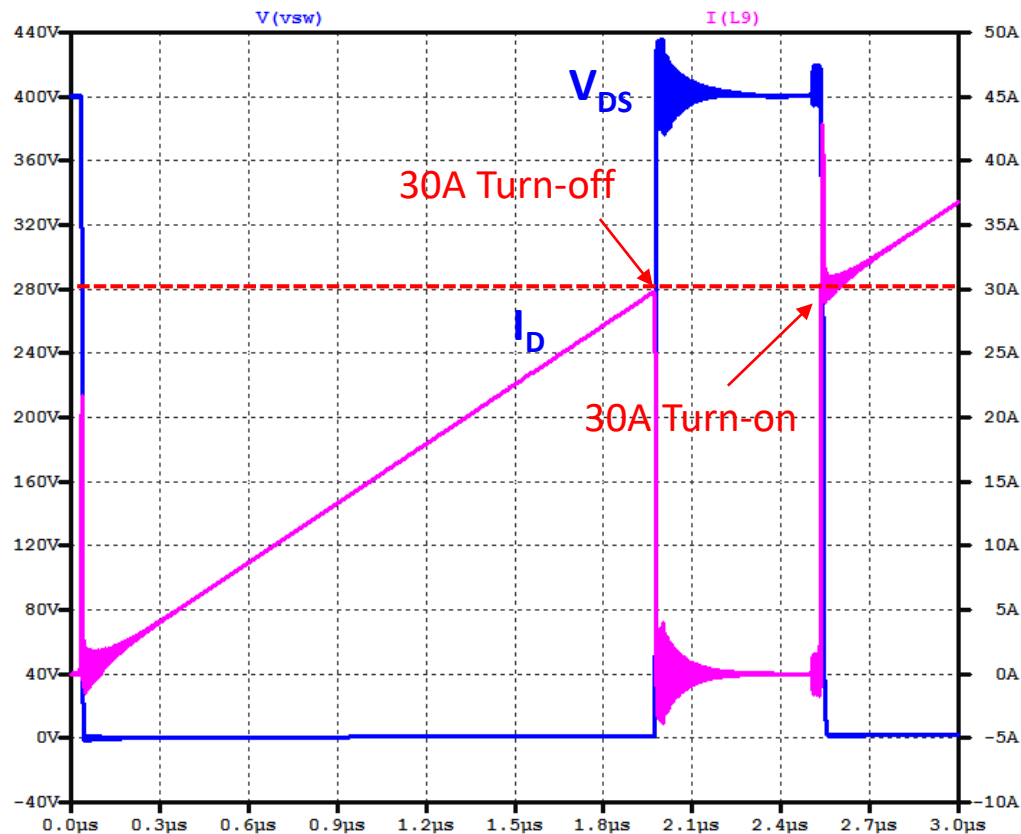
Parasitic Inductances

Gate waveforms (Simulated vs Measured)

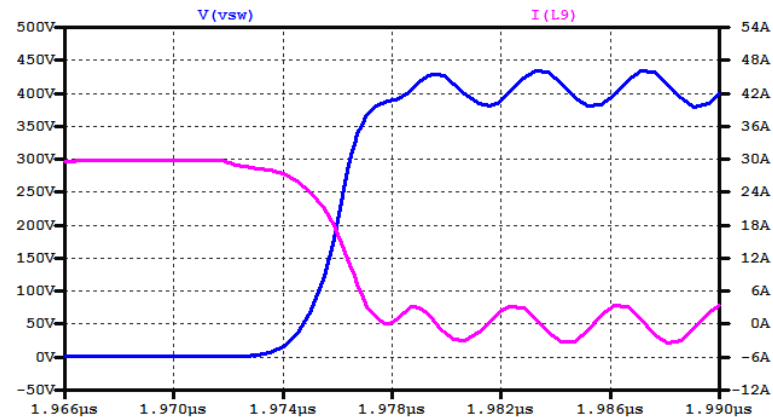
- Good correlation between simulated and measured waveforms.
- Parasitics: $L_{DS} = 3\text{nH}$, $L_{GATE} = 3\text{nH}$



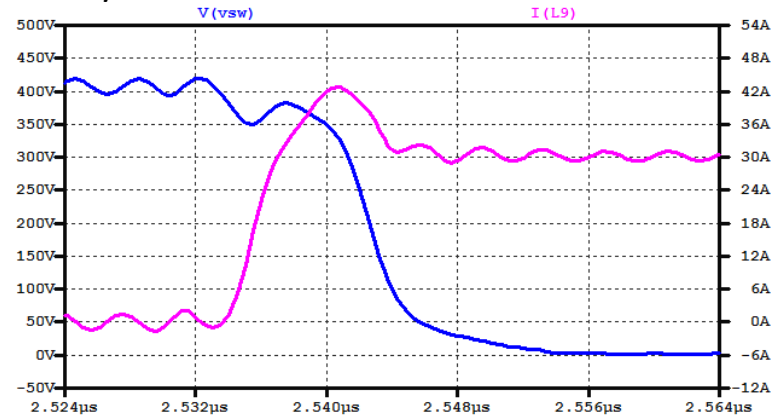
Double Pulse Simulation Results (400V/30A)



400V/30A Hard switch-off

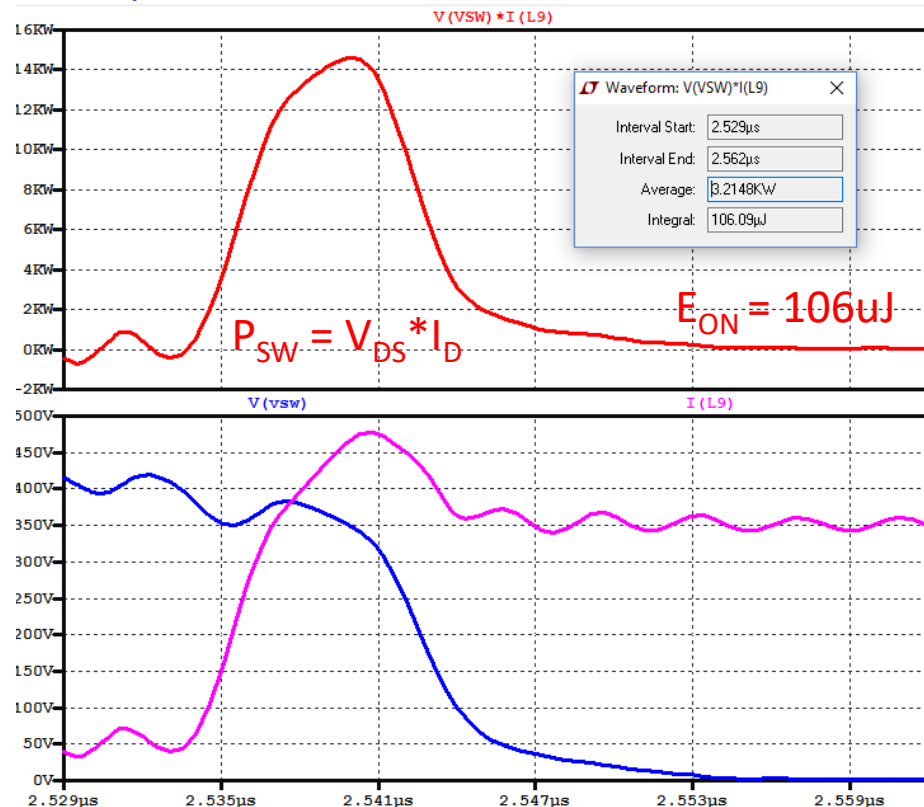


400V/30A Hard switch-on

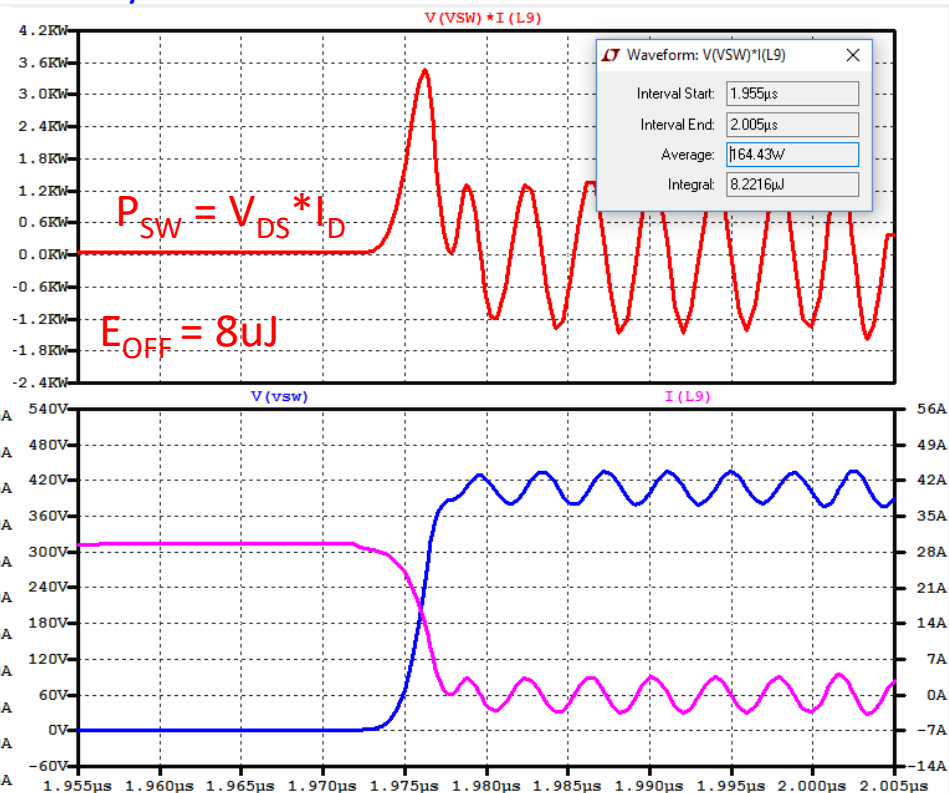


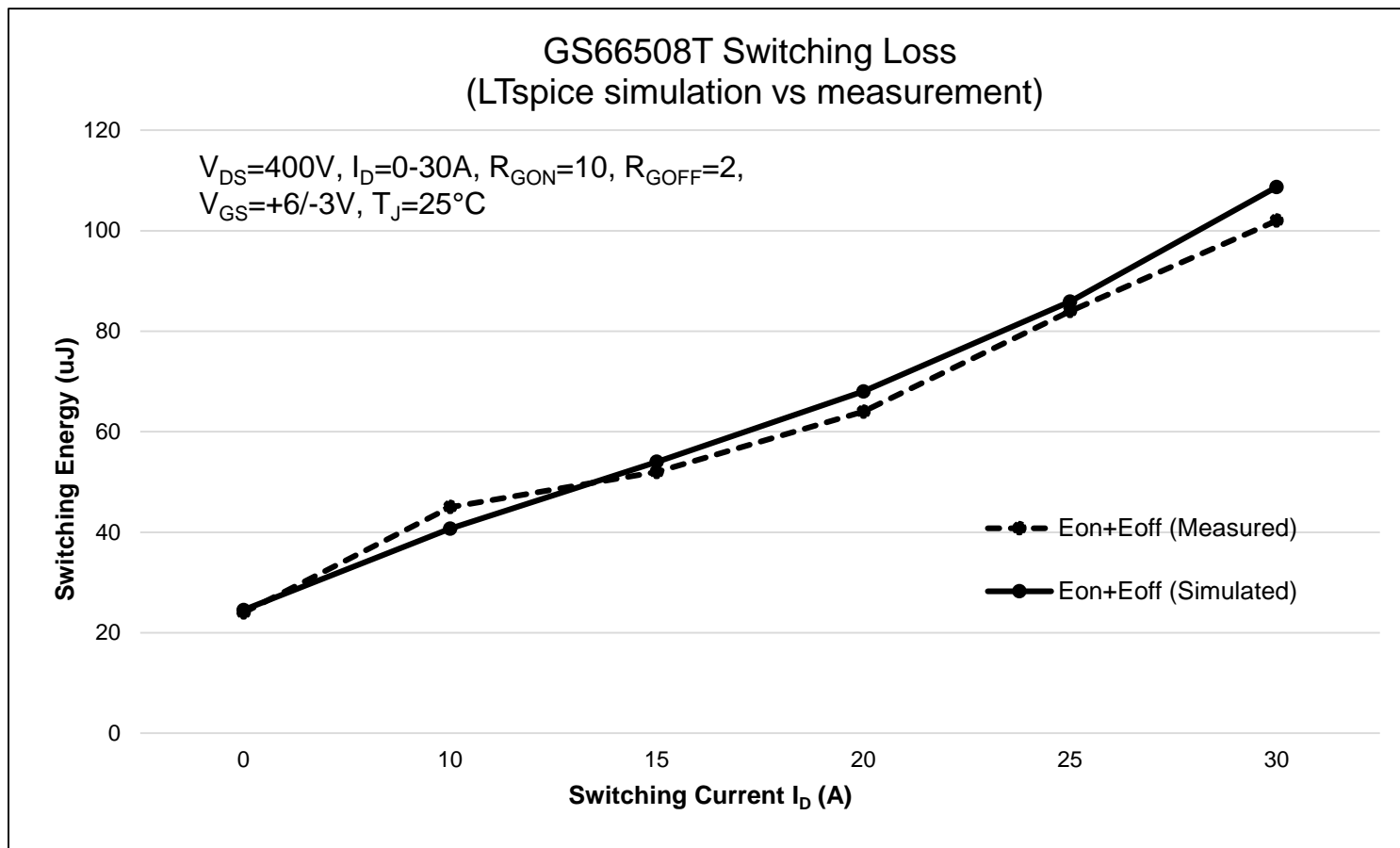
Switching Loss Calculation using LTSpice

400V/30A Turn-on



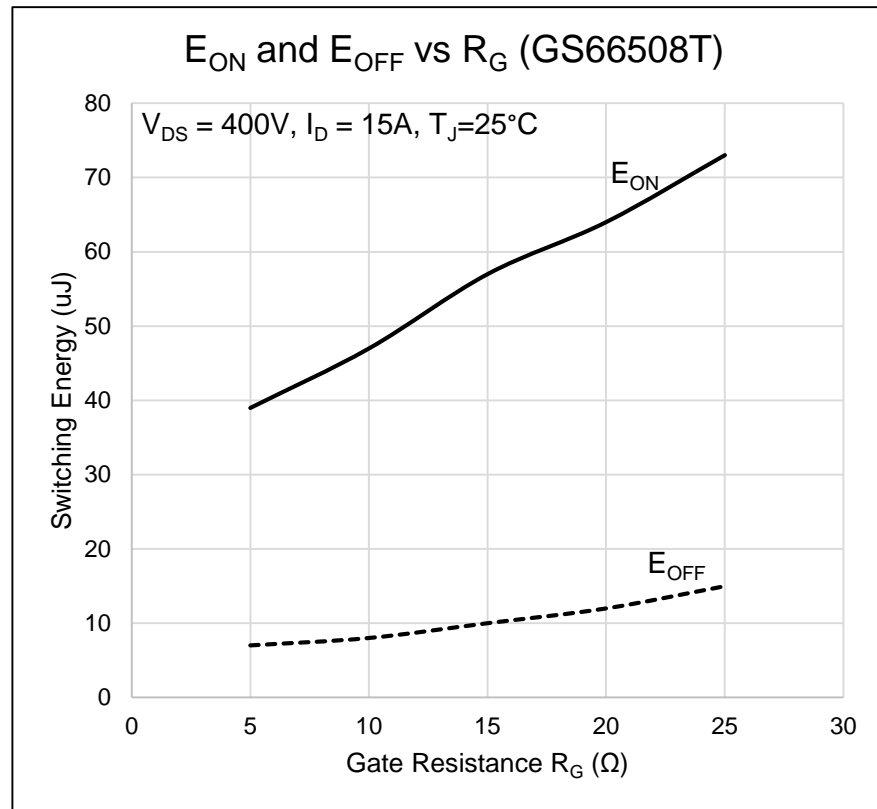
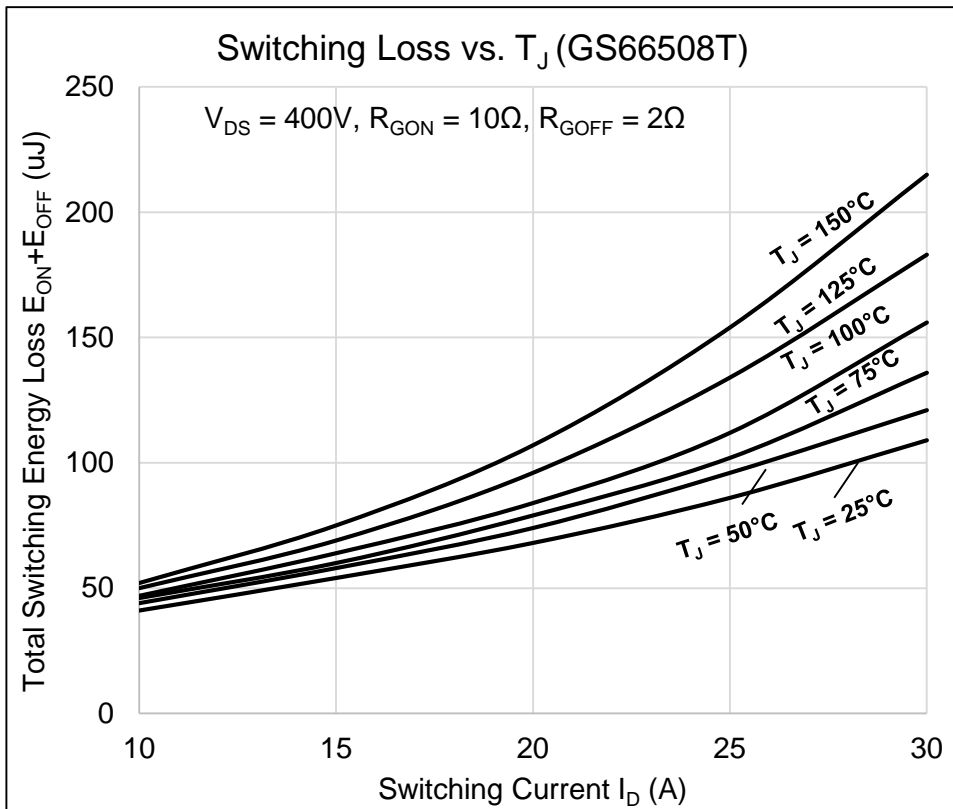
400V/30A Turn-off





- Turn-on loss increases with T_J due to the reduced trans-conductance at higher temperature
- Turn-off for GaN is small and less temperature dependent

- Switching Loss increases with R_G .

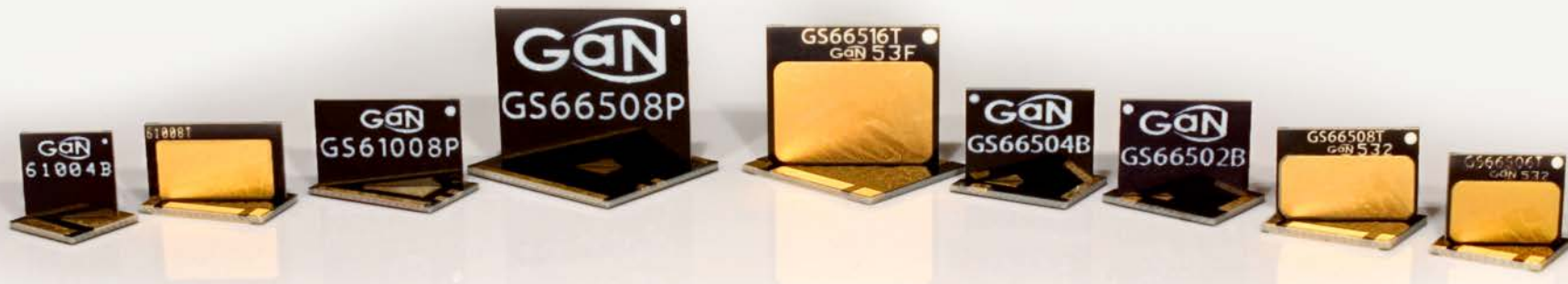


- The GaN E-HEMT switching losses were simulated in LTSpice using a half bridge double pulse test circuit.
- The simulation results were verified against lab measurements. Although the real world measurement can be affected by many factors, a reasonably good agreement was achieved between the simulation model and measurement data.
- This LTSpice test circuit is a convenient tool for end users to set up a simulation platform and familiarize themselves with with GaN E-HEMT switching characteristics.
- It can also be used to easily evaluate the effects of different electrical parameters on GaN E-HEMT switching performance.

[Click to download LTSpice Simulation File](#)

[Click to download the LTSpice Model User Guide](#)

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