Average Current Mode Control
of Switching Power Supplies

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Abstract

Current mode control as usually implemented in switching power supplies actually senses and controls peak inductor current. This gives rise to many serious problems, including poor noise immunity, a need for slope compensation, and peak-to-average current errors which the inherently low current loop gain cannot correct. Average current mode control eliminates these problems and may be used effectively to control currents other than inductor current, allowing a much broader range of topological application.

General Perspective

Current mode control is a two-loop system as shown in the simple example of Fig. 1. The switching power supply inductor is "hidden" within the inner current control loop. This simplifies the design of the outer voltage control loop and improves power supply performance in many ways, including better dynamics. The objective of this inner loop is to control the state-space averaged inductor current, but in practice the instantaneous peak inductor current is the basis for control. (Switch current --equal to inductor current during the "on" time--is often sensed.) If the inductor ripple current is small, peak inductor current control

is nearly equivalent to average inductor current control.

In a conventional switching power supply employing a buck derived topology, the inductor is in the output. Current mode control then is actually output current control, resulting in many performance advantages. On the other hand, in a high power factor preregulator using the boost topology, the inductor is in the input. Current mode control then controls input current, allowing it to be easily conformed to the desired sinusoidal waveshape.

Peak Current Mode Control Problems

Poor noise immunity. The peak method of inductor current control functions by comparing the upslope of inductor current (or switch current) to a current program level set by the outer loop-see Fig. 1. The comparator turns the power switch off when the instantaneous current reaches the desired level. The current ramp is usually quite small compared to the programming level, especially when V_{IN} is low. As a result, this method is extremely susceptible to noise. A noise spike is generated each time the switch turns on. A fraction of a volt coupled into the control circuit can cause it to turn off immediately, resulting in a subharmonic operating mode with much greater ripple. Circuit layout and bypassing are critically important to successful operation.

Slope compensation required. The peak current mode control method is inherently unstable at duty ratios exceeding 0.5,
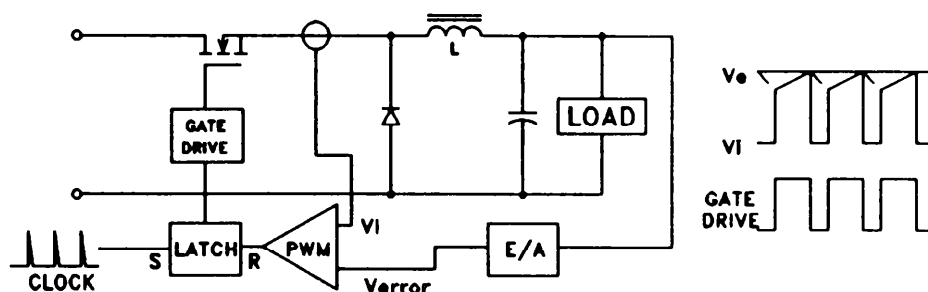

Fig. 1 - Peak Current Mode Control Circuit and Waveforms

resulting in sub-harmonic oscillation. A compensating ramp (with slope equal to the inductor current downslope) is usually applied to the comparator input to eliminate this instability. In a buck regulator the inductor current downslope equals V_O/L. With V_O constant, as it usually is, the compensating ramp is fixed and easy to calculate-but it does complicate the design. With a boost regulator in a high power factor application, the downslope of inductor current equals $(V_{IN}-V_O)/L$ and thus varies considerably as the input voltage follows the rectified sine waveform. A fixed ramp providing adequate compensation will overcompensate much of the time, with resulting performance degradation and increased distortion.

Peak to average current error. The peak to average current error inherent in the peak method of inductor current control is usually not a serious problem in conventional buck-derived power supplies. This is because inductor ripple current is usually much smaller than the average full load inductor current, and because the outer voltage control loop soon eliminates this error.

In high power factor boost preregulators the peak/avg error is very serious because it causes distortion of the input current waveform. While the peak current follows the desired sine wave current program, the average current does not. The peak/avg error becomes much worse at lower current levels, especially when the inductor current becomes discontinuous as the sine wave approaches zero every half cycle. To achieve low distortion, the peak/avg error must be small. This requires a large inductor to make the ripple current small. The resulting shallow inductor current ramp makes the already poor noise immunity much worse.

Topology problems. Conventional peak current mode control actually controls inductor current. As normally used for output current control, it is most effective when applied to a buck regulator where the inductor is in the output. But for flyback or boost topologies the inductor is not in the output, the *wrong* current is controlled, and much of the advantage of current mode control is lost.

Likewise, the boost topology with its inductor at the input is well suited for input current control in a high power factor preregulator, but buck and flyback topologies are not well suited because the inductor is not in the input and the wrong current is controlled.

Average Current Mode Control

Peak current mode control operates by directly comparing the actual inductor current waveform to the current program level (set by the outer loop) at the two inputs of the PWM comparator. This current loop has low gain and so cannot correct for the deficiencies noted above.

Referring to Fig. 2, the technique of average current mode control overcomes these problems by introducing a high gain integrating current error amplifier *(CA)* into the current loop. A voltage across R_P (set by the outer loop) represents the desired current program level. The voltage across current sense resistor R_S represents actual inductor current. The difference, or current error, is amplified and compared to a large amplitude sawtooth (oscillator ramp) at the PWM comparator inputs.

The gain-bandwidth characteristic of the current loop can be tailored for optimum performance by the compensation network around the *CA*. Compared with peak current mode control, the current loop gain crossover frequency, f_c, can be made approximately the same, but the gain will be much greater at lower frequencies.

The result is:

1) Average current tracks the current program with a high degree of accuracy. This is especially important in high power factor preregulators, enabling less than 3% harmonic distortion to be achieved with a relatively small inductor. In fact, average current mode control functions well even when the mode boundary is crossed into the discontinuous mode at low current levels. The outer voltage control loop is oblivious to this mode change.

2) Slope compensation is not required, but

there is a limit to loop gain at the switching frequency in order to achieve stability.

3) Noise immunity is excellent. When the clock pulse turns the power switch on, the oscillator ramp immediately dives to its lowest level, volts away from the corresponding current error level at the input of the PWM comparator.

4)   The average current mode method can be used to sense and control the current in any circuit branch. Thus it can control input current accurately with buck and flyback topologies, and can control output current with boost and flyback topologies.

Designing the Optimum Control Loop

Gain Limitation at f_s: Switching power supply control circuits all exhibit subharmonic oscillation problems if the slopes of the waveforms applied to the two inputs of the PWM comparator are inappropriately related.

With peak current mode control, slope compensation prevents this instability.

Average current mode control has a very similar problem, but a better solution. The oscillator ramp effectively provides a great amount of slope compensation. One criterion applies in a single pole system: *The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp sIope at the other comparator input.* This criterion puts an upper limit on the current amplifier gain at the switching frequency, indirectly establishing the maximum current loop gain crossover frequency, f_C. It is the first thing that needs to be considered in optimizing the average current mode control loop.

In the following examples, we assume that the power circuit design has been completed, and only the *CA* compensation remains to be worked out.

Example 1: Buck Regulator Output Current.
The simple buck regulator shown in Fig. 2 has the following operating parameters:

Switching Frequency, f_S = 100 kHz
Input Voltage, V_{IN} = 15 - 30V
Output Voltage, V_0 = 12V
Output Current, I_O = 5A (6A O.L.)
Inductance, $L = 60 \ \mu H$
max. ΔI_O @ 30V (100 kHz) = 1.2A
Sense Resistance, R_S = 0.10

C_{FP} is temporarily omitted. Zero $R_F C_{FZ}$ is well below the switching frequency. Near f_s, the amplifier gain is flat. The overall current loop has only one active pole (from the inductor).

The inductor current is sensed through R_S. (How this is accomplished will be discussed later.) The inductor current waveform with its sawtooth ripple component is amplified and inverted through the CA and applied to the comparator. The inductor current downslope (while the switch is off) becomes an upslope, as shown in Fig. 2. To avoid subharmonic oscillation, this off-time CA output slope must not exceed the oscillator ramp slope. In Fig. 2, the off-time CA output slope is much less than the oscillator ramp slope, indicating that the CA gain is less than optimum.

Calculating the slopes:

Inductor Current Downslope = Vo/L
Oscillator Ramp Slope = $Vs/Ts = Vsf_s$

Where V_s is the oscillator ramp p-p voltage, T_S and f_s are the switching period and frequency.
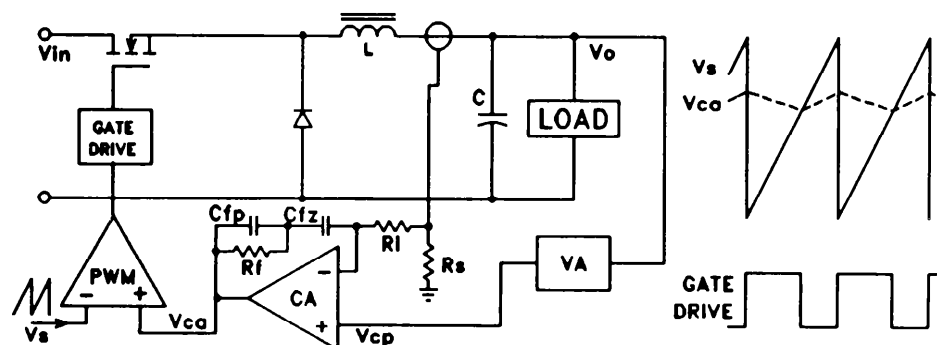

Fig. 2 - Average Current Mode Control Circuit and Waveforms

The inductor current downslope is translated into a voltage across current sense resistor R_S and multiplied by the *CA* gain, G_{CA}. This is set equal to the oscillator ramp slope to determine the *CA* gain allowed at f_S:

$$(V_O/L)R_S G_{CA} = V_S f_S$$

$$\therefore \quad \max \ G_{CA} = \frac{v_{CA}}{v_{RS}} = \frac{V_S f_S L}{V_O R_S} \quad (1)$$

Applying the values given in the example, and with V_S of 5Vpp, the maximum G_{CA} at the switching frequency is 25 (28dB). The current error amplifier gain at f_S is set to this optimum value by making the ratio $R_F/R_I = 25$.

The small-signal control-to-output gain of the buck regulator current loop power section (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_s) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\frac{V_{IN}}{sL} = \frac{1590}{f} \quad (@30V) \quad (2)$$

The overall open loop gain of the current loop is found by multiplying (1) and (2). The result is set equal to 1 to solve for the loop gain crossover frequency, f_c:

$$\frac{R_S}{V_S}\frac{V_{IN}}{2\pi f_C L}\frac{V_S f_S L}{V_O R_S} = 1$$

$$f_C = \frac{f_S V_{IN}}{2\pi V_O} = \frac{f_S}{2\pi D} \quad (3)$$

Setting the CA gain at the limit found in (1), the crossover frequency will never be less than one sixth of the switching frequency. (This is exactly the same result reported by Middlebrook [1] for peak current mode control with recommended slope compensation.) In this example, f_c is 20 kHz with V_{IN} at 15V (D= .8), and 40 kHz when V_{IN} at 30V (D= .4).

If the error amplifier had a flat gain characteristic, the phase margin at crossover would be 90° -much more than required-and the gain at lower frequencies wouldn't be much better than with peak current mode control. But zero $R_F C_{FZ}$ placed at 10 kHz, below the minimum crossover frequency, reduces the phase margin

to 63°, and boosts the low frequency gain dramatically, with an integrator gain of 250K/f. It is this characteristic which causes the current loop to rapidly and accurately home in on the average current called for by the outer loop. Even though the comparator actually turns off the power switch when a *peak* inductor current is reached, this peak current level is adjusted by the current amplifier so that the average current is correct.

Fig. 3 shows the start-up waveforms of the voltages at the PWM comparator inputs and the inductor current with V_{IN} at 30V and full load. Note how the amplified and inverted inductor current downslope virtually coincides with the oscillator ramp, because the CA gain was set at the optimum level according to Equation (1). Note also that if the CA gain is increased further, not only will the off-time slope exceed the oscillator ramp slope, but the positive excursion may reach the CA compliance limit, clipping or clamping the waveform.
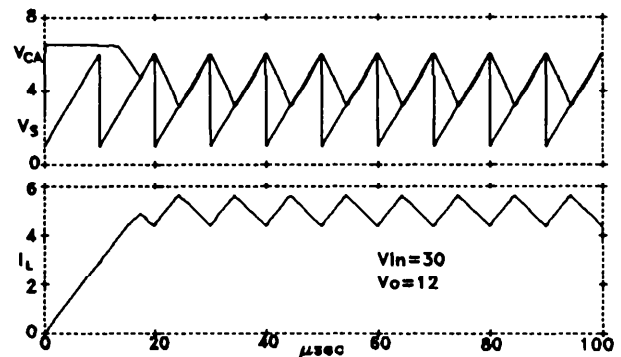

Fig. 3 - Buck Waveforms, Optimized Gain

Pole $R_F C_{FP} C_{FZ}/(C_{FP}+C_{FZ})$ is set at switching frequency f_s (100 kHz). This pole has one purpose-to eliminate noise spikes riding on the current waveform, the nemesis of peak current mode control. The sawtooth CA output waveform is also diminished, especially the higher order harmonics, and shifted in phase as shown in Fig. 4. The pole-zero pair (at 100 kHz and 10 kHz) reduces the phase margin at crossover to a very acceptable 45° -see Fig. 5.

The reduced amplitude and slopes of the CA waveform resulting from the 100 kHz pole might suggest that the CA gain could be in-

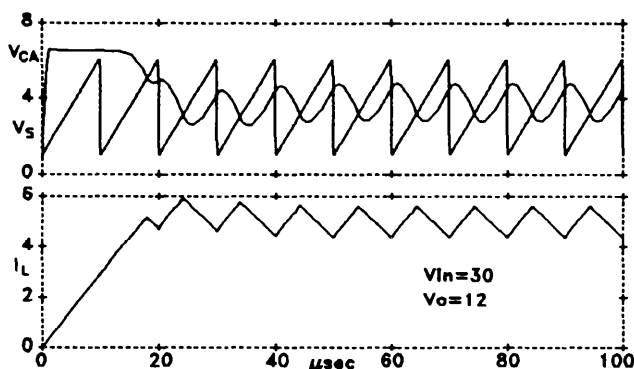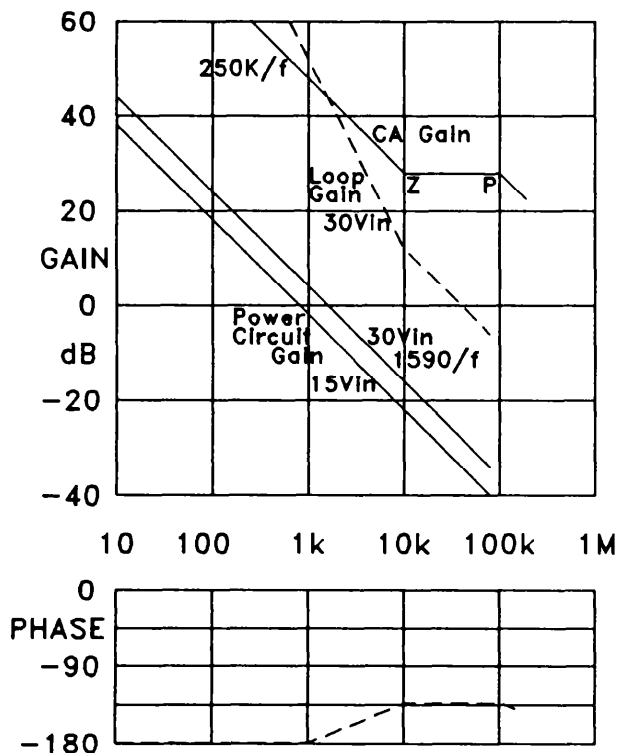Fig. 4 - Buck with Additional Pole at f_s

Fig. 4 - Buck with Additional Pole at f_s

Fig. 5 - Buck Regulator Bode Plot

creased beyond the maximum value from Equation (1), but beware-Eq. (1) is valid only for a system with a single pole response at f_s, but with C_{FP} added there are now two active poles at f_s. Experimentally, increasing G_{CA} may incur subharmonic oscillation.

Discontinuous Operation. When the load current I_O becomes small, the inductor current becomes discontinuous. The current level at the continuous/discontinuous mode boundary is:

$$I_O = I_L = \frac{V_O(V_{IN} - V_O)}{V_{IN} 2f_s L} \qquad (4)$$

Worst case is at max V_{IN}, when ripple current is greatest. In this example, the mode boundary occurs at $I_O(=I_L)$ of 0.2A when V_{IN} is 15V, and at 0.6A when V_{IN} is 30V.

In the discontinuous mode, below the mode boundary, changes in I_O require large duty cycle changes. In other words, the power circuit gain suddenly becomes very low. Also, the single pole characteristic of continuous mode operation with its 90° phase lag disappears, so the power circuit gain is flat-independent of frequency. The current loop becomes more stable, but much less responsive.

With peak current mode control in the discontinuous mode, peak/avg current error becomes unacceptably huge. But with average current mode control, the high gain of the current error amplifier easily provides the large duty cycle changes necessary to accommodate changes in load current, thereby maintaining good average current regulation.

Referring to Fig. 2, when the current loop is closed, the voltage across current sense resistor V_{RS} equals the current programming voltage V_{CP} (from the voltage error amplifier) at frequencies below f_s. The transconductance of the closed current loop is a part of the outer voltage control loop:

$$g = \frac{i_L}{v_{CP}} = \frac{v_{RS}/R_S}{v_{CP}} = \frac{1}{R_S} \qquad (5)$$

The closed loop transconductance rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_s.

Example 2: Boost Regulator Input Current.
A 1 kW off-line preregulator (Fig 6) operates with the following parameters:

Switching Frequency, f_s = 100 kHz
Input Volts, V_{IN} = 90 - 270V rms
output Volts, V_O = 380Vdc
Max. O.L. I_{IN} (@90V) = 12A rms, 17A pk
L = 0.25mH
$\Delta I_L, \Delta I_{IN}$ @90V = 3.4A
$R_S = 0.05\Omega$

The max. overload line current at min. V_{IN} corresponds to 1080W input. The max. peak overload 60Hz line current (17A) should-by design-correspond to a limit on the current programming signal, I_{CP}. The max peak 100kHz current through the switch and rectifier is 17A plus one-half ΔI_L: 17 + 3.4/2 = 18.7A
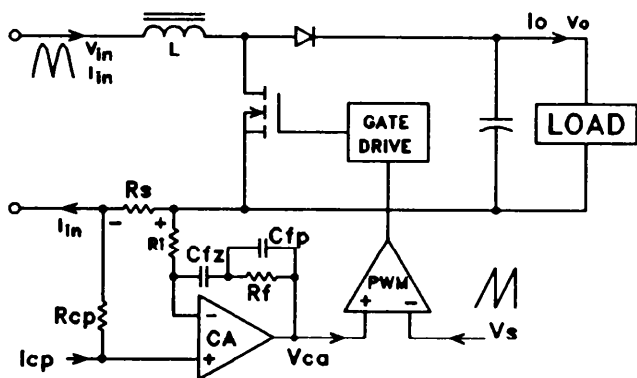

Fig. 6 - Boost Preregulator Circuit

The current downslope occurs when the power switch is off:

Inductor Current Downslope $=(V_O-V_{IN})/L$
Worst case when $V_{IN}=V_O/L$
Oscillator Ramp Slope $= Vs/Ts = Vs\, f_s$

Multiply the downslope by R_S and *CA* gain and set equal to the oscillator ramp slope, then solve for maximum *CA* gain:

$$(V_O/L)R_S G_{CA} = V_s f_s$$

$$\therefore \quad \max \; G_{CA} = \frac{\hat{v}_{CA}}{\hat{v}_{RS}} = \frac{V_s f_s L}{V_O R_S} \quad (6)$$

Note the form of Equation (6) is identical to the buck regulator in (1). Using the values for

this application, the maximum G_{CA} is 6.58, accomplished by making R_F/R_I = 6.58.

The small-signal control-to-input gain of the current loop power section (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{\hat{v}_{RS}}{\hat{v}_{CA}} = \frac{R_S}{V_S}\frac{V_O}{sL} = \frac{2420}{f} \quad (7)$$

Note that (7) is nearly identical to (2) for the buck regulator, except the gain depends on V_O (which is constant), rather than V_{IN}.

The overall current loop gain is found by multiplying (6) and (7). The result is set equal to 1 to solve for the crossover frequency, f_C:

$$\frac{R_S}{V_S}\frac{V_O}{2\pi f_C L}\frac{V_s f_s L}{V_O R_S} = 1$$

$$f_C = \frac{f_s}{2\pi} \quad (8)$$

With the *CA* gain at the limit found in (6), the current loop f_C is *fixed* at $f_s/6$ (16.7 kHz).

As with the earlier example, with a flat gain error amplifier the phase margin at crossover is 90° — larger than necessary. So zero $R_F C_{FZ}$ is set at 1/2 of the minimum crossover frequency $(f_C/2 = f_s/12 = 8.33$ kHz), providing a low frequency boost with an integrator gain of 55K/f. Pole $R_F C_{FP} C_{FZ}/(C_{FP}+C_{FZ})$ is set at 6 times the zero frequency (50 kHz) to eliminate noise spikes. Together, the zero at 8.33 kHz and the pole at 50 kHz leave a phase margin at crossover of 40°. Startup waveforms are shown in Fig. 7, and the Bode plot in Fig. 8.
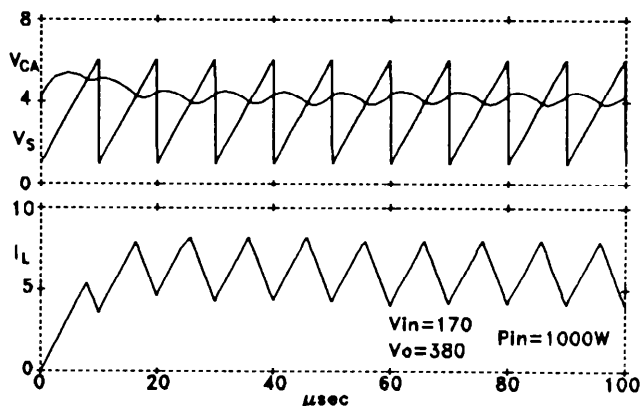

Fig. 7 - Boost Regulator Waveforms

Referring back to Fig. 6 — when the current loop is closed, the voltage across current sense resistor V_{RS} equals the voltage across current programming resistor V_{RCP}. In this case, programmed with a current source I_{CP}, the current gain of the closed current loop is:

$$G = \frac{i_L}{i_{CP}} = \frac{v_{RS}/R_S}{v_{RCP}/R_{CP}} = \frac{R_{CP}}{R_S} \qquad (9)$$

The closed loop current gain rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S.
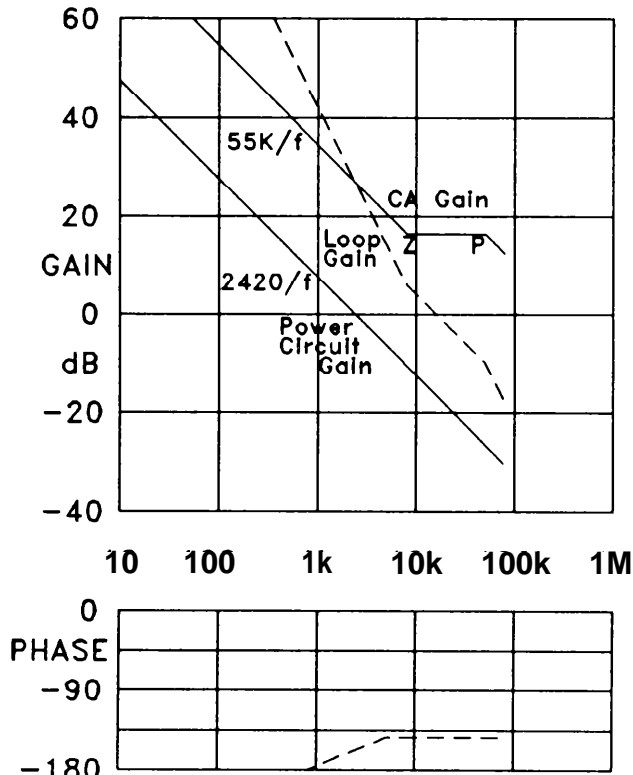

Fig. 8 - Boost Regulator Bode Plot

In a high power factor preregulator application, the current is programmed to follow the rectified line voltage. As the rectified sine wave voltage and current approaches the cusp at zero, the inductor current becomes discontinuous. Discontinuous operation can occur over a substantial portion of the line cycle, especially when line current is low at high line voltage and/or low power input. With peak current mode control, discontinuous operation results in a large peak/average current error. A large inductance is required to make ripple current small and put the mode boundary at a low

current level. However, average current mode control eliminates the peak/average error. A small inductance can and should be used to reduce cost, size and weight and improve current loop bandwidth.

Figure 9 shows a boost preregulator programmed to follow a 60 Hz (rectified) sine wave input. The lower waveforms show the programmed and actual line current waveforms. (The programmed waveform has been increased by 5% to make the two waveforms visible. The actual waveform leads the programmed waveform by a small amount and has less than 0.5% 3rd harmonic distortion! The upper waveforms show the duty cycles of the switch and diode throughout the line cycle. The inductor current is continuous when the current is high, and the switch and diode duty cycles add up to 1. But as the current approaches zero crossing, operation becomes discontinuous as shown by the appearance of "dead" time (when neither the switch, the diode, or the inductor are conducting).
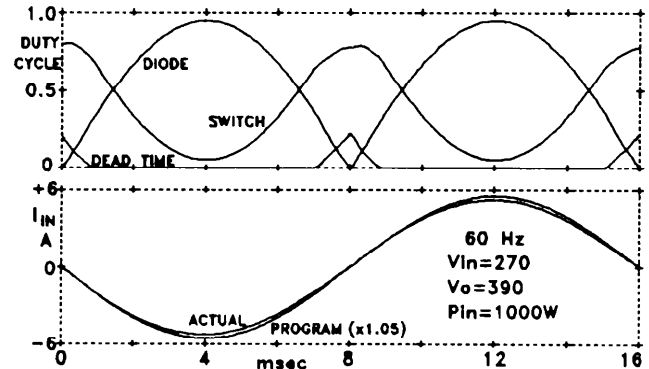

Fig. 9 - Boost 60Hz Sine Wave Input Current

Note that the switch duty cycle does not change as much when operation becomes discontinuous. With the boost (and flyback) topology in the discontinuous mode, average input current tends to follow input voltage at a constant duty cycle. Even though plenty of CA gain is available to change the duty cycle, little change is required for perfect tracking.

Figure 10 shows how the actual input current sine wave tracks the programming signal at 400 Hz. The distortion is worse -- 4.5% 3rd harmonic. This is for two reasons:
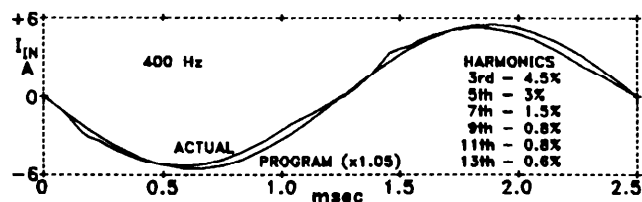
Fig. 10 - Boost 400Hz Sine Wave Input Current

1. The harmonic components of the rectified 400 Hz waveform are at higher frequencies and closer to the current loop crossover frequency where the loop gain is less, compared with the 50 or 60 Hz harmonics.
2. The inductor current has difficulty rising off zero because the input voltage is so very low at that point. So the inductor current lags coming off zero, then catches up and overshoots the programmed level. (This effect is much worse with peak current mode control because of the large inductor required.)

Controlling Average Switch Current

In the previous examples, average current mode control was applied to controlling inductor current (buck output current and boost input current). This is relatively easy because the inductor current is mostly DC with only a small amount of ripple to deal with. But if it is desired to use a buck or flyback topology to control input current in a high power factor application, then the chopped current waveform through the power switch must be averaged, a more difficult task.

Example 3: Flyback Regulator Input Current: A 1000 W off-line preregulator uses a flyback circuit in order to achieve a standard 300V output bus even though the input voltage ranges above and below 300V (Figs. 11,12).

The flyback converter could be designed to operate in the discontinuous inductor current mode in this application. The discontinuous flyback converter is not difficult to control (crudely) by fixing the duty cycle during each line half-cycle, but the peak currents through the power switch and rectifier are nearly twice as high as with continuous mode operation.
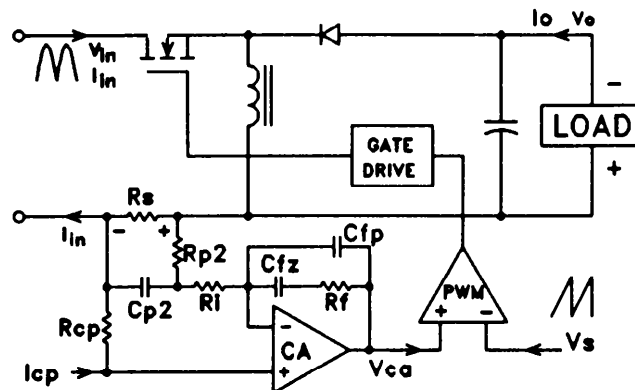

Fig. 11 - Flyback Preregulator Circuit

The high peak current lowers efficiency and requires devices with higher current ratings.

Continuous mode operation suffers the problem that the boundary is crossed into the discontinuous mode at light loads and high input voltage, unless a large filter inductor is used, which hurts the frequency response and the power factor as well as the pocketbook.

This dilemma disappears with average current mode control because it functions well in the discontinuous as well as the continuous mode, enabling the use of a small inductance value. In this example, the flyback converter operates in the continuous mode when it is important do so--at high current levels, to keep the maximum peak current to half that of a strictly discontinuous flyback converter. The operating parameters are:

$$\text{Switching Frequency, } f_S = 100 \text{ kHz}$$
$$\text{Input Volts, } V_{IN} = 90 - 270V \text{ rms}$$
$$\text{Output Volts, } V_O = 300V \text{ dc}$$
$$\text{Max. O.L. } I_{IN} (@90V) = 12A \text{ rms, } 17A \text{ pk}$$
$$L = 0.25mH$$
$$\Delta I_L @9OV = 3.6A$$
$$R_S = 0.025\Omega$$

The max. overload rms line current at min. V_{IN} equates to 1080W input (2160Wpk 60Hz). The max. overload peak 60 Hz line current (17A) should be made to correspond to a limit on the current programming input, I_{CP}. Unlike the boost converter, the flyback input current is chopped, so the peak 100kHz current through

the switch, the inductor, and the rectifier are much greater than the 60 Hz peak current-see Fig. 12. The worst case, at low line and max. overload input current is:

$$I_{PK(100kHz)} = \frac{I_{PK(60Hz)}}{D} = \frac{17}{.702} = 24.2A$$

Add to this one-half ΔI_L to obtain the absolute max. peak current through the switch, inductor, and rectifier: $24.2 + 3.6/2 = 26A$.

Compared to the boost converter, the flyback topology requires higher current and higher voltage devices and generates a lot more input noise because of the chopped waveform. In its favor, the flyback converter can operate with any input/output voltage ratio, can provide current limiting, and input/output isolation.

As discussed in the previous example, the boost converter amplifier gain at f_S was limited only by the criteria that the inductor current downslope must not exceed the oscillator ramp slope. The power circuit control-to-input current gain had a simple -1 slope from zero to f_S, making it very easy to compensate.

But with the flyback converter, the chopped switch current waveform will be averaged. This results in a lower crossover frequency, f_C, and lower gain-bandwidth for two reasons:

1. The large amplitude chopped current waveform must be integrated by the CA. The upslope of the resulting triangular waveform at the CA output must not exceed the oscillator ramp slope. (The inductor current downslope is not relevant.)
2. There is a zero (conventional left half-plane) in the control-to-input current gain characteristic. This zero moves with output current level. Loop gain crossover cannot be much higher than the lowest zero frequency.

The small-signal control-to-input gain of the flyback current loop power circuit (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\left(I_L + \frac{V_o}{sL}\right) \qquad (10)$$

This is the characteristic of a "normal" zero-a -1 slope with 90° phase lag below f_Z and flat gain with no phase shift above f_Z. The zero frequency may be calculated:

$$f_Z = \frac{V_o}{2\pi L I_L} \qquad (11)$$

Note that the zero moves inversely with inductor current and inductance value. This zero has a big effect on loop compensation. To obtain the best loop response, it is important that f_{Zmin} be as high as possible, by making the inductance small. Fortunately, with average current mode control, there is no need to worry about crossing into discontinuous operation. The limit on making the inductance too small is when the inductor ripple current becomes too large, increasing peak switch and rectifier currents an undesirable amount.

Using the specific values of this example, the power circuit gain is:

$$\frac{v_{RS}}{v_{CA}} = \frac{I_L}{200} - j\frac{960}{f}$$

The minimum zero frequency is 8 kHz, which occurs at 24.2A, the max. overload *inductor* current at 90V low line. The gain above f_Z is 0.12 (-18.4dB). The power circuit gain is shown in the Bode plot of Fig. 13.

Turning now to the current error amplifier (Fig. 11), the chopped input (switch) current waveform shown in Fig. 12 flows through R_S. The average value of this waveform, chopped at 100 kHz, is compared to the current program level across R_{CP} and amplified. Assume for the moment that C_{P2} is zero and C_{FZ} is shorted. The CA gain in the vicinity of 100 kHz is determined by integrator $(R_I+R_{P2})C_{FP}$. Averaging is accomplished because the DC gain is high, but the 100 kHz rectangular waveform with its harmonics is amplified relatively little. The rectangular waveform is converted into a triangular wave as shown in Fig. 12.
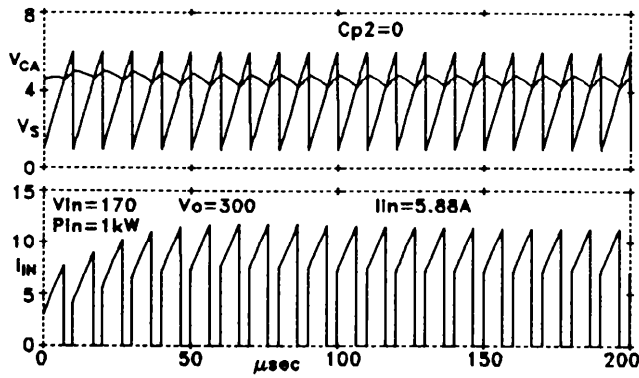
Fig. 12 - Flyback Regulator Waveforms

The optimum CA integtator gain at 100 kHz is the gain at which the maximum CA output upslope equals the oscillator ramp slope. This is the same principle used in the previous two examples, but in those cases the inductor (whose current was being controlled) did most of the averaging. The inductor did the integration to provide the triangular ripple current waveform and the CA gain was flat in the vicinity of f_S. But in this flyback preregulator example, the chopped *switch* current is being controlled so the averaging and the triangular waveshape are achieved by an integrating amplifier.

The upslope of the CA output occurs when the switch is off and the 100 kHz current waveform is at zero. The CA inputs are both at program voltage V_{CP}. V_{CPmax} equates to the max. overload peak 60Hz input current (17A) through R_S. Therefore, during the switch "off" time, the maximum current through $R = (R_I + R_{P2})$ i s :

$$I_{RImax} = \frac{V_{CPmax}}{R} = \frac{I_{INpk} R_S}{R}$$

The upslope of the CA output is determined by the current through R_I charging C_{FP}:

$$\text{max } CA \text{ Upslope} = \frac{I_{RImax}}{C_{FP}} = \frac{I_{INpk} R_S}{C_{FP} R_I}$$

$$Oscillator \ Ramp \ Slope = V_s/T_s = V_s f_S$$

Equating the slopes and solving for C_{FP}:

$$\frac{I_{INpk} R_S}{C_{FP} R} = V_s f_S$$

$$C_{FP} = \frac{I_{INpk} R_S}{V_s f_S R} \qquad (12)$$

Using the values from this example, and assuming $R = 10K$ ($R_I = 9K, R_{P2} = 1K$) :

$$C_{FP} = \frac{17 \times .025}{5 \times 0.1 \times 10^6 \times 10K} = 85 \, pF$$

The CA integrator gain may now be calculated and entered in the Bode plot:

$$G_{CA} = \frac{1}{2\pi f R C_{FP}} = \frac{187,000}{f} \qquad (13)$$

The compensation circuit as designed so far (with C_{P2} zero and C_{FZ} open) has high loop gain and is very stable only when the inductor current is high, maintaining the power circuit zero near the position shown in Fig. 13, so that its gain is flat at f_C. At lower current levels, the power circuit zero slides down to the right and
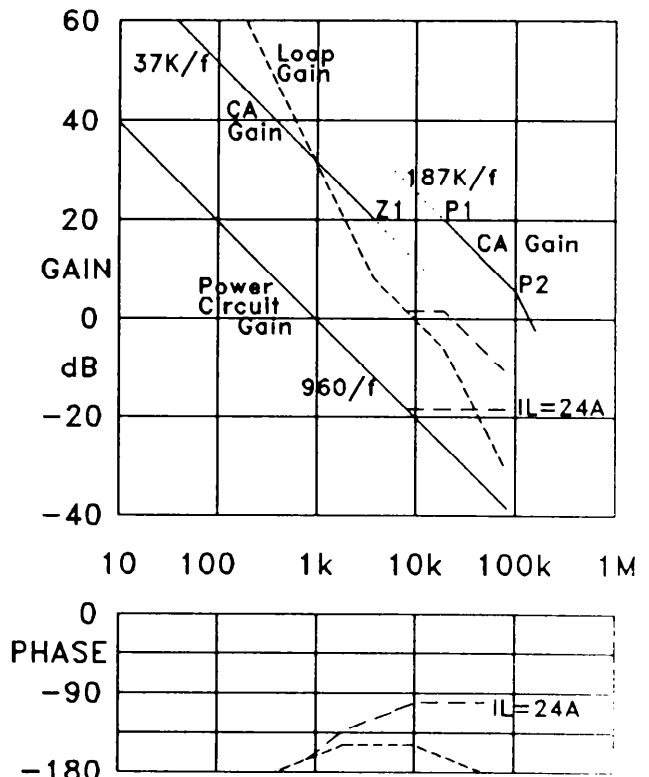

Fig. 13 - Flyback Regulator Bode Plot

the power circuit gain at f_c has a -1 slope. With the -1 slope of the CA gain, the overall current loop gain has a slope of -2 at crossover, and will ring excessively. It is necessary to add a pole-zero pair to the CA gain to reduce the slope to -1 in the vicinity of f_C. Offsetting the integrator gain by a factor of 5, as shown in the Bode plot, provides a phase bump which increases the actual phase margin to 42°, a slightly underdamped condition (the Bode *approximation* is 31°, as shown).

The offset factor of 5 is provided by $C_{FZ} = 4 \cdot C_{FP} = 340pF$. C_{FZ} and C_{FP} in parallel set the integrator gain at low frequencies to 37,000/f.

The location of the flat portion of the CA gain characteristic is determined by R_F. It is easiest to solve this graphically using the Bode plot. Ideally, Z1 and P1 should bracket the crossover frequency. *Simply slide the flat portion up and down between the integrator slopes until its gain is equal (but opposite in sign) to the power circuit gain at the same frequency as the center of the flat potion.* That frequency is the crossover frequency, f_C. In Fig 13, the CA gain in the flat portion is 10 (20dB). This is accomplished by:

$$R_F = 10R = 10(R_I + R_{P2}) = 100K \quad (14)$$

The precise value of R_F (and f_C) is not at all critical. The phase bump is broad, and the loop response is really determined by the integrator gain below f_C (37,000/f).

Finally, an additional pole $R_{P2}C_{P2}$ is placed at 100kHz to filter out noise spikes. This pole frequency is too high to significantly affect phase margin at crossover.

Referring back to Fig. 11 — when the current loop is closed, the voltage across current sense resistor V_{RS} equals the voltage across current programming resistor V_{RCP}. Programmed with a current source I_{CP}, the current gain of the closed current loop is identical to Eq. 9:

$$G = \frac{\hat{i}_L}{\hat{i}_{CP}} = \frac{\hat{v}_{RS}/R_S}{\hat{v}_{RCP}/R_{CP}} = \frac{R_{CP}}{R_S} \quad (15)$$

Just as in the previous examples, the closed loop current gain rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S. The moving zero of the flyback power circuit is hidden within the inner current loop, and is invisible to the outer voltage control loop. In fact-regardless of the power circuit topology-with average current mode control, the external characteristics of the current loops are identical: flat gain, rolling off with a single pole characteristic above the open loop crossover frequency.

Example 4: Buck Regulator Input Current: The buck regulator is sometimes used in high power factor preregulator applications. It can only function when V_O is less than V_{IN}, so the output bus voltage must be low. Normally, a low output voltage should be avoided, because the bus filter capacitor becomes large and expensive, but in applications such as telephone or battery charging this is not a problem and/or there is no choice. With 120V line input and 48 volt output bus, the input current will drop to zero for a substantial portion of each line cycle, each time the instantaneous line voltage goes below 48V. Third harmonic distortion will be 7 - 8% at low line, but the power factor of 0.99 is good enough for most applications.

Although the flyback topology might be used in the same low voltage output application, the buck topology operates with lower inductor current and lower peak current through the switch and rectifier. Peak voltages on the switch and rectifier are also much lower. But the flyback topology can provide line isolation in the preregulator by using a flyback transformer instead of simple inductor.

The buck circuit can be almost the same as the flyback circuit of Fig. 11, interchanging the inductor and the rectifier (cathode up).

The control loop design procedure is the same as for the flyback in Example 3. The buck regulator has the same left half-plane zero. In fact, the power circuit control-to-input gain equation is identical to Eq. 10 for the flyback circuit.

Controlling Average Rectifier Current

Peak current mode control has been used with great success in conventional power supplies using buck-derived topologies. It works well because peak current mode control actually controls inductor current, and the inductor is located in the output of all buck topologies. When boost or flyback topologies are used, peak current mode control functions poorly, because the wrong current is controlled-the inductor current is not in the output. Although peak current mode control eliminates the inductor from the small-signal characteristic of the outer loop, the right half-plane zero present in boost and flyback outputs remains to plague outer loop compensation.

In boost or flyback circuits, the diode is in the output side, and ideally the diode current should be controlled, not inductor current. This is no problem for average current mode control. Its integrating current error amplifier can average the rectangular diode current waveform in the same way that it averages the switch current in the input of the buck or flyback preregulators discussed earlier. The right half-plane zero forces a lower current loop crossover frequency, but the RHP zero is "buried" within the current loop. The outer voltage control loop sees only a flat gain characteristic with a single pole roll-off at the crossover frequency-just the same as all the other topologies previously discussed. A flyback circuit using average current mode control is shown in Figure 14.
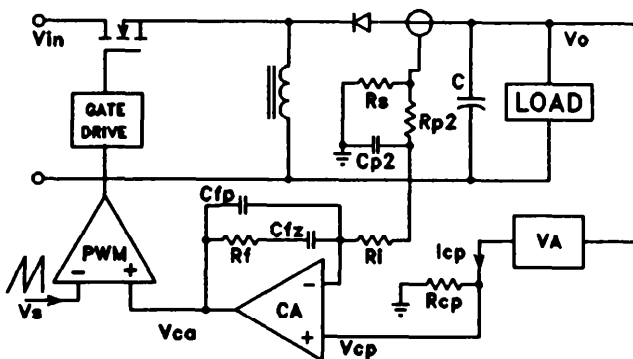

Fig. 14 - Flyback Output Current Control

The circuit is almost identical to the flyback preregulator of Fig. 11, except output current

is sensed and controlled.

The small-signal control-to-output gain of the flyback current loop power circuit (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\left[\frac{V_O}{sL} - I_L\right] \qquad (16)$$

The same equation applies to controlling the output current of a boost circuit. Note the similarity with Eq. 10 for flyback or buck input current control. In Eq. 16, low frequency gain depends on V_{IN} rather than V_O, but more importantly, the inductor current I_L has a minus sign, which represents 180° phase lag above the zero frequency. This is the characteristic of a right half-plane zero, and it makes the loop compensation much more difficult. It is usually necessary to cross over at a frequency one half to one fourth of the RHP zero frequency in order to cross over with adequate phase margin. This results in lower closed loop bandwidth for the current loop than the previous examples. However, once this is accomplished, the RHP zero does not appear in the outer loop.

It is very important to make the inductance small to achieve the highest possible RHP zero frequency. Fortunately, average current mode control allows the mode boundary to be crossed. This permits a much smaller inductance than with peak current mode control, resulting in a much higher RHP zero frequency and higher crossover frequency.

Current Sensing

One important advantage of having a high gain current error amplifier is that it permits a very small current sense resistor value resulting in low power dissipation. The CA can make up for the gain lost with the small resistor.

In many applications, however, using a current sense resistor in the direct path of the current to be measured is not practical. The tiny R_S value may be difficult to implement, and the power dissipation in a practical sense

resistor is too great. Often, the R_S circuit location is at a large potential difference from the control circuit. This is especially a concern when current must be sensed on the other side of the isolation boundary.

A current sense transformer (C.T.) can provide the necessary dielectric isolation and eliminate the need for an extreme low-value resistor. As shown in Fig. 15, this technique
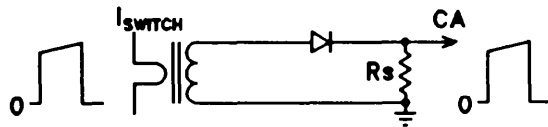

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works well for average current mode control when the current to be sensed and averaged is a pulse which returns to zero within each switching period-such as switch current (buck or flyback input current) or diode current (boost or flyback output current). Although "transformers can't couple DC", a **C.T.** does couple the entire instantaneous current waveform including its DC component if the core is reset to zero baseline each time the pulse goes to zero.

Total reset requires the same volt-seconds (of opposite sign) that were applied to "set" the core. At duty cycles approaching 1.0-which can occur temporarily with most topologies-the time available for reset may be only a tiny fraction of the switching period. Achieving total reset in a short time requires a large backswing of voltage across the C.T., so don't use low voltage diodes to couple the C.T. to R_S.

With a boost converter controlling input current in a high power factor preregulator application, a current sense resistor easily ties in directly with the control circuit, as shown in Fig. 6. Nevertheless, many designers would prefer to use a current transformer to minimize power loss and allow the use of a much higher R_S value. However, since the input current of a boost converter *is* the inductor current, the input current never goes to zero when operating in the continuous mode. Therefore, a C.T.. can't be used to sense input current of a boost

converter because the DC value is lost, and the C.T. cannot reset-it will saturate. The same problem occurs in a buck regulator circuit, where the C.T. can't directly sense average output (inductor) current.

The answer to this problem is to use *two* C.T.s–one sensing switch current, the other sensing diode current. By summing their outputs as shown in Fig. 16, the true inductor current is reconstituted. Each C.T. has plenty of time to reset.
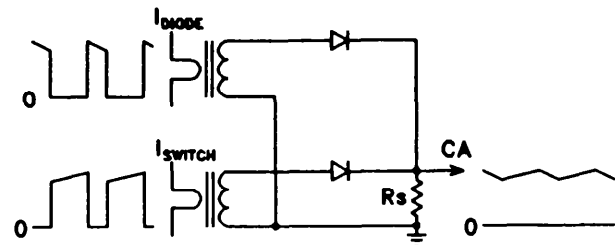
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Using Current Sense Transformers:
It is not difficult to achieve excellent results using low cost commercially available pulse transformers. A current sense "inductor" such as Pulse Engineering 51688 is a toroidal core wound with 200 secondary turns for a secondary inductance of 80 mH. A 0.18" hole is provided to slip the primary wire through.

The pulse voltage across the windings of a current transformer generates a magnetizing current which starts at zero and increases fairly linearly with time. The magnetizing current subtracts from the pulse current delivered to the secondary. Initially, the current through R_S is precisely I_{PRI}/N, but as time passes, the secondary current drops off more rapidly than it should, This effect is called "droop". It is usually not a problem if certain precautions are observed. The amount of current droop through the current sense resistor can be calculated:

$$\Delta I_{PRI(droop)} = \frac{N_S}{N_P} \frac{V_S}{L_S} \Delta t \qquad (17)$$

where N is the turns ratio, V_S the voltage across the secondary, L_S the secondary inductance and Δt is the max. pulse width. As the

equation shows, droop is minimized by maximizing secondary inductance-use the largest you can get. Don't use a large R_S value to obtain a large secondary voltage-its not necessary and makes reset more difficult. Make the turns ratio as low as possible by using two or three primary turns if space allows. Don't reduce the turns ratio by reducing the secondary turns-this is counter-productive because the inductance goes down with the turns *squared.*

For example, consider the flyback input current preregulator of Fig. 11, using a current transformer in series with switch instead of the 0.025Ω sense resistor shown. Using the Pulse Engineering #51688 current sense inductor with one turn primary, the turns ratio is 1:200. Secondary inductance is 80 mH. The 24A max. overload pulse current becomes a 0.12A current pulse on the secondary side. A 10Ω sense resistor will have a max. voltage of 1.3V sent to the CA, and the max. secondary voltage including diode forward drop is 2.0V. The maximum pulse width is 7.02μsec.

Applying these values to Eq. 17:

$$\Delta I_{PRI(droop)} = \frac{200}{1} \frac{2.0}{80\times10^{-3}} 7\times10^{-6} = .035A$$

Only 35mA droop out of 24A isn't bad!

When two C.T.s are used-one on either side of isolation boundary-their turns ratios must be proportioned the same as the power transformer pri/sec turns ratio so that currents through R_S will be equalized.

All of the equations containing R_S given earlier in this paper assume the sense resistor is measuring current directly. When using a current sense transformer, reflect the actual R_S on the C.T. secondary side into the primary by substituting $R_S N_P/N_S$.

References:

[1] S. Hsu, A. Brown, L. Rensink, R.D. Middlebrook, "Modelling and Analysis of Switching DC-to-DC Converters in Constant Frequency Current Programmed Mode, *"IEEE PESC Proceedings,* 1979

[2] R.D. Middlebrook, "Topics in Multiple-Loop Regulators and Current-Mode Programming" *IEEE PESC Proceedings,* June 1985

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