High-Performance Analog Products

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Impact of sampling-clock spurs on ADC performance

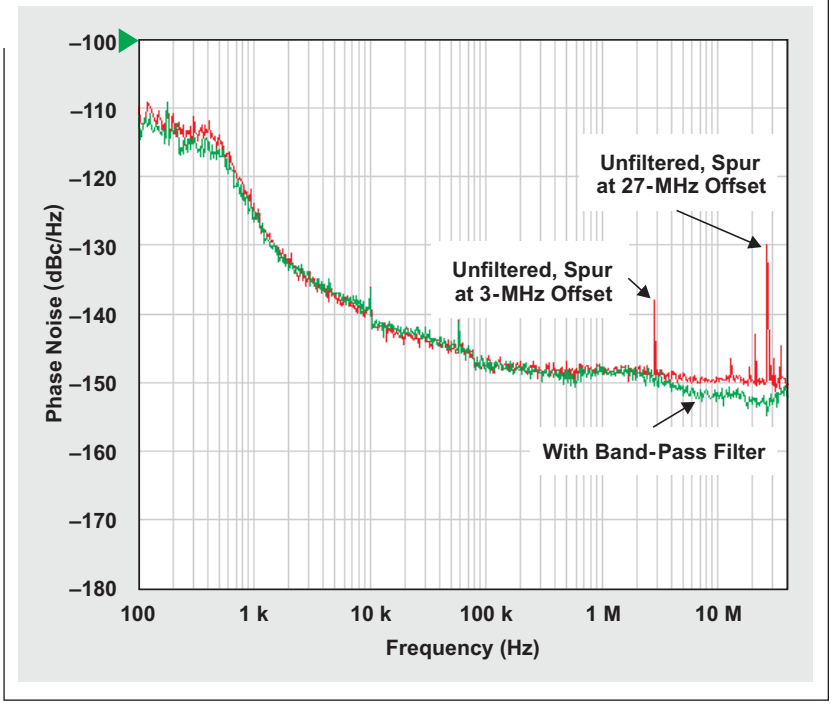
By Thomas Neu
Analog Field Applications Engineer

Introduction

As modern, high-speed analog-to-digital converters (ADCs) push the spurious-free dynamic range (SFDR) beyond the 100-dB barrier, the demand for a high-quality sampling clock has become greater than ever. Traditionally, system engineers focused mainly on the clock quality when they were trading off the signal-to-noise ratio (SNR) against the input-signal frequency in undersampling applications. As tougher system requirements such as multicarrier GSM emerge and are starting to demand dynamic ranges in excess of 80 dB over a wide bandwidth, system designers try to eliminate any possible SFDR degradation, such as the spur feedthrough from a distorted sampling clock.

Spurs on the sampling clock as low as –90 dBc can significantly impact the SFDR of the data converter. These low-level spurs can be very difficult to track down because they can have a variety of different origins. They can be generated from crosstalk with an adjacent digital circuit that occurs due to layout constraints, or they can occur simply because the clock source is not properly filtered. An example of improper filtering is shown in Figure 1, which compares two LVDS outputs of the Texas Instruments (TI) CDCE72010, one unfiltered and one with a band-pass filter. The spur reduction of the filtered output is clearly visible.

Figure 1. Phase noise of CDCE72010's filtered and unfiltered LVDS outputs



This article will discuss how spurs on the sampling clock get translated into the output spectrum of the data converter. It will also investigate how the spur amplitude changes with different input frequencies. More and more system designers are moving to an undersampling architecture, and the spur amplitude is highly dependent upon input frequency, as will be shown later. This article will also show how to estimate the SNR degradation caused by the sampling-clock spurs.

Sampling theory

The spurs that result from sampling a data converter with a distorted clock are best described by the relationship of their frequency and amplitude components to the same components of the sampled input signal. In order to derive that relationship, one has to start with the basic sampling theory. Let's consider the setup shown in Figure 2, where the input signal is

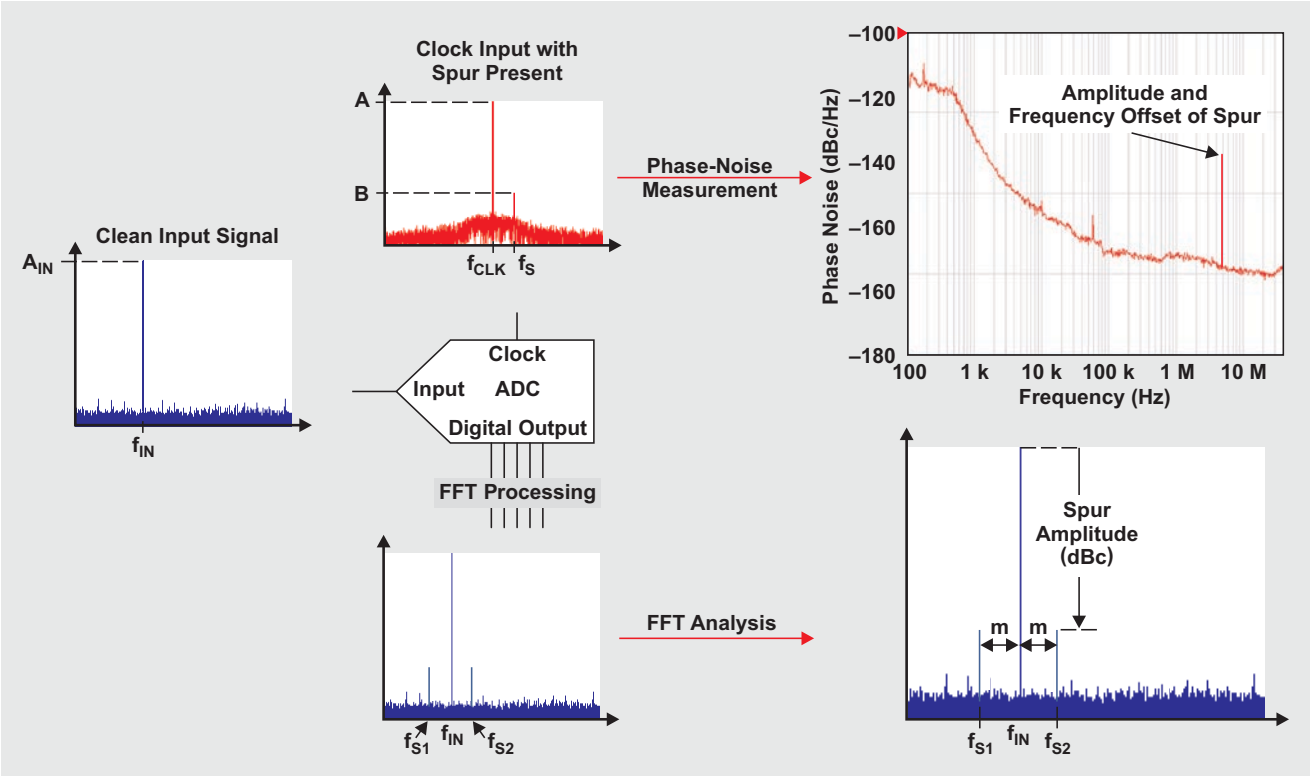
$$x(t) = A_{IN} \times \sin(\omega_{IN} t),$$

and the clock input with a spurious component is

$$y(t) = A \times \sin(\omega_{CLK} t) + B \times \sin(\omega_S t).$$

The quality of the sampling clock can easily be evaluated with a phase-noise analyzer. It displays the clock's phase noise versus frequency offset from the carrier, which is very helpful when the clock jitter is calculated to determine the SNR of the receiver. The phase-noise plot displays any spurious component on the clock signal, referencing its frequency offset and spur amplitude, S_X, to the main signal. If the amplitude is normalized in dBc/Hz, care must be

Figure 2. Setup with input signal, clock, and clock spur



taken to extract it with the resolution bandwidth of the instrument in that measurement:

$$\text{Amplitude (dBc)} = S_X \text{ (dBc/Hz)} + 10\log(\text{Resolution Bandwidth})$$

Due to the presence of the spur, the original sampling instant, or zero crossing of the clock, has shifted slightly by ΔT. Now the sampling instant, $y(t) = 0$, can be solved for:

$$y(t) = A \times \sin[\omega_{CLK}(t+\Delta T)] + B \times \sin[\omega_S(t+\Delta T)] = 0$$

$$y(t) = A \times \sin(\omega_{CLK}t) \times \cos(\omega_{CLK}\Delta T) + A \times \cos(\omega_{CLK}t) \times \sin(\omega_{CLK}\Delta T) + B \times \sin(\omega_S t) \times \cos(\omega_S \Delta T) + B \times \cos(\omega_S t) \times \sin(\omega_S \Delta T) = 0$$

Assuming that $B << A$ and $\Delta T \approx 0$ results in: $\cos(\omega_{CLK}\Delta T) \approx 1$ $\sin(\omega_{CLK}\Delta T) \approx \omega_{CLK}\Delta T$

$\cos(\omega_S \Delta T) \approx 1$ $\sin(\omega_S \Delta T) \approx \omega_S \Delta T$

The ideal sampling instant is $t = 0$, hence: $\sin(\omega_{CLK}t) = 0$ $\cos(\omega_{CLK}t) = 1$ $\cos(\omega_S t) = 1$

Substituting these results into $y(t) = 0$ produces:

$$y(t) = A \times \underbrace{\sin(\omega_{CLK}t)}_{0} \times \underbrace{\cos(\omega_{CLK}\Delta T)}_{1} + A \times \underbrace{\cos(\omega_{CLK}t)}_{1} \times \underbrace{\sin(\omega_{CLK}\Delta T)}_{\omega_{CLK}\Delta T} + B \times \sin(\omega_S t) \times \underbrace{\cos(\omega_S \Delta T)}_{1} + B \times \underbrace{\cos(\omega_S t)}_{1} \times \underbrace{\sin(\omega_S \Delta T)}_{\omega_S \Delta T} = 0$$

$$y(t) = A \times \omega_{CLK}\Delta T + B \times \sin(\omega_S t) + B \times \omega_S \Delta T = 0$$

Then ΔT can be solved for: $\Delta T = -\dfrac{B \times \sin(\omega_S t)}{A \times \omega_{CLK} + B \times \omega_S}$. Assuming that $A >> B$ results in $\Delta T = -\dfrac{B \times \sin(\omega_S t)}{A \times \omega_{CLK}}$.

Next, the input signal, $x(t) = A_{IN} \times \sin(\omega_{IN}t)$, is sampled at the zero crossing, $t + \Delta T$, of the non-ideal clock:

$$x(t) = A_{IN} \times \sin(\omega_{IN}T) = A_{IN} \times \sin\left[\omega_{IN}(t+\Delta T)\right] = A_{IN} \times \sin(\omega_{IN}t) \times \underbrace{\cos(\omega_{IN}\Delta T)}_{1} + A_{IN} \times \cos(\omega_{IN}t) \times \underbrace{\sin(\omega_{IN}\Delta T)}_{\omega_{IN}\Delta T}$$

This results in $x(t) = \underbrace{A_{IN} \times \sin(\omega_{IN} t)}_{\text{Ideal Sample}} + \underbrace{A_{IN} \times \cos(\omega_{IN} t) \times \omega_{IN} \Delta T}_{\text{Error Sample}}$.

Focusing on the error sample and substituting ΔT produces:

$$x(t) = A_{IN} \times \omega_{IN} \times \frac{-B \times \sin(\omega_S t)}{A \times \omega_{CLK}} \cos(\omega_{IN} t) = \underbrace{A_{IN} \times \omega_{IN} \times \frac{B}{A \times \omega_{CLK}} \times \frac{1}{2}}_{\text{Scale Factor of Spur Amplitude}} \underbrace{\left\{ \sin\left[(-\omega_S + \omega_{IN}) \times t\right] + \sin\left[(-\omega_S - \omega_{IN}) \times t\right] \right\}}_{\text{Two Frequency Products: } -\omega_S + \omega_{IN} \text{ and } -\omega_S - \omega_{IN}}$$

Therefore, it can be observed that each spurious component of the sampling clock generates two spurs, S1 and S2, in the data converter with amplitude and frequencies relative to the input signal as follows.

S1 and S2 amplitude: $\frac{B}{A} \times \frac{\omega_{IN}}{2 \times \omega_{CLK}} = \frac{B}{A} \times \frac{f_{IN}}{2 \times f_{CLK}}$ or, in terms of decibels,

$$= B - A + 20 \log\left(\frac{f_{IN}}{2 \times f_{CLK}} \right).$$

S1 and S2 frequencies: $f_{S1} = -f_S - f_{IN}$

$f_{S2} = -f_S + f_{IN}$

The resulting spurs can be shifted by one clock period, $2\pi/T = f_{CLK}$, and considering $f_S - f_{CLK} = m$ yields:

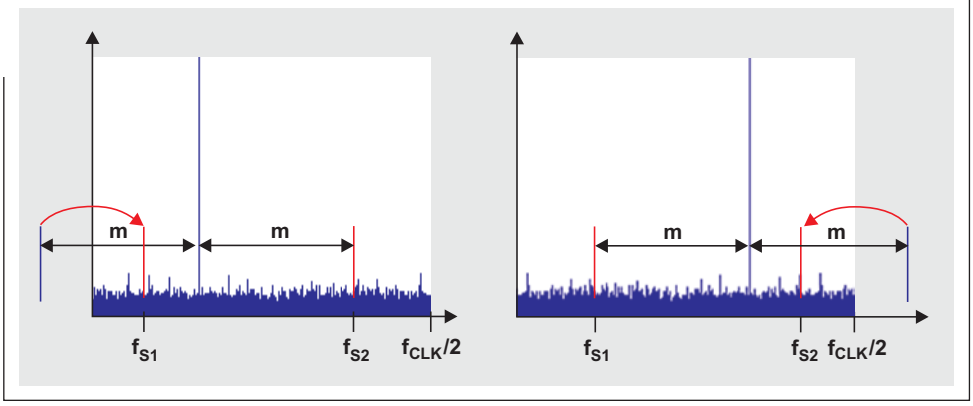
$f_{S1} = -f_S - f_{IN} + f_{CLK} = -f_{IN} + f_{CLK} - f_S = -(f_{IN} - f_{CLK} + f_S) = -(f_{IN} + m) = f_{IN} + m$

$f_{S2} = -f_S + f_{IN} + f_{CLK} = +f_{IN} + f_{CLK} - f_S = f_{IN} - m$

These equations show that the frequencies of the generated spurs will be centered around the input signal and offset by the distance m, which is the difference between the clock frequency and the clock-spur frequency. The amplitude of the generated spurs, on the other hand, is highly dependent upon the input frequency. For every doubling of the input frequency (e.g., f_{IN} = 20 MHz versus f_{IN} = 10 MHz), the spur amplitude increases by 6 dB! Hence, as system designers consider sampling in higher Nyquist zones, this relationship becomes very important to them.

Sometimes the fast Fourier transform (FFT) plot can be a bit misleading when one is trying to trace spurs back to their origins. If the clock spur is relatively far from the clock frequency, the generated spurs of the ADC can get pushed outside the plot's boundaries—either to negative frequencies or beyond $f_{CLK}/2$. The spurs then alias back in-band and generate an asymmetric FFT plot, as demonstrated in Figure 3.

Figure 3. Spurs pushed outside the FFT band and aliased back in-band



Measurements

To further demonstrate the impact of the spur's frequency and amplitude, the following experiment was set up (see Figure 4). A low-jitter-signal generator was used to provide a sine-wave input signal to TI's ADS5463 evaluation module (EVM). The ADC input was sampled with a 122.88-MHz clock, and a power combiner and third signal generator were used to mix a spur into the clock's frequency. This way the frequency and amplitude of the spur could easily be adjusted. The spur's amplitude and frequency were verified with a phase-noise analyzer.

For the first experiment, the spur generator was set up to output a tone with a frequency of 102 MHz and an amplitude of –30 dBm. The power combiner reduced the clock and spur signals by about 3 dB. The phase-noise analyzer showed the amplitudes of the clock and spur at –9 dBm and about –33 dBm, respectively, with an offset (m) of about 20.9 MHz (122.88 MHz – 102 MHz) as illustrated in the screen capture in Figure 5. As previously derived, this setup generated two spurs with a spur-amplitude scale factor of

$$B - A + 20\log\left(\frac{f_{IN}}{2\times f_{CLK}}\right) = -33\ \text{dBm} - (-9\ \text{dBm}) + 20\log\left(\frac{10\ \text{MHz}}{2\times 122.88\ \text{MHz}}\right) = -51.8\ \text{dBc}$$

and spur frequencies of

$f_{S1} = f_{IN} + m = 10\ \text{MHz} + 20.9\ \text{MHz} = 30.9\ \text{MHz}$ and

$f_{S2} = f_{IN} - m = 10\ \text{MHz} - 20.9\ \text{MHz} = -10.9\ \text{MHz}$.

Figure 4. Test setup to mix a spur and clock signal

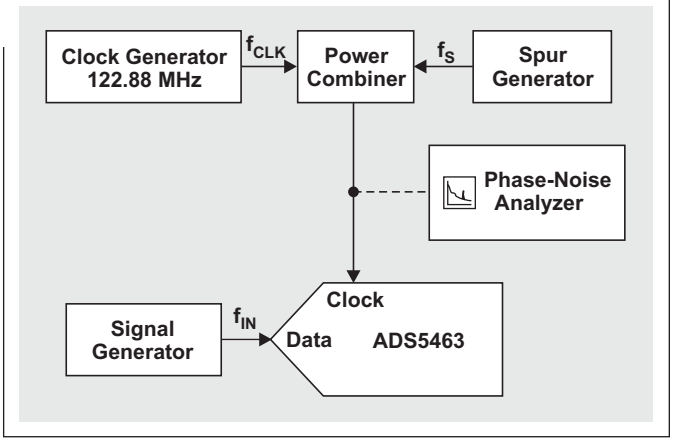
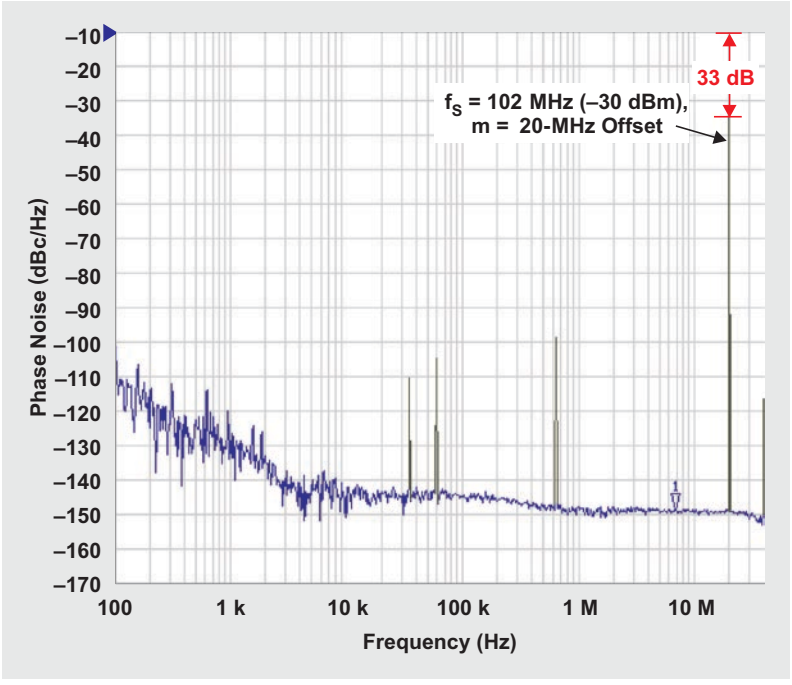


Figure 5. Phase-noise plot of 102-MHz spur with –33-dBm amplitude

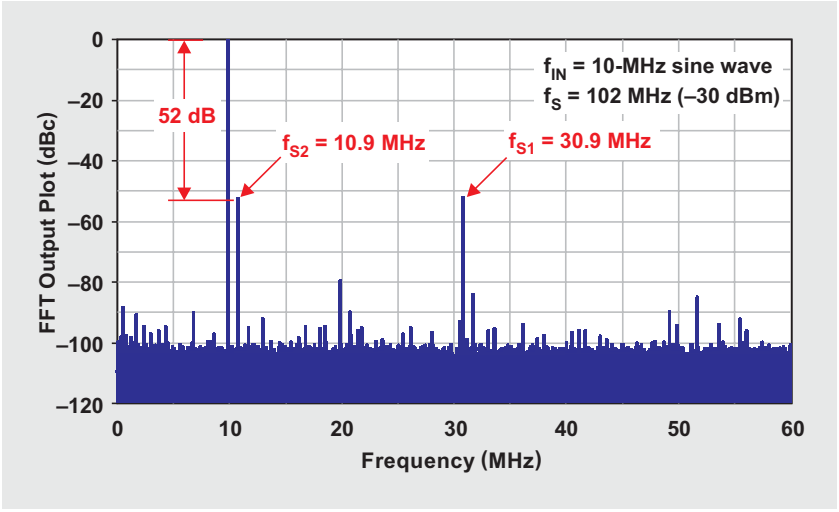


The resulting FFT plot of the ADS5463 output is shown in Figure 6. The generated spurs are about 52 dB lower than the input signal and are located at 10.9 and 30.9 MHz. This matches the calculated values very closely.

Next, the spur amplitude was lowered from –30 dBm to –40 dBm. It was expected that the S1 and S2 spur amplitudes would drop by 10 dB as well. This was confirmed with the FFT plot of the ADS5463 output, as illustrated in Figure 7. The frequencies of the spurs stayed the same.

As discussed previously, the spur amplitude is highly dependent upon the frequency of the input signal. To further illustrate this, the frequency of the input signal was increased from 10 MHz to 100 MHz. This changed the spur-amplitude scale factor to

Figure 6. FFT output of 102-MHz, –30-dBm clock spur



$$B - A + 20\log\left(\frac{f_{IN}}{2\times f_{CLK}}\right) = -33\text{ dBm} - (-9\text{ dBm}) + 20\log\left(\frac{100\text{ MHz}}{2\times 122.88\text{ MHz}}\right) = -24 - 7.8 = -31.8\text{ dBc}$$

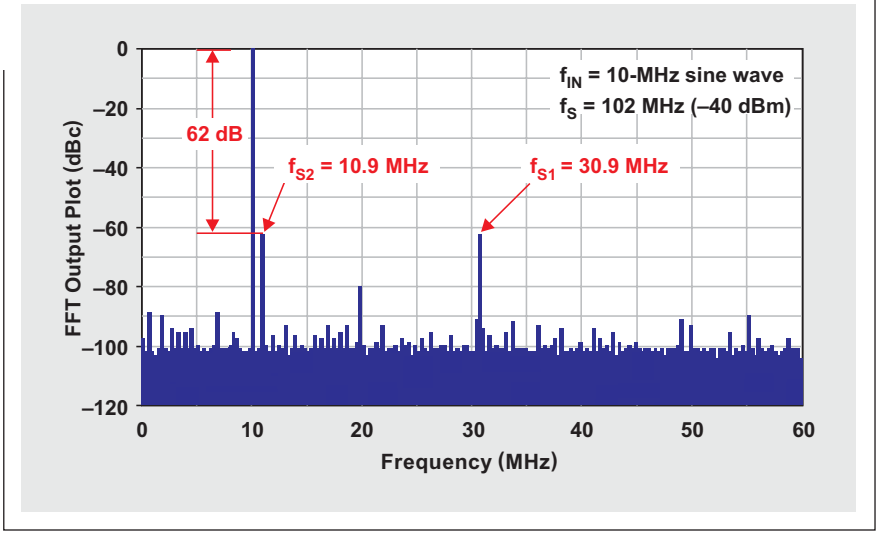
and the frequencies of the two spurs to $f_{S1} = -f_S + f_{IN} = -102\text{ MHz} + 100\text{ MHz} = -2\text{ MHz}$ and

$f_{S2} = -f_S - f_{IN} = -102\text{ MHz} - 100\text{ MHz} = -202\text{ MHz}$.

Aliasing them back in-band generated two spurs, $f_{S1} = -2\text{ MHz} = +2\text{ MHz}$ and

$f_{S2} = -202\text{ MHz} + (2\times 122.88\text{ MHz}) = 43.8\text{ MHz}$.

Figure 7. FFT output of 102-MHz, –40-dBm clock spur



This was also confirmed with the FFT plot of the ADS5463 output (see Figure 8).

For the last experiment, a comparison of spur frequencies was made with the clock frequency set at 102 MHz and at 132 MHz. The spur amplitude was set to –30 dBm, and the input signal was set to 10 MHz. These settings caused the spur-frequency offset (m) to change from about 20.9 MHz to about 9.1 MHz, respectively. Two new spur frequencies resulted:

$f_{S1} = f_{IN} + m = 10\ MHz + 9.1\ MHz = 19.1\ MHz$

$f_{S2} = f_{IN} - m = 10\ MHz - 9.1\ MHz = 0.9\ MHz$

Once again, this correlated very well with the FFT output plot from the ADS5463, as illustrated in Figure 9.

Practical example

Let's go back and analyze the case of the CDCE72010, mentioned earlier under "Introduction." This device's low-jitter phase-locked loop was configured to drive the TI ADS5483 with LVDS outputs at 122.88 MSPS. No filter was placed between the outputs of the CDCE72010 and the clock input of the ADS5483. This way the full effect of the clock spurs in a real-world design can be observed.

Figure 8. FFT output of 102-MHz, –30-dBm clock spur

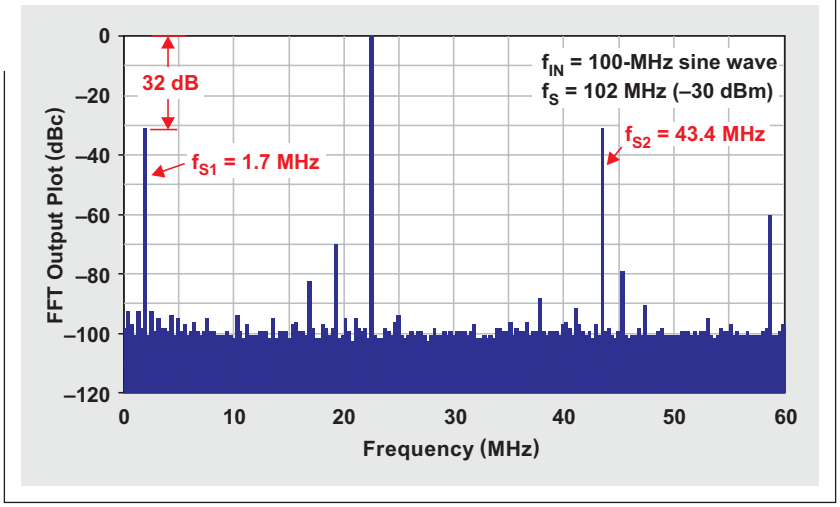
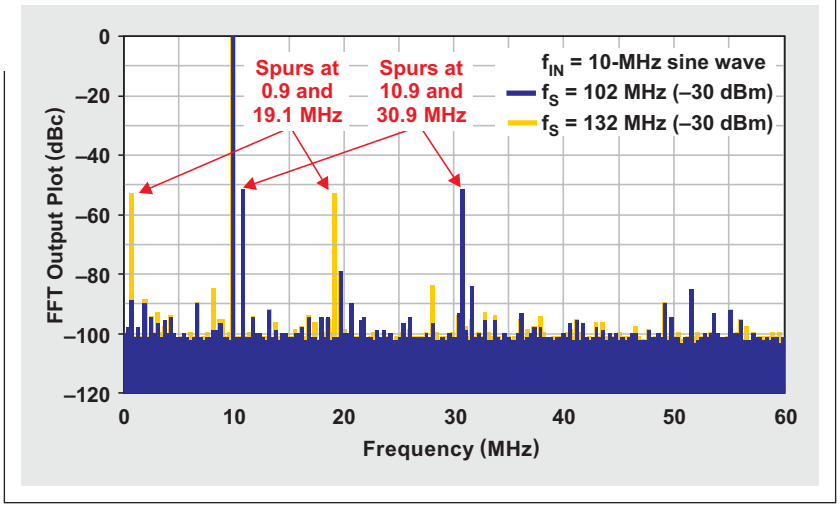


Figure 9. FFT output of –30-dBm clock spur at 132 MHz versus 102 MHz



The phase-noise plot of the unfiltered CDCE72010 in Figure 10 shows two spurs that will impact the SFDR performance of the ADS5483.One spur (S1) is offset about 27 MHz with an amplitude of about –130 dBc/Hz; the other spur (S2) is offset about 3 MHz with an amplitude of about –138 dBc/Hz. The actual spurs are 6 dB lower than shown in the plot because the phase-noise analyzer sums the spurs of the two sidebands together.

The amplitudes of the two spurs can be converted from dBc/Hz to dBc as described before:

$$\text{For S1, } 136 \text{ dBc/Hz} = -136 \text{ dBc} + 10\log(27 \text{ MHz} \times 1\%)$$
$$= -136 \text{ dBc} + 54.4 \text{ dB}$$
$$= -81.6 \text{ dBc}.$$
$$\text{For S2, } -144 \text{ dBc/Hz} = -144 \text{ dBc} + 10\log(3 \text{ MHz} \times 1\%)$$
$$= -144 \text{ dBc} + 45 \text{ dB}$$
$$= -99 \text{ dBc}.$$

These results can be used to calculate the spur amplitudes of the ADC output spectrum:

$$S1 = 81.6 \text{ dBc} + 20\log\left(\frac{100 \text{ MHz}}{2 \times 122.88 \text{ MHz}}\right)$$
$$= -81.6 \text{ dBc} - 7.8 \text{ dB}$$
$$= -89.4 \text{ dBc}$$
$$S2 = -99 \text{ dBc} + 20\log\left(\frac{100 \text{ MHz}}{2 \times 122.88 \text{ MHz}}\right)$$
$$= -99 \text{ dBc} - 7.8 \text{ dB}$$
$$= -106.8 \text{ dBc}$$

These amplitudes match the measured spur amplitudes of the ADC output spectrum fairly well (within 1 to 2 dB), as shown in Figure 11.

Figure 10. Phase-noise plot of CDCE72010's unfiltered LVDS output

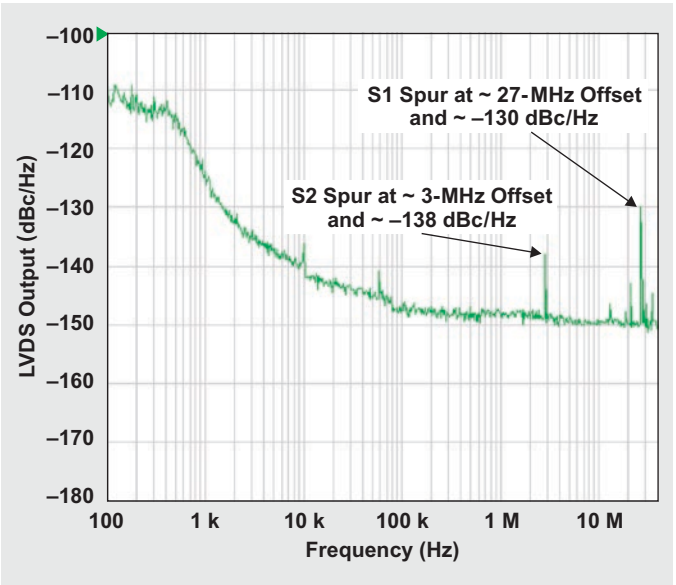


Figure 11. FFT output with 100-MHz input and a 122.88-MHz LVDS clock

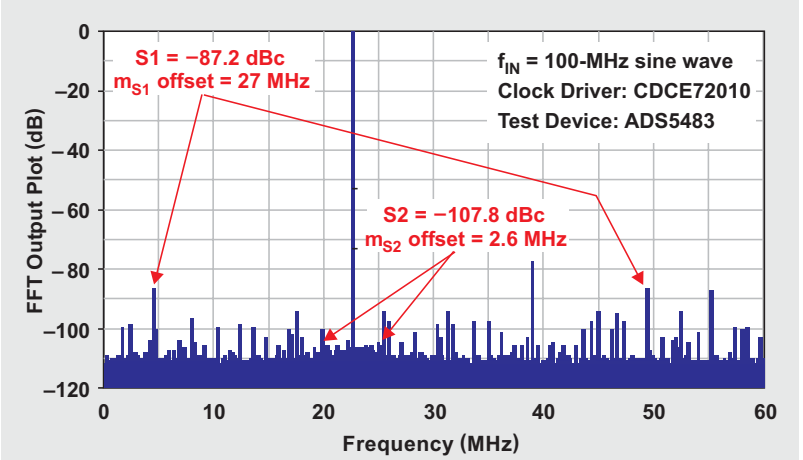
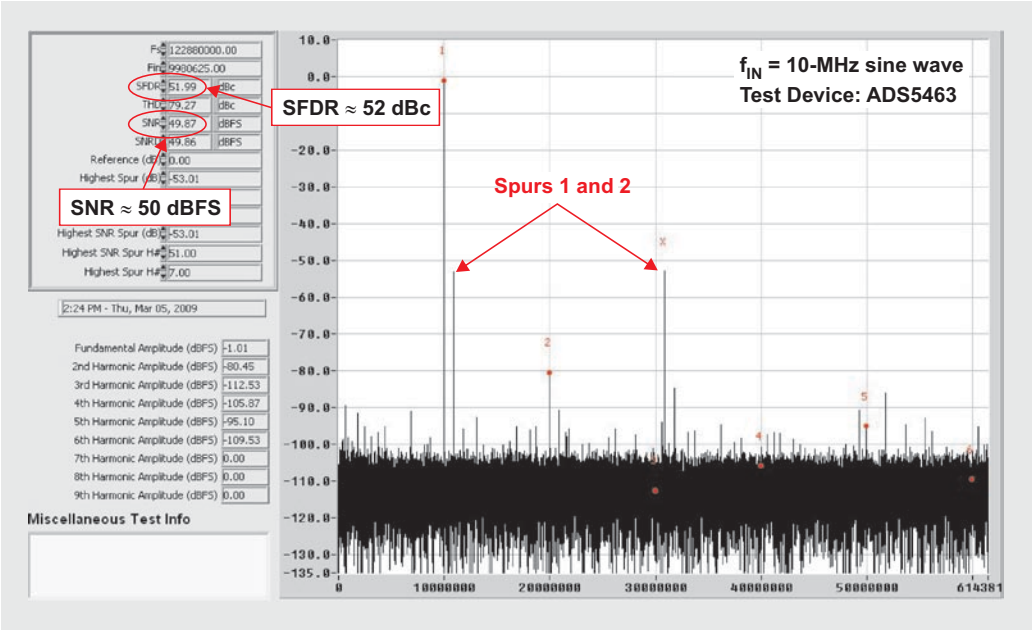


Figure 12. FFT output with 122.88-MHz clock and a 102-MHz, –30-dBm spur



Impact of clock spurs on SNR

Besides reducing the SFDR, spurs on the clock also impact the SNR of the data converter. Since the spurs are at a fixed frequency, they are considered deterministic jitter (DJ); and they contribute to the overall clock jitter, which in turn highly impacts the SNR.

The peak-to-peak DJ from the clock spur can be approximated by

$$DJ_{PP} \approx \frac{2\times10^{\frac{S_X(dBc)}{20}}}{\pi\times f_{CLK}},$$

where S_X (dBc) is the spur amplitude in dBc. The RMS jitter can be calculated as

$$DJ_{RMS} \approx \frac{DJ_{PP}}{14}.$$

As in the first experiment, with the measured amplitude of the spurs at –33 dBm and that of the clock at about –10 dBm, the relative spur amplitude is roughly

$$-33\text{ dBm} - (-10\text{ dBm}) = -23\text{ dBc}.$$

Substituting –23 dBc into the formula for DJ_{RMS} yields

$$DJ_{RMS} \approx \frac{DJ_{PP}}{14} = \frac{1}{14}\times\frac{2\times10^{\frac{-23}{20}}}{\pi\times122.88\text{ MHz}} = 26\text{ ps}.$$

Since there are two spurs with a 20-MHz offset, the 26-ps DJ of each spur can be summed together for a total DJ of about 52 ps.

For calculating the SNR of the data converter, the DJ needs to be added to the phase noise of the clock and the aperture jitter of the ADC. However, in this case, the DJ far exceeds the other two jitter components. Therefore, the resulting SNR can be calculated with a jitter of about 52 ps (f_{IN} = 10 MHz), which is approximately 50.5 dBFS.

The resulting FFT plot of this setup with the ADS5463 is shown in Figure 12. The plot clearly shows the two resulting spurs with an amplitude of –52 dBc and an SFDR of about –52 dBc. The SNR ≈ 50 dBFS, which matches the calculated value very well.

Conclusion

This article has shown that spurs on the ADC sampling clock can significantly degrade the overall system SFDR as well as the SNR. This effect gets amplified even more in undersampling applications where the signal input is moved to higher frequencies than those traditionally used for baseband input. Therefore, it can be concluded that a filtered, high-quality sampling clock is necessary for system engineers who are trying to achieve maximum data-converter performance.

Related Web sites

dataconverter.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with ADS5463, ADS5483, or CDCE72010

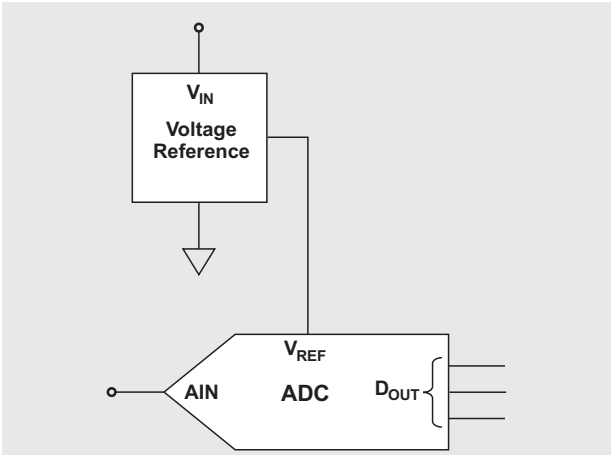
How the voltage reference affects ADC performance, Part 2

By Miro Oljaca, *Senior Applications Engineer,*
and Bonnie Baker, *Senior Applications Engineer*

Introduction

This article is Part 2 of a three-part series that investigates the design and performance of a voltage-reference system for a successive-approximation register (SAR) analog-to-digital converter (ADC). A simplified version of this system is shown in Figure 1. When a design uses an ADC in this system, it is critical to understand the voltage-reference path to the converter. Part 1 (see Reference 1) examined the fundamental operation of an ADC independent of the voltage reference, and then analyzed the performance characteristics that have an impact on the accuracy and repeatability of the system. Part 2 looks at the key characteristics of the voltage-reference block in Figure 1 and the reference's possible impact on the ADC's performance. Part 2 also shows how to design an appropriate external reference for 8- to 16-bit ADCs. Part 3, which will appear in a future issue of the *Analog Applications Journal*, will investigate the impact of the voltage-reference buffer and the capacitors that follow it, discuss how to ensure that the amplifier is stable, and provide a reference design that is appropriate for ADCs with 16+ bits.

Figure 1. Voltage-reference system for SAR ADC

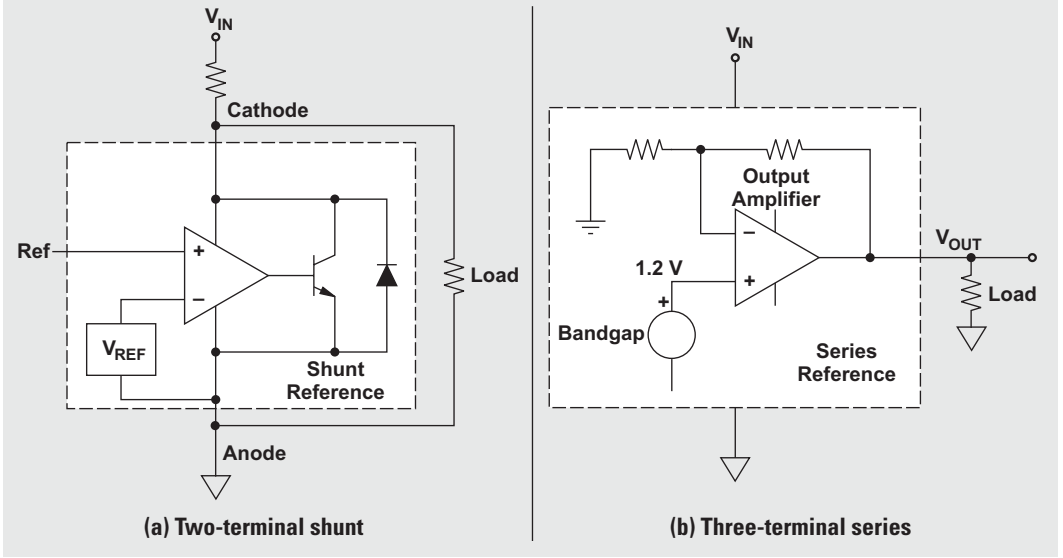


Choosing the correct V_{REF} topology

Voltage references are available in two-terminal shunt or three-terminal series configurations (see Figure 2). Figure 2a shows a two-terminal shunt voltage reference, in which the entire IC chip of the shunt reference operates in parallel to its load. With a shunt voltage reference, an input voltage is applied to the resistor that is connected to the cathode. The typical initial voltage accuracy of this device can be as low as 0.5% or range up to 5%, with a temperature coefficient of approximately 50 to 100 µV/°C. The shunt voltage reference can be used to create positive, negative, or floating reference voltages.

The three-terminal series voltage reference (Figure 2b) operates in series with its load. An internal bandgap voltage, in combination with an internal amplifier, creates the output voltage of this reference. The series voltage reference produces an output voltage between the output and ground while providing the appropriate output current to

Figure 2. Voltage-reference configurations



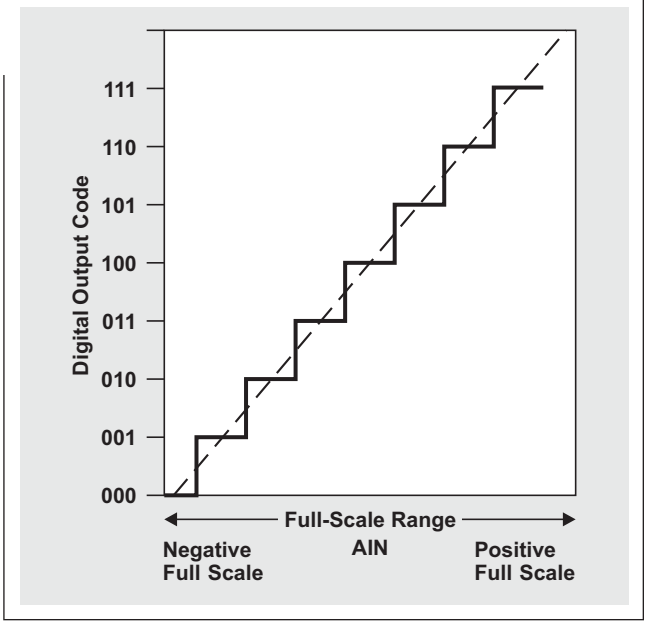
the external load. As the load current increases or decreases, the series reference maintains the voltage at V_{OUT}.

The typical initial voltage accuracy of a series-reference device can be as low as 0.05% or range up to 0.5%, with temperature coefficients as low as 2.5 ppm/°C. Because of the series reference's superior initial output voltage and overtemperature performance, this type of device would be used to drive the reference pins of precision ADCs. Beyond 8 or 14 resolution bits, where the size of the least significant bit (LSB) is respectively 0.4% and 0.006%, an external series voltage reference ensures that the intended precision of the converter can be achieved.

Another common application for series voltage references is sensor conditioning. In particular, a series voltage reference is useful in bridge-sensor applications as well as applications that have thermocouples, thermopiles, and pH sensors.

The initial accuracy of the series voltage reference in an ADC application (as in Figure 1) provides the general reference for the conversion process. Any initial inaccuracy of the output voltage can be calibrated in hardware or software. Additionally, changes in the accuracy of the voltage-reference output can be a consequence of the temperature coefficient, the line regulation, the load regulation, or long-term drift. The series voltage reference provides better performance in all of these categories.

Figure 3. An ideal, 3-bit ADC transfer function



Understanding reference-voltage noise

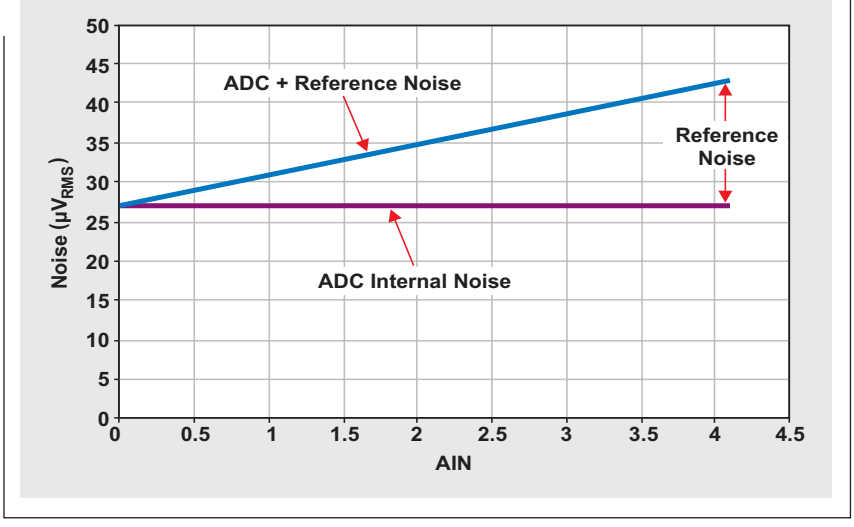
From Part 1 of this series it can be concluded that the ADC has only one function. That function is to compare an input voltage to a reference voltage, or to create an output code based on an input signal and reference voltage. Part 1 presented diagrams and formulas that describe the basic transfer function of the ADC along with the device's noise characteristics. The typical transfer function of an ideal ADC, shown here in Figure 3, was described as

$$\text{Code} = V_{IN} \times \frac{2^n}{V_{REF}}, \qquad (1)$$

where "Code" is the ADC output code in decimal form, V_{IN} is the analog input voltage to the ADC, n is the number of ADC output bits, and V_{REF} is the analog value of the reference voltage to the ADC. This formula shows that any initial error or noise in the reference voltage translates to a gain error in the code output of the ADC.

If several points from the ADC's negative full-scale input to its positive full-scale input are measured, it becomes clear that the contribution of the reference noise is a function of the ADC input voltage. To evaluate the voltage-reference noise as well as the overall noise, it is necessary to measure the noise close to both the negative full scale and the positive full scale. Figure 4 shows the results of measuring the reference noise and the ADC noise in a system. These results show that the overall noise is not constant but linearly dependent on the ADC's analog input voltage. When this type of system is designed, it is important to keep the reference noise lower than the ADC's internal noise.

Figure 4. Total noise at ADC output as a function of ADC input voltage



Both reference topologies in Figure 2 generate comparable noise over frequency. The voltage noise in series voltage references comes mainly from the bandgap and

the output amplifier. Both of these elements generate noise in the 1/f region and the broadband region (see Figure 5).

Noise in the voltage reference's 1/f region

In the data sheets of most series-reference devices, the specification for output-voltage noise is over the frequency range of 0.1 to 10 Hz, which encompasses the 1/f region in Figure 5. Noise in the 1/f region, often called "pink noise," is replaced in the higher frequency domain by the broadband noise.

Noise in the voltage reference's broadband region

Some manufacturers include specifications for the voltage reference's output noise density. This type of specification is usually for noise in the broadband region, such as the noise density at 10 kHz. Broadband noise, which is present over the higher wideband frequencies, is also known as "white noise" or "thermal noise."

An added low-pass filter with an extremely low corner frequency will reduce the broadband noise at the output of the reference. This filter is designed with a capacitor, the equivalent series resistance (ESR) of the capacitor, and the open-loop output impedance of the reference output amplifier (see Figure 6).

Table 1 shows the noise measured from the Texas Instruments REF5040 for different frequency bandwidths as well as for different external-capacitor values and types. These measurements demonstrate that ceramic capacitors with a low ESR of about 0.1 Ω have a tendency to increase noise compared to tantalum capacitors with a standard ESR of about 1.5 Ω. This tendency is the result of stability problems and the gain peaking of the reference's output amplifier.

As mentioned earlier, the two sources of noise in the reference voltage are the internal output amplifier and the bandgap. The internal schematic of the REF5040 in Figure 7 shows that the TRIM pin provides direct access to the bandgap. An external capacitor can be added to the TRIM pin to create a low-pass filter. This filter provides a

Figure 5. Example voltage-noise regions in the frequency domain

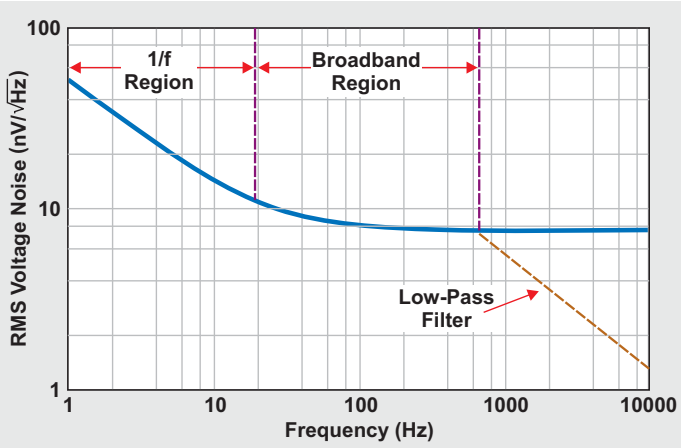


Figure 6. Low-pass filter between series voltage reference and ADC

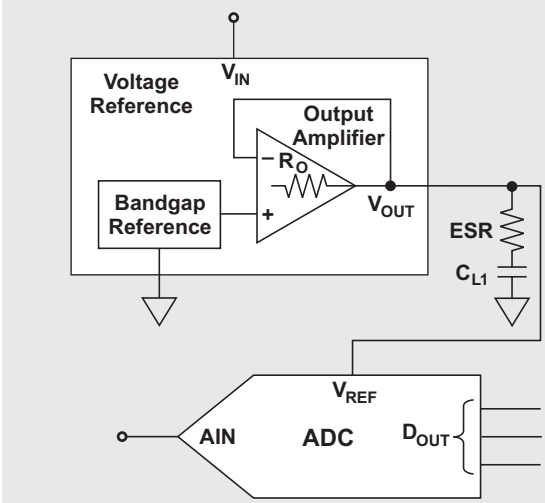


Figure 7. Using TRIM pin to filter REF5040 bandgap noise

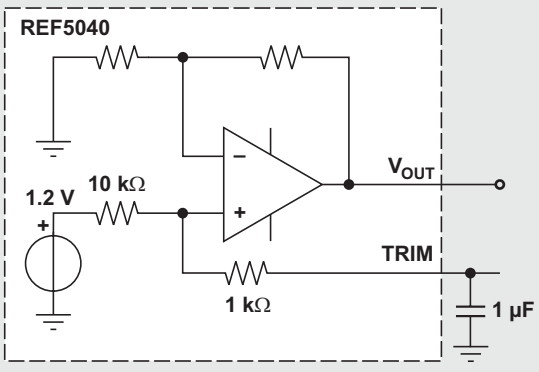


Table 1. Noise measured from REF5040 for different bandwidths and capacitor values and types

CAPACITOR	MEASURED NOISE (μV_{RMS}) FOR FOUR BANDWIDTHS			
	22 kHz (Low-Pass 5-Pole)	30 kHz (Low-Pass 3-Pole)	80 kHz (Low-Pass 3-Pole)	>500 kHz
GND	0.8	1	1.8	4.9
1 µF (tantalum)	37.8	41.7	53.7	9017
2.2 µF (ceramic)	41.7	46.2	55.1	60.8
10 µF (tantalum)	33.4	33.4	35.2	38.5
10 µF (ceramic)	37.1	37.2	37.8	39.1
20 µF (ceramic)	33.1	33.1	33.2	34.5
47 µF (tantalum)	23.2	23.8	24.1	26.5

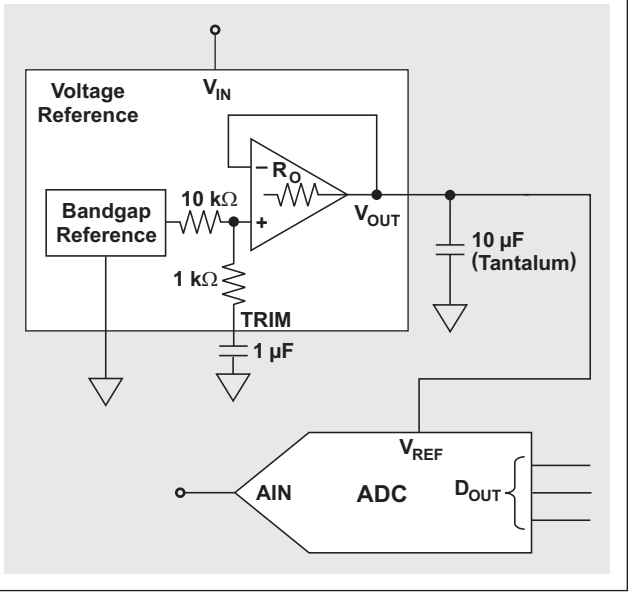
bandgap broadband attenuation of approximately –21 dB. For example, a small 1-µF capacitor adds a pole at 14.5 Hz and a zero at 160 Hz. If more filtering is needed, a larger-value capacitor can be used in place of the 1-µF capacitor. For instance, a 10-µF capacitor will generate a 3-dB corner frequency of 1.45 Hz. This low-pass filter will lower the bandgap noise. Attaching a 1-µF capacitor to the TRIM pin of the REF5040 will lower the total output RMS noise by a factor of 2.5.

Conclusion

Figure 8 shows a complete circuit diagram for a reference system configured with an 8- to 16-bit converter. The accuracy of the voltage reference in this system is important; however, any initial inaccuracy can be calibrated with hardware or software. On the other hand, eliminating or reducing reference noise will require a degree of characterization and hardware-filtering techniques. Part 3 of this article series will explore the proper filtering for the broadband region.

Part 3 will also investigate and explain how to design a reference circuit that is appropriate for converters with 16+ bits. The impact of the voltage-reference buffer and its following amplifier/resistor/capacitor network will be analyzed. With the measurements that follow the final system tuning, the assumptions and conclusions of this article series will be compared to the real world.

Figure 8. Voltage-reference circuit for 10- to 14-bit converters



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Document Title	TI Lit. #
1. Bonnie Baker and Miro Oljaca, "How the Voltage Reference Affects ADC Performance, Part 1," *Analog Applications Journal* (2Q 2009)	slyt331
2. Bonnie Baker, "A Glossary of Analog-to-Digital Specifications and Performance Characteristics," Application Report	sbaa147
3. Tim Green. Operational amplifier stability, Parts 3, 6, and 7. *EN-Genius Network: analogZONE: acquisitionZONE* [Online]. Available: http://www.analogzone.com/acqt*0000*.pdf (Replace "*0000*" with "0307" for Part 3, "0704" for Part 6, or "0529" for Part 7.)	—
4. Bonnie C. Baker and Miro Oljaca. (2007, June 7). External components improve SAR-ADC accuracy. *EDN* [Online]. Available: http://www.edn.com/contents/images/6447231.pdf	—
5. Wm. P. (Bill) Klein, Miro Oljaca, and Pete Goad. (2007). Improved voltage reference circuits maximize converter performance. Analog eLab™ Webinar [Online]. Available: http://dataconverter.ti.com (Scroll down to "Videos" under "Analog eLab™ Design Support" and select webinar title.)	—
6. Art Kay. Analysis and measurement of intrinsic noise in op amp circuits, Part I. *EN-Genius Network: analogZONE: audiovideoZONE* [Online]. Available: http://www.en-genius.net/includes/files/avt_090406.pdf	—

Related Web sites

dataconverter.ti.com
www.ti.com/sc/device/REF5040

Reducing radiated EMI in WLED drivers

By Jeff Falin
Senior Applications Engineer

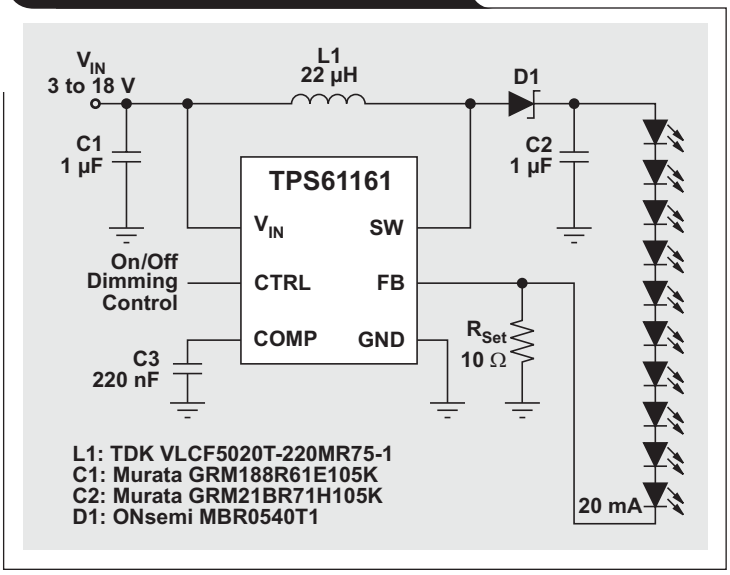
Most mobile phones use white LEDs (WLEDs) as the backlight for their displays. Li-Ion batteries with an output range of 2.7 to 4.2 V are the most common power source for mobile phones. Since several WLEDs in series, each with forward voltages around 3.6 V, are typically used for the backlight, the backlight driver must provide a voltage higher than the Li-Ion range. Therefore, an inductive boost converter is a common power-supply topology for WLED drivers. Figure 1 shows a typical backlight-driver solution that uses the TPS61161 to drive ten LEDs in series.

All inductive switching converters cause radiated electromagnetic interference (EMI) that is directly proportional to output power. As the size of mobile phone displays increases to accommodate more features, the backlight driver's increased output power results in more EMI. Factors at each design step, from driver-IC selection to board layout, impact the WLED driver's EMI. Therefore, minimizing the WLED backlight driver's radiated EMI so that it does not affect other systems is a major concern for manufacturers of both the backlight driver IC and the mobile phone.

Radiated EMI is caused by induced electric fields where capacitors store their energy, and induced magnetic fields where inductors store their energy. The electric-field strength of a capacitor is directly proportional to its capacitance and the voltage across its terminals. The capacitance is inversely proportional to the distance between the terminals. Ideally, the IC and components are laid out on the board to minimize the undesired (often called "parasitic") capacitance. Such capacitance can be created, for example, by a large metal trace or plane on top of a ground trace or plane. Likewise, an inductor's magnetic-field strength is directly proportional to its inductance value and the current flowing through it. The inductance value is directly proportional to the wire or trace length. The board ideally is laid out to minimize parasitic inductance created by long wires, loops, and traces; and shielded inductors are used on the PCB itself. Moreover, the rate of change of the voltages across and the currents through these parasitic components directly impacts their field strengths. Key methods of reducing EMI are to minimize the size of and interaction between these parasitic components and to reduce their voltages and current ramp rates.

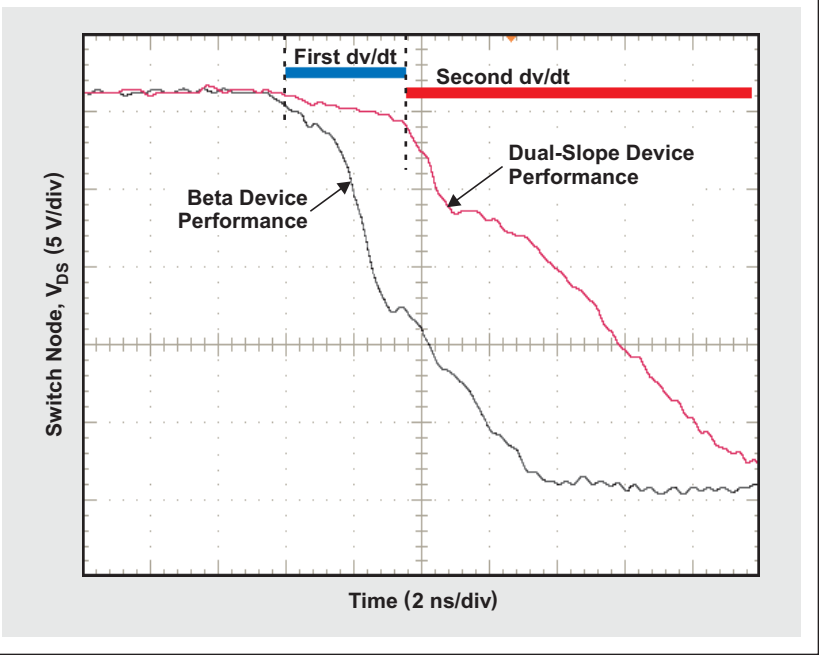
The circuit designer and IC-layout engineer are responsible for minimizing the parasitic inductances and capacitances that occur at high frequencies (greater than 300 MHz) and/or for managing voltage and current ramp rates inside the IC. Otherwise, the IC itself will generate

Figure 1. TPS61161 backlight driver



EMI. Consider Figure 2, which shows the drain voltage, V_{DS}, of the TPS61161's internal NMOS FET (i.e., the switch node) as the FET turns on. The blue trace is from a test board with beta TPS61161 silicon that has a commonly used high-speed gate drive. The red trace shows the same node on the same test board but with the final TPS61161 silicon that has TI's dual-slope switching technology. This technology controls the switch node's slope on the falling edge (i.e., dv/dt) in two steps. When the internal power FET first turns on, there is a large current spike. During the first step of a dual-slope FET compared to a normal FET, the dv/dt is slowed to reduce the amplitude of the current spike and the EMI that results primarily from parasitic inductance. During the second step, the switch FET returns to its normal, faster dv/dt to minimize the switching losses that would otherwise occur.

Figure 2. Switch node (V_{DS} of NMOS FET) of TPS61161's WLED driver



To measure the far-field EMI from a battery-powered evaluation module (TPS61161EVM-243), an IC with a traditional switch (shown in red in Figure 3) and an IC with a dual-slope switch (shown in green) were used in the same test environment. The black curve shows the noise floor of the measurement, and the 850-MHz spike is from a spurious GSM signal. It is clear that the dual-slope switching technology reduced the EMI in the 400-MHz range by 10 dBµV/m.

Figure 3. TPS61161's EMI measurements with traditional switch and dual-slope switch

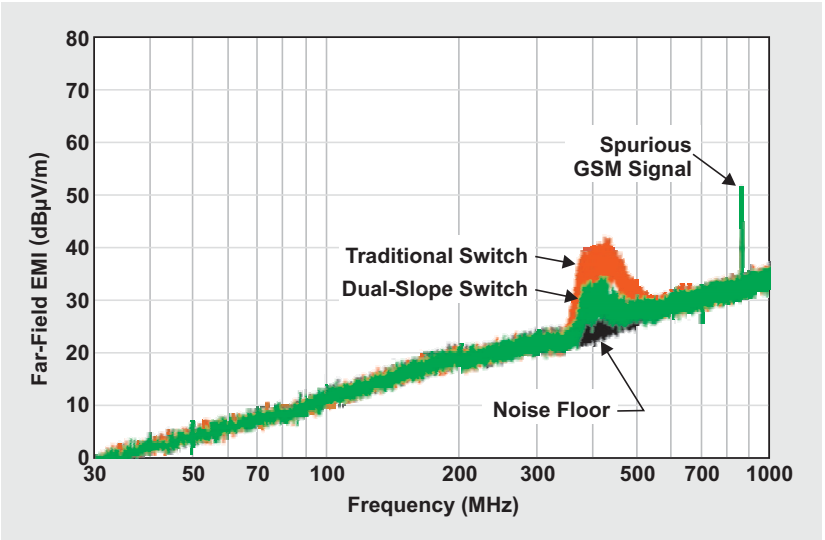
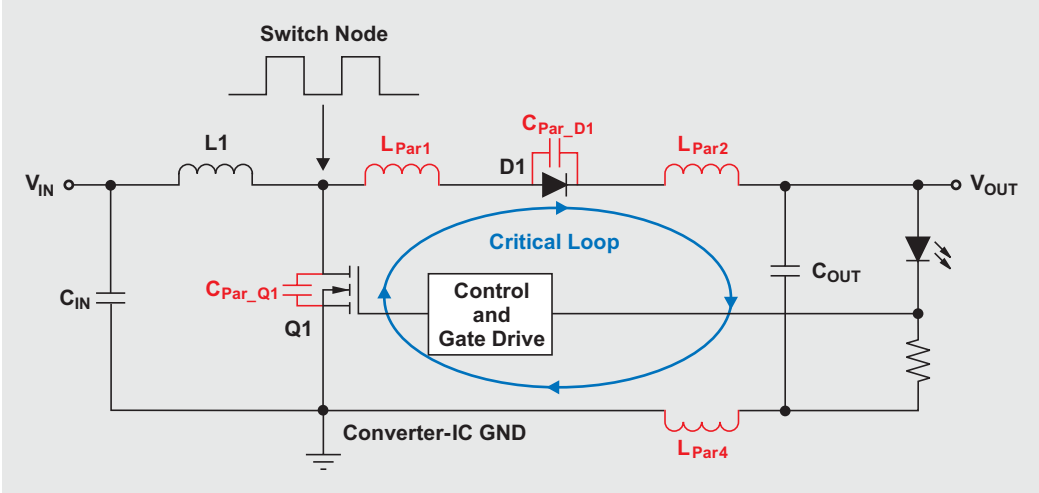


Figure 4. Schematic of boost-converter-based WLED driver



At lower frequencies, the parasitic inductance and capacitance of the PCB's traces and planes are the primary contributors to EMI. Figure 4 shows the schematic for a boost-converter-based WLED driver. The loop created by the parasitic capacitance of Q1 and D1 and the parasitic inductance of the board traces conducts current when switches D1 and Q1 turn on and off. When switch Q1 turns off, inductor L1 is fully charged and ready to continue the current flow. Since the only available element through which current can continue to flow is D1, the inductor voltage quickly switches from GND to V_{OUT}, which causes ringing due to the parasitics. The resonance point of the parasitic inductance and capacitance can sometimes be seen on the oscilloscope as ringing at the resonant frequency. In addition to the parasitic capacitance of Q1 and D1, ground planes and the traces over/under them also contribute to parasitic capacitance. A commonly overlooked type of parasitic capacitance is that formed by the switch node—with its large dv/dt—and the ground plane underneath. Figure 5 shows a poor PCB layout that uses the TPS61161, where L1 is the inductor, D1 is the diode, U1 is the TPS61161 controller, C1 is the input capacitor, and C3 and C4 are the output capacitors. The critical loop, highlighted in blue, is long; and there is a large ground plane underneath the large pad for L1 that serves as the high-speed switch node (not shown).

Figure 5. Poor PCB layout with TPS61161

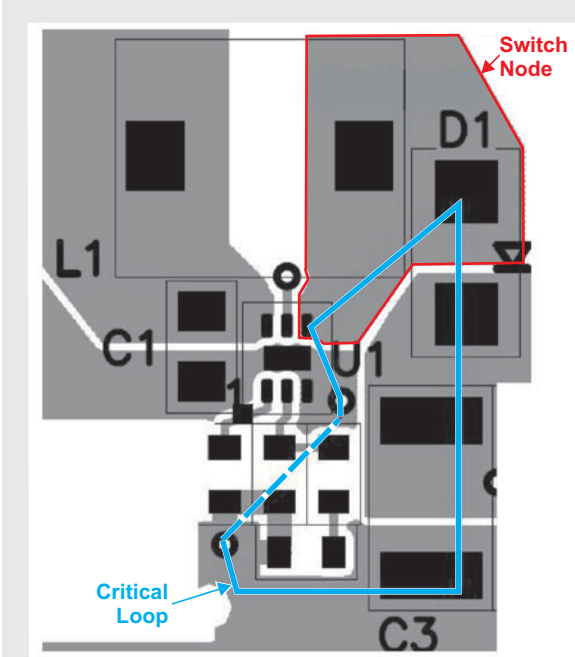


Figure 6. Improved PCB layout with TPS61161

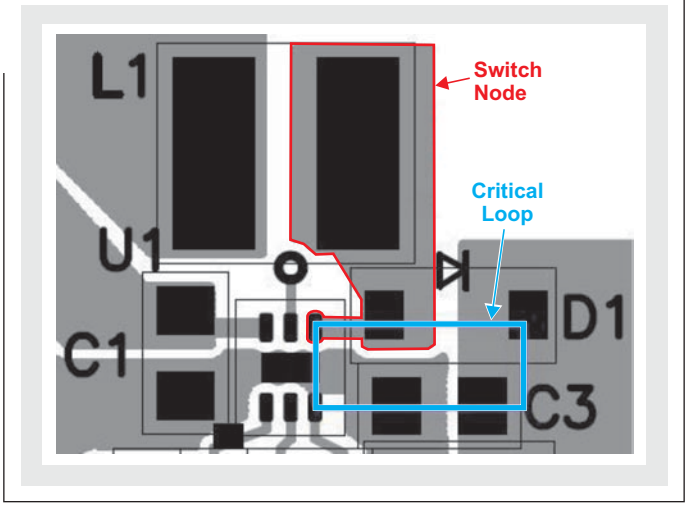


Figure 6 shows the TPS61161 evaluation module with the same components as in Figure 5 but with a smaller switch node, no ground plane underneath, and more compact part placement to reduce the length of the critical loop (shown in blue).

Figure 7 shows the near-field EMI measurements from two battery-powered test boards, one with poor layout and the other with improved layout. The tests were conducted under identical conditions with the same inductor and the TPS61161 (final silicon). Clearly, an improved board layout that minimizes parasitic board capacitance and inductance reduces EMI across multiple frequencies.

A switching converter's EMI cannot be completely eliminated. However, with careful IC and passive-component selection as well as good board-layout techniques, EMI can be reduced to acceptable levels.

Reference

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Document Title	**TI Lit. #**
1. "White LED Driver With Digital and PWM Brightness Control in 2mm × 2mm QFN Package for up to 10 LEDs in Series," TPS61160/61 Data Sheet.	slvs791

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power.ti.com
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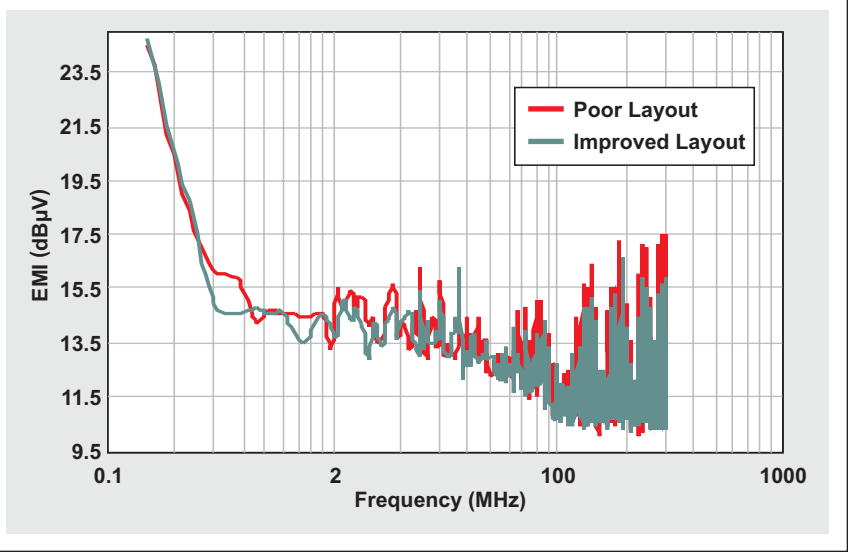
Figure 7. TPS61161's EMI measurements with poor and improved layouts



Using fully differential op amps as attenuators, Part 2: Single-ended bipolar input signals

By Jim Karki
Member, Technical Staff, High-Performance Analog

Introduction

Fully differential operational amplifiers (FDAs) can easily be used to attenuate and level-shift high-voltage input signals to match the input requirements of lower-voltage ADCs. This article is Part 2 of a three-part series. In Part 1 (see Reference 2) we considered a balanced, differential bipolar input signal and proposed an architecture utilizing an FDA to accomplish the task. In Part 2 we will show how to adapt the circuits presented in Part 1 to a high-voltage, single-ended (SE) bipolar input. Part 3, which will appear in a future issue of the *Analog Applications Journal*, will show the more generic case of an SE unipolar input with arbitrary common-mode voltage. As mentioned in Part 1, the fundamentals of FDA operation are presented in Reference 1, which provides definitions and derivations.

Attenuator circuit for SE bipolar input

Using an input attenuator

Now consider a high-amplitude, SE bipolar input signal that needs to be attenuated and level-shifted to the appropriate levels to drive a lower-voltage input ADC. The first step is to modify the differential bipolar input circuit presented in Part 1 to accept an SE bipolar input and keep the amplifier balanced. This is accomplished by grounding one side of the signal source, splitting R_T in half, and grounding the center point. Otherwise the circuit is the same. Splitting R_T in half and grounding the center point are key to keeping the resistances that set the gain on each side of the amplifier balanced so that no offsets are generated. Figure 5 shows the modified circuit.

We can build the circuit as shown (with appropriate values), but we can get the equivalent circuit shown in Figure 6 with a few simple changes: Combine R_S, R_G, and $R_T/2$ on the alternate input from the signal into an equivalent resistor R_{G-}; use reference designator R_{G+} on the positive side; and replace $R_T/2$ with R_T. The circuit analysis of Figure 6 is very similar to that of Figure 1 in Part 1 of this series, but the changes in the input configuration result in a new gain equation:

$$\frac{V_{OUT\pm}}{V_{Sig}} = \frac{R_T}{R_S + R_T} \times \frac{R_F}{R_{G+} + R_S \parallel R_T} \qquad (4)$$

The noise gain of the FDA can be set to 2 by making the second half of Equation 4 equal to 1:

$$R_{G+} + R_S \parallel R_T = R_F \qquad (5)$$

Figure 5. Differential bipolar input circuit modified to accept SE bipolar input

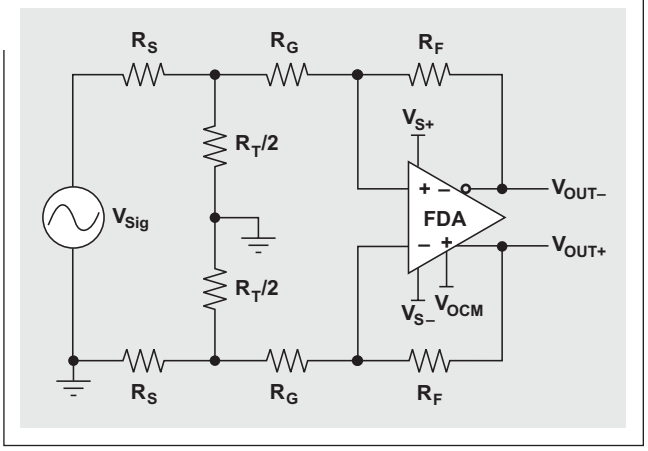
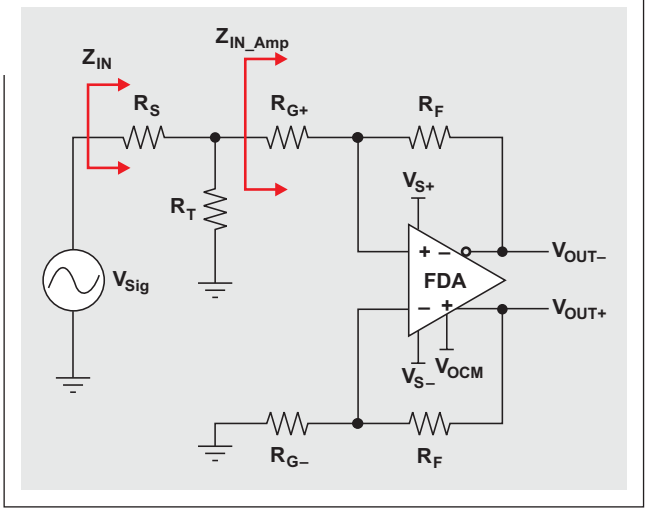


Figure 6. Equivalent SE bipolar input circuit



With this constraint, the overall gain equation reduces to

$$\frac{V_{OUT\pm}}{V_{Sig}} = \frac{R_T}{R_S + R_T}. \qquad (6)$$

The design equations provide two degrees of freedom for choosing components. The input impedance is given by

$Z_{IN} = R_S + R_T \| Z_{IN\_Amp}$, which is approximated by $Z_{IN} = R_S + R_T \| R_{G+}$; so we start by first choosing R_S close to the desired input impedance. We then select R_F in the recommended range for the device and calculate the required value of R_T to give the desired attenuation. These results can be used to calculate R_{G+} and an equivalent value for R_{G-}. To see an example Excel® worksheet, click on the Attachments tab or icon on the left side of the Acrobat® Reader® window. Open the file FDA_Attenuator_Examples_SE_Bipolar_Input.xls, then select the Bipolar SE FDA Input Atten worksheet tab.

Design Examples 3a and 3b

For Example 3a, let's say that again we have a 20-V_{PP} bipolar (±10-V) input, but this time it is an SE signal. We need a 1-kΩ input impedance and want to use the ADS8321 SAR ADC with a 5-V_{PP} differential input and a 2.5-V common-mode voltage. We choose R_S = 1 kΩ and R_F = 1 kΩ. Rearranging Equation 6 and using substitution, we can calculate

$$R_T = \frac{R_S}{\frac{V_{Sig}}{V_{OUT\pm}} - 1} = \frac{1\ k\Omega}{4-1} = 333.3\ \Omega.$$

The nearest standard 1% value, 332 Ω, should be used. Then, rearranging Equation 5 and using substitution, we can calculate

$$R_{G+} = R_F - R_S \| R_T = 1\ k\Omega - 1\ k\Omega \| 332\ \Omega = 750\ \Omega,$$

which is a standard 1% value. We can then calculate

$$R_{G-} = R_{G+} + R_S \| R_T = 750\ \Omega + 1\ k\Omega \| 332\ \Omega = 1\ k\Omega,$$

which is a standard 1% value. These values will provide the needed attenuation and keep the FDA stable. Again the V_{OCM} input on the FDA is used to set the output common-mode voltage to 2.5 V.

The input impedance is Z_{IN} = 1254 Ω, which is higher than desired. If the input impedance really needs to be closer to 1 kΩ, we can iterate with a lower value as before. In this case, using R_S = 787 Ω and R_F = 1 kΩ will yield Z_{IN} = 999 Ω, which comes as close as is possible when standard 1% values are used.

To see a TINA-TI™ simulation of the circuit in Example 3a, click on the Attachments tab or icon on the left side of the Acrobat Reader window. If you have the TINA-TI software installed, you can open the file FDA_Attenuator_Examples_SE_Bipolar_Input.TSC to view the example (the top circuit labeled "Example 3a"). To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

The simulation waveforms for Example 3a show that the signal is distorted. Further investigation will show that the input common-mode voltage range of the THS4520 used in the simulation has been violated, causing nonlinear operation. In this case the SPICE model shows a problem; but care must be taken to double-check operation against the data sheet, as not all SPICE models will show this error. For instance, replacing the THS4520 model with the THS4509 will simulate fine, but the actual device has a similar input common-mode voltage range.

One way to correct the problem is to use pull-up resistors from the FDA input pins to the +5-V supply, as described in the THS4520 data sheet. In this case, 2-kΩ pull-up resistors will bring the input common-mode voltage back into linear operation and will have no effect on the gain of the signal. To see a TINA-TI simulation of this corrected circuit (Example 3b), follow the same procedure as for Example 3a, but view the middle circuit labeled "Example 3b." Note that this circuit provides the same results as those shown in Figure 3 of Part 1.

Another way to eliminate the problem with input common-mode voltage is to use the R_F and R_G gain-setting resistors of the FDA as the attenuator, a method that is described next.

Using an FDA's R_F and R_G as an attenuator

The proposed circuit using gain-setting resistors to obtain an SE bipolar input signal is shown in Figure 7. In this circuit, the FDA is used as an attenuator in a manner similar to using an inverting op amp, as described in Part 1 for the differential bipolar signal. The design equations are the same as in Part 1, except that the input impedance is reduced by approximately half. Thus, the gain (or attenuation) is set by R_F and R_G:

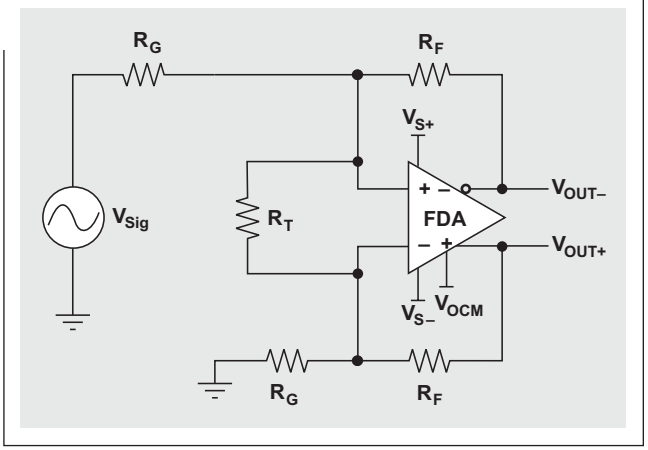
$$\frac{V_{OUT\pm}}{V_{Sig}} = \frac{R_F}{R_G}$$

R_T is used to set the noise gain to 2 for stability; i.e.,

$$R_F = R_G \| \frac{R_T}{2},$$

and the input impedance is $Z_{IN} \approx R_G$.

Figure 7. Using FDA's R_F and R_G as attenuator for SE bipolar input



Design Example 4

Using the same approach as for Example 3a, with $R_F = 1\ k\Omega$, we calculate $R_G = 4\ k\Omega$ (the nearest standard 1% value is 4.02 kΩ) and $R_T = 2.67\ k\Omega$ (the nearest standard 1% value is 2.67 kΩ). This makes $Z_{IN} \approx 4.02\ k\Omega$, and SPICE shows it to be more on the order of 4.46 kΩ. The simulation results are the same as before, but with this approach the only freedom of choice given the design requirements is the value of R_F.

To see an example Excel worksheet, click on the Attachments tab or icon on the left side of the Acrobat Reader window. Open the file FDA_Attenuator_Examples_SE_Bipolar_Input.xls, then select the Bipolar SE FDA RF_RG Atten worksheet tab. To see a TINA-TI simulation of the circuit in Example 4, follow the same procedure as for Example 3a, but view the bottom circuit labeled "Example 4." Note that the circuit provides the same results as those shown in Figure 3 of Part 1.

Conclusion

We have analyzed two approaches to using an FDA to attenuate and level-shift high-amplitude, SE bipolar signals to the input range of lower-voltage input ADCs. The first approach (Example 3a) uses an input attenuator with values chosen to provide the required attenuation and to keep the noise gain of the FDA equal to 2 for stability. We saw in the simulation of this example that there is a potential problem with input common-mode voltage that we can solve by using pull-up resistors from the inputs (Example 3b). The second approach (Example 4) uses the gain-setting resistors of the FDA in much the same way as using an inverting op amp, then a resistor is bootstrapped across the inputs to provide a noise gain of 2. Except for the potential problem with the input common-mode voltage in Example 3a, the approaches in Examples 3a and 4 yield the same voltage translation that is needed to accomplish the interface task. Other performance metrics were not analyzed here, but the two approaches have substantially the same noise, bandwidth, and other AC and DC performance characteristics as long as the value of R_F is the same.

The input-attenuator approach in Example 3a is more complex but allows the input impedance to be adjusted independently from the gain-setting resistors used around the FDA. At least to a certain degree, lower values can easily be achieved if desired, but there is a maximum allowable R_S where larger values require the R_{G+} resistor to be a negative value. For example, setting $R_S = 4\ k\Omega$ results in $R_{G+} = 0\ \Omega$. The spreadsheet tool provided will generate "#NUM!" errors for this input as it tries to calculate the nearest standard value, which then replicates throughout the rest of the cells that require a value for R_{G+}; but this value will work.

The approach in Example 4 is easier, but the input impedance is set as a multiplication of the feedback resistor and attenuation: $Z_{IN} \approx 2 \times R_F \times \text{Attenuation}$. This does allow some design flexibility by varying the value of R_F, but the impact on noise, bandwidth, distortion, and other performance characteristics should be considered.

One final note: The source impedance will affect the input gain or attenuation of either circuit and should be included in the value of R_S, especially if it is significant.

References

For more information related to this article, you can download an Acrobat® Reader® file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. Jim Karki, "Fully-Differential Amplifiers," Application Report.	sloa054
2. Jim Karki, "Using Fully Differential Op Amps as Attenuators, Part 1: Differential Bipolar Input Signals," *Analog Applications Journal* (2Q 2009)	slyt336

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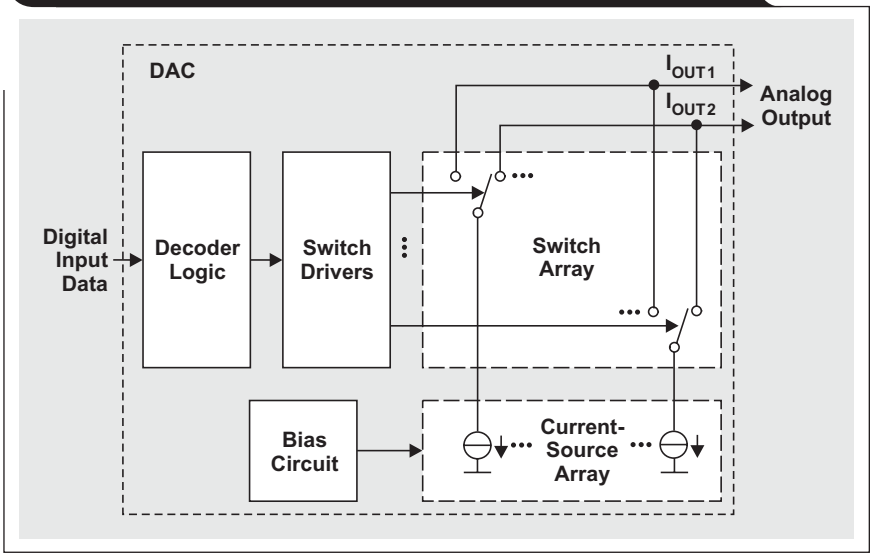
Interfacing op amps to high-speed DACs, Part 1: Current-sinking DACs

By Jim Karki
Member, Technical Staff, High-Performance Analog

Introduction

Digital-to-analog converters (DACs) come in many bit resolutions and sampling speeds. Outputs from lower-speed DACs are often single-ended and have either a voltage or a current output. Most high-speed DACs are designed with complementary outputs that either source or sink current. This article, Part 1 of a three-part series, discusses the interface between a current-sinking DAC and an op amp. Part 2, which will appear in a future issue of the *Analog Applications Journal*, will discuss the interface between a current-sourcing DAC and an op amp. Part 3, also in a future issue of the *Analog Applications Journal*, will provide a simplified approach to the interface analogy presented in Part 2.

Figure 1. Simplified block diagram of current-steering DAC



High-speed DACs are used in end-equipment applications like communications, test equipment, medical applications, industrial applications, and many more where signal generation is required. Each of these applications has its own specific requirements for signal characteristics and performance. This article focuses on end equipment that requires DC coupling, like signal generators with frequency bandwidths of up to 100 MHz and a single-ended output. In these cases, high-speed op amps can provide a good solution for converting the complementary-current output from a high-speed DAC to a voltage that can drive the signal output.

Overview of complementary-current-steering DAC

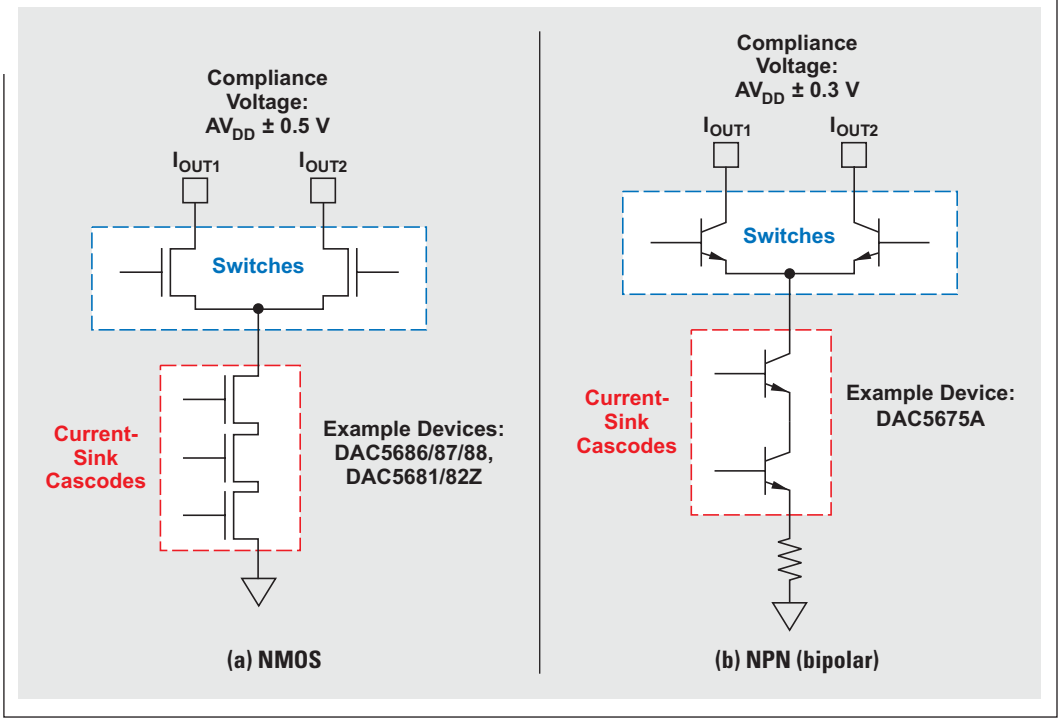
A simplified block diagram of a complementary-current-steering DAC is shown in Figure 1. The digital input is decoded for the switch drivers that switch, or steer, the appropriate current source(s) in the current-source array to the outputs, I_{OUT1} and I_{OUT2}. I_{OUT1} and I_{OUT2} are complementary, which means that if current flows out of one it is subtracted from the other, and vice versa, keeping the total current constant. For example, if full scale is 20 mA, the minimum code input or zero-scale input may provide 0 mA at I_{OUT1} and 20 mA at I_{OUT2}. At midscale, each output provides 10 mA; and at maximum or full scale, I_{OUT1} = 20 mA and I_{OUT2} = 0 mA. This example is illustrated in Table 1. It is important to note that the midscale input, with each output at 10 mA, will be used to set the output common-mode condition for the design.

The current-source array is constructed with either n-type or p-type transistors. The word "source" is used generically to refer to the transistor circuit structure, which may either source or sink current. This article considers the interface between a current-sinking DAC and an op amp in the case where the source array is constructed with n-type transistors.

Table 1. Example of I_{OUT1} and I_{OUT2} currents for 20-mA full scale

INPUT	I_{OUT1} (mA)	I_{OUT2} (mA)
Maximum Scale	20	0
Midscale	10	10
Zero Scale	0	20

Figure 2. Simplified NMOS and NPN current sinks

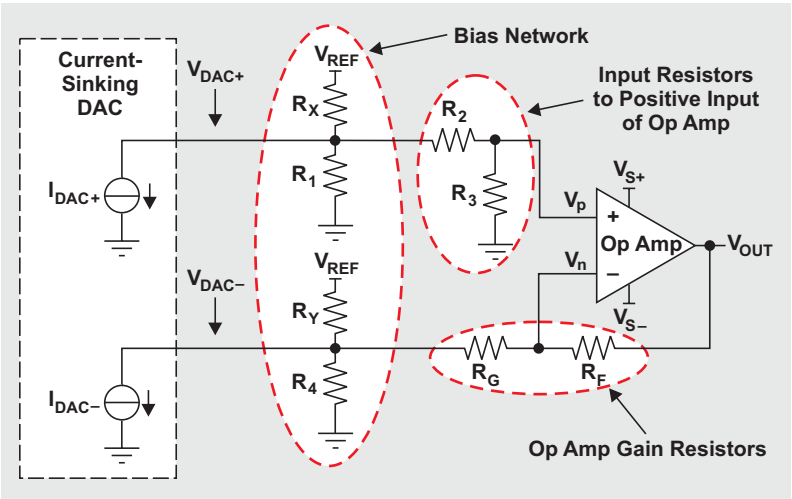


Architecture and compliance voltage of current-sinking DACs

Figure 2 shows simplified examples of NMOS and NPN current sinks and lists a few devices that use them. The compliance voltage shown for each group of devices is the voltage range at the DAC outputs within which a device will perform as specified. Lower voltages tend to shut down the outputs, and higher voltages have the potential to cause breakdown. Both of these should be avoided to provide the best performance and long-term reliability.

Generally the output is terminated via some impedance to a positive power supply. This impedance supplies a current path needed for the sink array, and the voltage drop across the same impedance can be used as a voltage output. The impedance can be constructed in various ways; it can be a simple resistor divider, a transformer-coupled impedance, or a combination of passive components and an active circuit. This article focuses on the latter option, with an op amp as the active circuit.

Figure 3. Proposed circuit for an op amp interface



Op amp interface

The proposed op amp interface is shown in Figure 3. This circuit will provide biasing of the DAC outputs, convert the DAC currents to voltages, and provide a single-ended output voltage via the op amp. The op amp is the active amplifier element for the circuit and uses R_2, R_3, R_G, and R_F to make a difference amplifier.

- I_{DAC+} and I_{DAC-} are the current outputs from the DAC.
- R_2 and R_3 are input resistors to the positive input of the op amp.
- R_G and R_F are the main gain-setting resistors for the op amp.
- R_X, R_1, R_Y, and R_4 provide bias and impedance termination for the DAC outputs.

- V_{DAC+} and V_{DAC-} are the voltages at the outputs of the DAC.
- V_p and V_n are the input terminals of the op amp.
- V_{S+} and V_{S-} are the power supplies to the op amp.

Proper component selection will provide the impedance required to maintain voltage compliance with maximum amplitude and balance for the best performance.

Typically, harmonic distortion in an op amp is dominated (at least at lower frequencies) by the second-order harmonics. Balanced inputs to the difference-amplifier circuit will help suppress second-order harmonics and provide for the best performance, but little impact is expected on third-order harmonics if the inputs are not balanced.

For analysis, it is easiest to break the circuit into positive and negative halves and examine each separately. It will also be assumed that the op amp is ideal.

Analysis of positive side

The positive half of the circuit is shown in Figure 4. To start the analysis, Kirchhoff's current law can be used to write a node equation at V_{DAC+}:

$$I_{DAC+} + \frac{V_{DAC+} - V_{REF}}{R_X} + \frac{V_{DAC+}}{R_1} + \frac{V_{DAC+}}{R_2 + R_3} = 0 \qquad (1)$$

The input impedance can be expressed as

$$Z_{DAC+} = R_X \parallel R_1 \parallel (R_2 + R_3). \qquad (2)$$

Equations 1 and 2 are simultaneous equations with many variables, and designers must choose or identify values based on other design criteria in order to solve them. The following assumptions are made for this article:

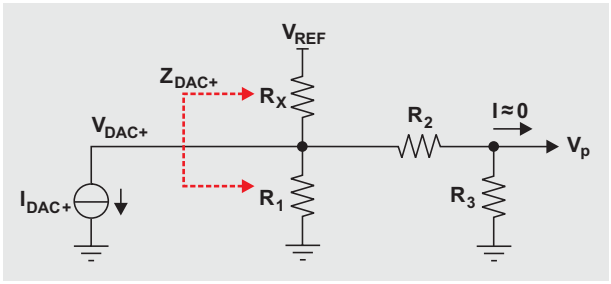
1. The DAC output current, I_{DAC+}, and the voltage swing, V_{DAC+}, are defined by the designer, which sets a target value for Z_{DAC+}.
2. An existing circuit voltage or other known voltage is used for V_{REF}.
3. In a difference amplifier, R_3/R_2 needs to equal R_F/R_G to balance the gain of the amplifier.*
4. The equations will be solved for the condition where the DAC current on the positive side is zero: I_{DAC+} = 0 mA. This in turn sets the DAC voltage on the positive side to its maximum value, $V_{DAC+} = V_{DAC+}(max)$.

With these constraints, the designer can apply algebra and simultaneous-equation techniques to Equations 1 and 2 to solve for $1/R_1$:

$$\frac{1}{R_1} = \frac{1}{Z_{DAC+}\left(1 + \frac{1}{\frac{V_{REF}}{V_{DAC+(max)}} - 1}\right)} - \frac{1}{R_2 + R_3} \qquad (3)$$

*Note that in a voltage-feedback op amp, it is desirable to make the impedance at V_p equal to that at V_n in order to cancel voltage offset caused by the input bias current. In a current-feedback op amp, the input bias currents are not correlated; so it is acceptable not to balance these impedances, but it may be desirable to minimize them.

Figure 4. Positive side of analysis circuit



The known value for R_1 can be substituted into Equation 2, which can then be rearranged to find $1/R_X$:

$$\frac{1}{R_X} = \frac{1}{Z_{DAC+}} - \frac{1}{R_1} - \frac{1}{R_2 + R_3} \qquad (4)$$

Analysis of negative side

The negative half of the circuit is shown in Figure 5. Analysis of the negative side is complicated, because V_n is driven not only by the negative side of the DAC but also by the positive side via the op amp's action. To start the analysis, Kirchhoff's current law can be used to write a node equation at V_{DAC-}:

$$I_{DAC-} + \frac{V_{DAC-} - V_{REF}}{R_Y} + \frac{V_{DAC-}}{R_4} + \frac{V_{DAC-} - V_n}{R_G + R_3} = 0 \qquad (5)$$

The input impedance can be expressed as

$$Z_{DAC-} = \frac{V_{DAC-}}{I_{DAC-}}. \qquad (6)$$

With substitution and rearrangement, the designer can use

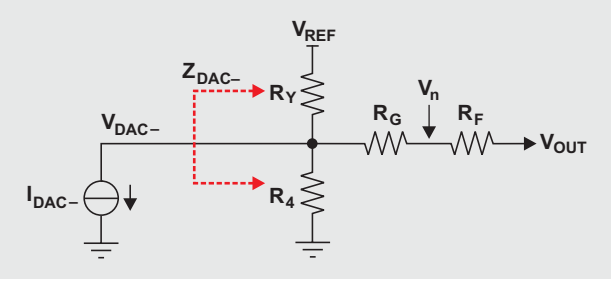
$$V_p = V_{DAC+} \times \frac{R_3}{R_2 + R_3}$$

and $V_n = \alpha V_p$ to rewrite Equation 6 as

$$\frac{1}{Z_{DAC-}} = \frac{1}{Z_{DAC+} \times \alpha\left(\frac{R_3}{R_2 + R_3}\right)} \times \left(\frac{1}{R_Y} + \frac{1}{R_4} + \frac{1}{R_G}\right). \qquad (7)$$

$$1 - \frac{}{R_G}$$

Figure 5. Negative side of analysis circuit



Using the same substitutions and general design constraints used on the positive side to drive values for Z_{DAC-}, V_{REF}, and R_G, simultaneous-equation techniques can be applied to Equations 5 and 7 to solve for $1/R_4$ (Equation 8). Note that the equations are solved for the condition where the DAC current on the negative side is zero: $I_{DAC-} = 0$ mA. This sets the DAC voltage on the negative side to its maximum value, $V_{DAC-} = V_{DAC-(max)}$, and sets the DAC voltage on the positive side to its minimum value, $V_{DAC+} = V_{DAC+(min)}$.

$$\frac{1}{R_4} = \frac{\dfrac{1-\dfrac{Z_{DAC+}\times\alpha\left(\dfrac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} + \left[\dfrac{V_{DAC+(min)}\times\alpha\left(\dfrac{R_3}{R_2+R_3}\right) - V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}} - 1\right]\left(\dfrac{1}{R_G}\right)}{\dfrac{V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}+1} \quad \textbf{(8)}$$

The value of $1/R_4$ can then be used to find $1/R_Y$:

$$\frac{1}{R_Y} = \frac{1-\dfrac{Z_{DAC+}\times\alpha\left(\dfrac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} - \left(\frac{1}{R_4}+\frac{1}{R_G}\right) \quad \textbf{(9)}$$

Note that α, the multiplication factor from V_p to V_n, in essence expresses the difference between the input pins. In a voltage-feedback amplifier, α is set by the loop gain of the amplifier. In a current-feedback amplifier, α is the gain of the input buffer between the inputs. All that aside, α is typically close enough to 1 that it can simply be removed from the calculation.

Calculating output voltage

Superposition can be used to write equations for the separate sources referred to V_{OUT}. Since the DAC only sinks current, which is by convention negative current flow, the output-voltage swing is the opposite of what might be expected. In other words, when the DAC is sinking current on the positive side, the output of the op amp tends to swing negative, and when the DAC is sinking current on the negative side, the output of the op amp tends to swing positive. This means that in the following equations, I_{DAC+} and I_{DAC-} are always negative or zero.

The output-referred DC bias from the positive side is

$$V_{OUT\_V_{p(DC)}} = \left(1+\frac{R_F}{R_G+R_Y \parallel R_4}\right)\times\left[V_{REF}\times\frac{R_1R_3}{R_1(R_2+R_3)+R_X(R_1+R_2+R_3)}\right].$$

The output-referred DAC signal from the positive side is

$$V_{OUT\_V_{p(DAC)}} = \left(1+\frac{R_F}{R_G+R_Y \parallel R_4}\right)\times\left[I_{DAC+}\times\frac{R_XR_1R_3}{R_XR_1+(R_1+R_X)(R_2+R_3)}\right].$$

The output-referred DC bias from the negative side is

$$V_{OUT\_V_{n(DC)}} = -\left(V_{REF}\times\frac{R_4}{R_Y+R_4}\times\frac{R_F}{R_G+R_Y \parallel R_4}\right).$$

The output-referred DAC signal from the negative side is

$$V_{OUT\_V_{n(DAC)}} = -\left(I_{DAC-}\times\frac{R_YR_4R_F}{R_YR_4+R_GR_4+R_YR_G}\right).$$

Adding these four equations provides an expression for V_{OUT}:

$$V_{OUT} = V_{OUT\_V_{p(DC)}} + V_{OUT\_V_{p(DAC)}} + V_{OUT\_V_{n(DC)}} + V_{OUT\_V_{n(DAC)}} \quad \textbf{(10)}$$

If it is assumed that $I_{DAC} = I_{DAC+} - I_{DAC-}$, $Z = Z_{DAC+} = Z_{DAC-}$, and $R_F/R_G = R_3/R_2$, the DC component of the DAC outputs will cancel and the AC-signal's gain equation from the DAC output current to the voltage output of the op amp can be simplified and written as

$$\frac{V_{OUT}}{I_{DAC}} = 2Z\times\frac{R_F}{R_G}. \quad \textbf{(11)}$$

Design example and simulation

For an example of how to proceed with the design, assume that one of the NMOS DACs noted earlier, with a compliance voltage of 3.3 ±0.5 V, is being used. Also assume that the full-scale output is set to 20 mA. To get a 5-V_{PP}, DC-coupled single-ended output signal, the circuit shown in Figure 3 can be used. Since a ±5-V power supply is being used for the op amp, it is convenient to make V_{REF} = 5 V. Given that $I_{DAC±}$ = 20 mA and $V_{DAC±}$ = 1 V_{PP}, the target impedance, $Z_{DAC±}$, can be calculated to equal 50 Ω.

With the starting design constraints given earlier, the THS3095 current-feedback op amp is selected as the amplifier, where $R_3 = R_F$ = 750 Ω. The gain from $V_{DAC±}$ to the output is given by the resistor ratios $R_F/R_G = R_3/R_2$, so R_G can be calculated as

$$R_G = R_2 = R_F \times \frac{V_{DAC±}}{V_{OUT}} = 750\ \Omega \times \frac{2(1\ V)}{5\ V} = 300\ \Omega.$$

The nearest standard 1% value, 301 Ω, should be used.

Equations 3, 4, 8, and 9 can be used to find, respectively, R_1, R_X, R_4, and R_Y:

$$R_1 = \frac{1}{\frac{1}{Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(max)}}-1}\right)} - \frac{1}{R_2+R_3}} = \frac{1}{\frac{1}{50\ \Omega\left(1+\frac{1}{\frac{5\ V}{3.8\ V}-1}\right)} - \frac{1}{301\ \Omega+750\ \Omega}} = 259.8\ \Omega$$

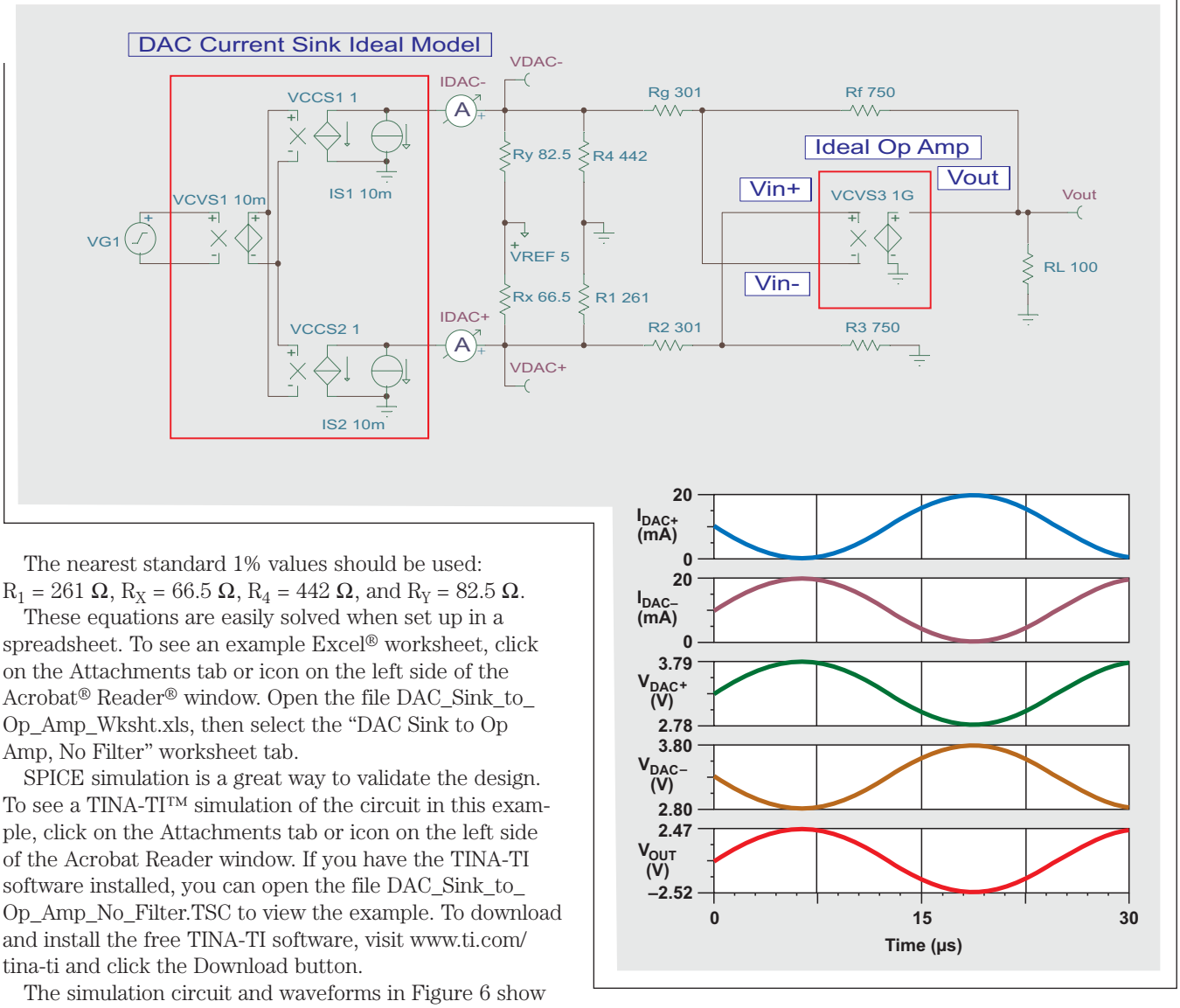
$$R_X = \frac{1}{\frac{1}{Z_{DAC+}} - \frac{1}{R_1} - \frac{1}{R_2+R_3}} = \frac{1}{\frac{1}{50\ \Omega} - \frac{1}{259.8\ \Omega} - \frac{1}{301\ \Omega+750\ \Omega}} = 65.8\ \Omega$$

$$R_4 = \frac{\frac{V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}+1}{\frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} + \left[\frac{V_{DAC+(min)}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)-V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}-1\right]\left(\frac{1}{R_G}\right)}$$

$$= \frac{\frac{3.8\ V}{5\ V-3.8\ V}+1}{\frac{1-\frac{50\ \Omega\times1\times\frac{750\ \Omega}{301\ \Omega+750\ \Omega}}{301\ \Omega}}{50\ \Omega} + \left(\frac{2.8\ V\times1\times\frac{750\ \Omega}{301\ \Omega+750\ \Omega}-3.8\ V}{5\ V-3.8\ V}-1\right)\left(\frac{1}{301\ \Omega}\right)} = 447.2\ \Omega$$

$$R_Y = \frac{1}{\frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} - \left(\frac{1}{R_4}+\frac{1}{R_G}\right)} = \frac{1}{\frac{1-\frac{50\ \Omega\times1\times\frac{750\ \Omega}{301\ \Omega+750\ \Omega}}{301\ \Omega}}{50\ \Omega} - \left(\frac{1}{447.2\ \Omega}+\frac{1}{301\ \Omega}\right)} = 82.9\ \Omega$$

Figure 6. Simulation of current-sinking DAC interfaced to op amp



The nearest standard 1% values should be used: R_1 = 261 Ω, R_X = 66.5 Ω, R_4 = 442 Ω, and R_Y = 82.5 Ω.

These equations are easily solved when set up in a spreadsheet. To see an example Excel® worksheet, click on the Attachments tab or icon on the left side of the Acrobat® Reader® window. Open the file DAC_Sink_to_Op_Amp_Wksht.xls, then select the "DAC Sink to Op Amp, No Filter" worksheet tab.

SPICE simulation is a great way to validate the design. To see a TINA-TI™ simulation of the circuit in this example, click on the Attachments tab or icon on the left side of the Acrobat Reader window. If you have the TINA-TI software installed, you can open the file DAC_Sink_to_Op_Amp_No_Filter.TSC to view the example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

The simulation circuit and waveforms in Figure 6 show that the circuit simulates as expected. I_{DAC+} and I_{DAC-} are the DAC currents, V_{DAC+} and V_{DAC-} are the voltages developed at the DAC outputs, and V_{OUT} is the output of the amplifier. The current-sinking DAC and op amp are ideal elements constructed with SPICE macros and are intended to show that the equations derived earlier for R_1, R_X, R_4, and R_Y are valid for ideal elements. Actual performance will vary depending on selected devices.

DAC image-filter considerations

The DAC output signal will have the desired baseband signal as well as the sampling images that occur at multiples of the sampling frequency. Filtering is usually used to reduce the amplitude of the sampling images because they degrade performance. Filtering directly at the DAC output before the op amp will preserve the best performance. This is especially important with multitone signals where second-order intermodulation products from the sampling images appear at the baseband.

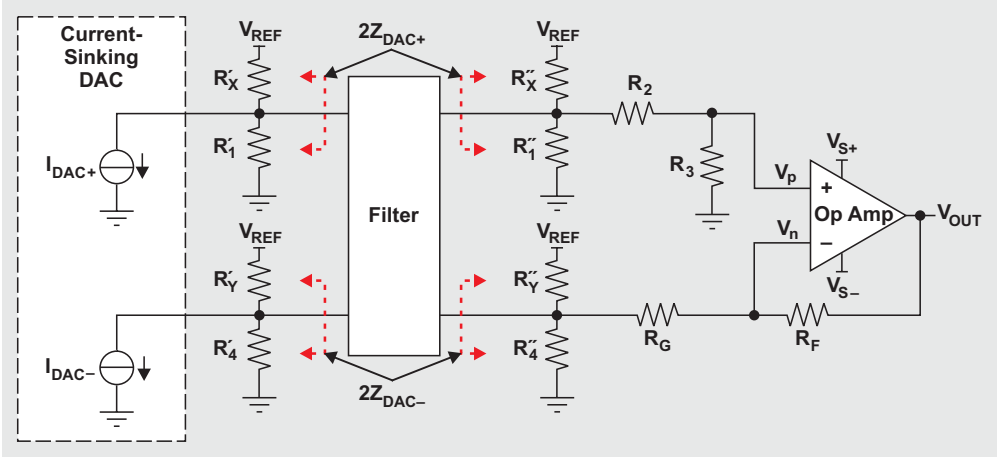
Filter design is not the topic of this article, so it will not be covered in much detail; but for proper operation the filter component values are calculated based on the input and output impedances seen by the filter. While finding the exact value of the impedance is not so troublesome, it is usually much easier to find standard component values to implement the filter when the input and output impedances to the filter are equal. With this in mind, let's now consider how to achieve the same goals as before while keeping the impedance seen by the filter balanced.

Figure 7 shows the proposed circuit implementation. R_1, R_X, R_4, and R_Y have been replaced with prime and double-prime components on either side of the filter, where

$R_1 = R'_1 \parallel R''_1$,
$R_X = R'_X \parallel R''_X$,
$R_4 = R'_4 \parallel R''_4$, and
$R_Y = R'_Y \parallel R''_Y$.

With the additional constraint that the impedance seen on each terminal of the filter is $2 \times Z_{DAC\pm}$, the following equations can be derived after quite a lot of algebra:

Figure 7. Inserting DAC image filter



$$\frac{1}{R'_1} = \frac{1}{2Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(max)}}-1}\right)} \quad \textbf{(12)}$$

$$\frac{1}{R''_1} = \frac{1}{2Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(max)}}-1}\right)} - \frac{1}{R_2+R_3} \quad \textbf{(13)}$$

$$\frac{1}{R'_X} = \frac{1}{2Z_{DAC+}} - \frac{1}{R'_1} \quad \textbf{(14)}$$

$$\frac{1}{R''_X} = \frac{1}{2Z_{DAC+}} - \frac{1}{R''_1} - \frac{1}{R_2+R_3} \quad \textbf{(15)}$$

$$\frac{1}{R'_4} = \frac{\left[1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{\frac{R_G}{2Z_{DAC-}}}\right]}{\frac{V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}+1} \quad \textbf{(16)}$$

$$\frac{1}{R''_4} = \frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{\frac{R_G}{2Z_{DAC-}}} + \left[\frac{V_{DAC+(min)}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)-V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}-1\right]\left(\frac{1}{R_G}\right)}{\frac{V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}+1} \quad \textbf{(17)}$$

$$\frac{1}{R'_Y} = \frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{2Z_{DAC-}} - \frac{1}{R'_4} \quad \textbf{(18)}$$

$$\frac{1}{R''_Y} = \frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{2Z_{DAC-}} - \left(\frac{1}{R''_4}+\frac{1}{R_G}\right) \quad \textbf{(19)}$$

These equations are easily solved when set up in a spreadsheet. To see an example Excel worksheet, click on the Attachments tab or icon on the left side of the Acrobat Reader window. Open the file DAC_Sink_to_Op_Amp_Wksht.xls, then select the "DAC Sink to Op Amp, With Filter" worksheet tab.

SPICE simulation is a great way to validate the design. To see a TINA-TI simulation comparing results with a filter used in the circuit, click on the Attachments tab or icon on the left side of the Acrobat Reader window. If you have the TINA-TI software installed, you can open the file DAC_Sink_to_Op_Amp_With_Filter.TSC to view the example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button. To show

the effects of balancing the filter impedance, a 100-MHz differential filter designed for 100-Ω input and output impedance is inserted into the interface of the DAC and op amp. In the top circuit, the filter is inserted between the bias resistors and amplifier gain resistors with no regard for balancing the impedance; the output is labeled "V_{OUT} No Match1." In the bottom circuit, the filter is inserted between the DAC and the bias resistors with no regard for balancing the impedance; the output is labeled "V_{OUT} No Match2." In the center circuit, the bias network is designed for 100-Ω balanced impedance; the output is labeled "V_{OUT} Matched." The transient simulation waveforms look the same as those shown in Figure 6 for each of these circuits, but simulation of an AC transfer function (see Figure 8) shows that the unmatched implementations result in significant ripple in the frequency response while the matched design performs as desired.

During design of the Texas Instruments TSW3070 evaluation board, a circuit was derived as shown in Figure 9 that appears to be well-balanced and that provides for proper impedance matching to the

Figure 8. Simulation of AC transfer function with matched vs. unmatched filter implementations

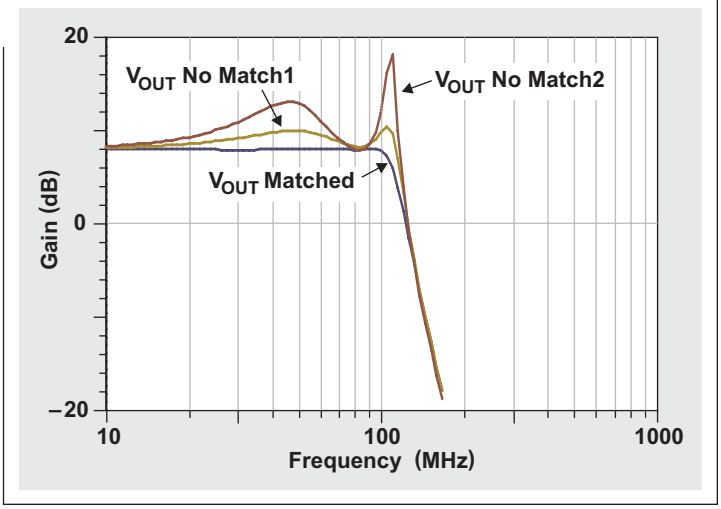
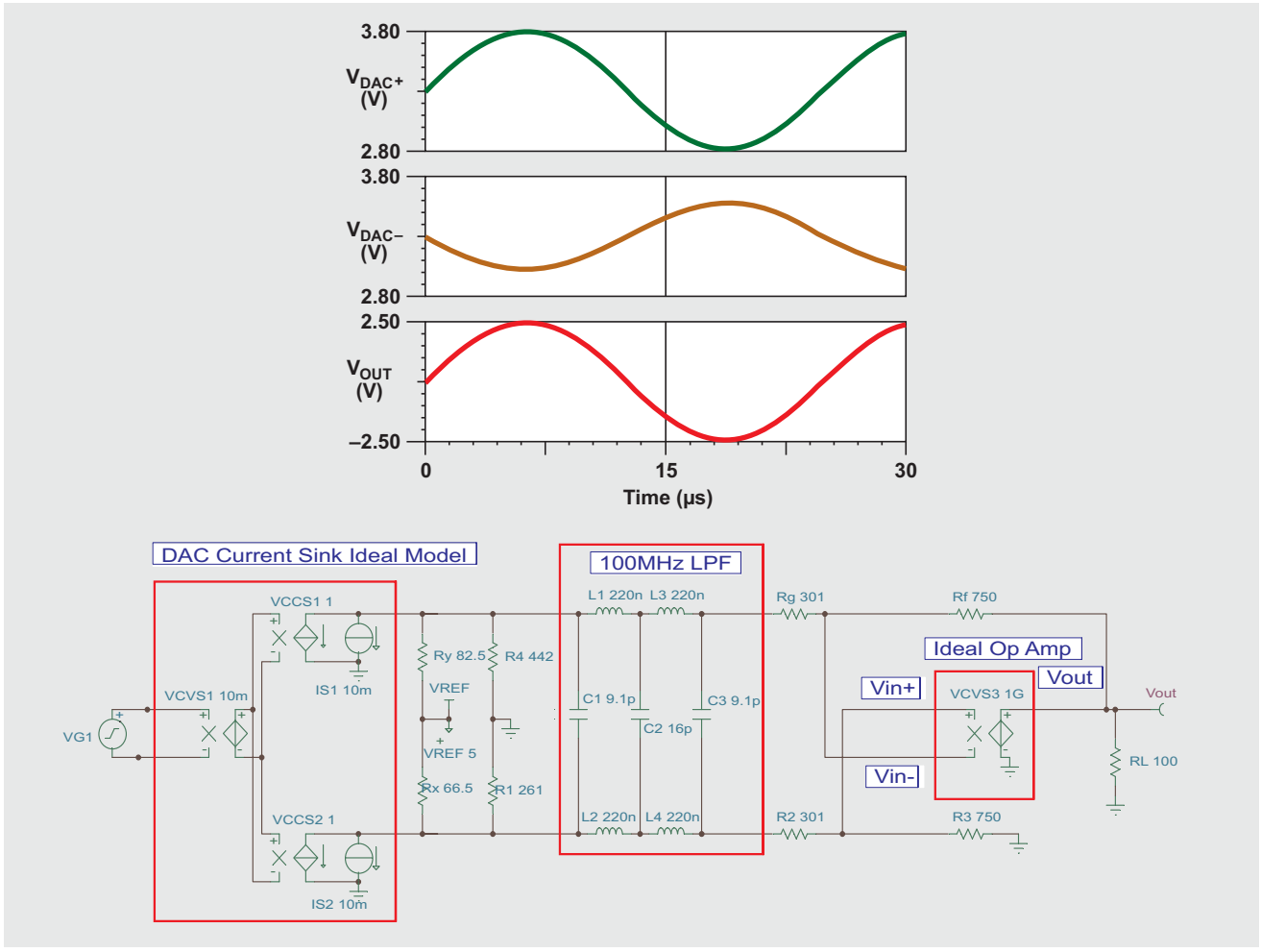


Figure 9. Original TSW3070 circuit simulation (not balanced)



100-MHz low-pass filter (LPF). However, the circuit's simulation waveforms show that the impedances seen by the outputs of the DAC are not balanced and that the voltage at V_{DAC+} is not the mirror image of that at V_{DAC-}. Per the last example given, this circuit was modified to balance the impedances for the DAC and the LPF. Performance of the second and third harmonics was tested before and after the modification, and the results (shown in Figure 10) show as much as a 10-dB improvement in the second harmonics (depending on the frequency) with basically no change in the third harmonics.

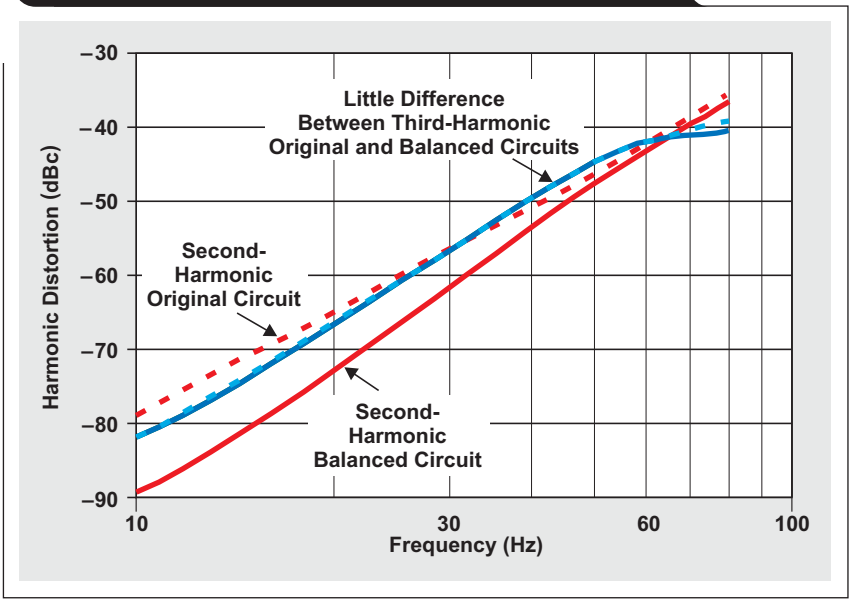
Conclusion

This article has shown a circuit implementation using a single-stage op amp to convert complementary-current outputs from a current-sinking DAC to a single-ended voltage. Equations were derived and a methodology presented for proper selection of component values to set the DAC's output-voltage compliance while maintaining balanced input signals to the op amp for best overall performance. Filter-design considerations were also included to explain proper insertion when filtering before the amplifier is desired.

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with DAC5675A, DAC5681, DAC5682Z, DAC5686, DAC5687, DAC5688, or THS3095
www.ti.com/tina-ti
www.ti.com/tsw3070

Figure 10. Harmonic distortion with balanced versus unbalanced impedance



Using the infinite-gain, MFB filter topology in fully differential active filters

By Thomas Kuehl
Senior Applications Engineer

Active filters are commonly employed in analog signal-conditioning applications. Some of the more common applications include tailoring a signal's bandwidth to reduce noise. One example of this is a low-pass anti-aliasing filter in front of an analog-to-digital converter (ADC); another is an anti-imaging filter that follows the output of a delta-sigma digital-to-analog converter (DAC) to remove unwanted high-frequency content. These filters—most commonly low-pass, high-pass, and band-pass filters—are often used to manage the amplitude response within a particular frequency range. The amplitude response may be tailored to track a particular pass-band or stop-band characteristic such as one provided by a Butterworth, Chebyshev, or Bessel filter. Filter-synthesis software is available from several sources, including Texas Instruments (TI). The synthesis programs and various on-line calculators allow for quick realization of practical filter designs. TI's FilterPro™ software accommodates all of the filters just mentioned.

Differential-amplifier and differential-input mixed-signal circuits such as ADCs are recognized for their inherent ability to reject common-mode signals and noise.[1] This ability provides a distinct advantage over the performance of single-ended-input/output ADCs, where unintended noise and signals may be processed along with the intended signal. Both the circuit complexity and the passive component count increase for a differential circuit, but maximizing system performance may easily justify the increased complexity. Like the basic differential-amplifier stages, differential active filters reject common-mode signals.

Designers often need to filter a signal as it is processed through the circuit's signal chain. In most instances the application calls for a low-pass filter. Other filters such as the band-pass, high-pass, band-reject, or an all-pass (used to create a specific time delay) are sometimes needed, but not nearly as often as the low-pass filter.

The Sallen-Key and infinite-gain, multiple-feedback (MFB) filter topologies are well-documented in filter literature, books, and on-line resources. Their popularity may stem from the fact that they require only one operational amplifier per second-order stage. Alternate topologies are available that provide a very precise filter response and offer lower component sensitivity; but they require two to four operational amplifiers per second-order stage, plus several additional precise passive components. Using one or more cascaded Sallen-Key or MFB stages often provides the necessary level of filter performance without resorting to more complex topologies.

The MFB configuration is one of the few topologies that readily lends itself to an application requiring a fully differential active filter because typical feedback paths run from the amplifier output back to only one input circuit—the inverting input circuit. The noninverting input is either biased at a common-mode potential or grounded, and no feedback is applied to it in its most common connection. The basic single-ended MFB filter topology can be used as the basis for developing a differential filter that has equivalent response characteristics. Nearly all other filter topologies require one or more feedback paths to each input of the operational amplifiers and are therefore more difficult to apply.

Transforming a single-ended-input/output filter into a fully differential filter

Filter handbooks and software don't always include topologies for differential filters, so knowing how to convert a single-ended-input/output filter to a fully differential filter when needed can save design time. For example, TI's FilterPro includes a provision for selecting a fully differential low-pass or high-pass filter but not a fully differential band-pass filter. Suppose the latter is needed. A basic single-ended MFB filter created with FilterPro can be used

as a starting point. The 10-kHz second-order Butterworth filter (Q = 0.707) shown in Figure 1 is used here as an example. Butterworth filters have a maximally flat pass-band response, which is a desirable trait for most analog signal paths. A higher-order Butterworth filter further flattens the pass-band response and provides higher attenuation in the stop band. The second-order filter used in this example provides an amplitude roll-off rate of –40 dB/decade, beyond the –3-dB cutoff frequency. For now, a value of 100 nF is selected for C2, and all the other components are allowed to float to their calculated values. FilterPro allows the designer to enter a capacitor value or a seed value for the input resistor; in this case, C2's value of 100 nF is entered. Once the filter requirements are entered into the program, the resulting values are displayed within a schematic of the filter.

A helpful FilterPro feature is that it selects standard capacitance values and then calculates the required resistances that meet the filter response. Often the resistor values are within the range of resistors with 1% tolerance. Capacitors with a tolerance of better than 5%, such as 2 or 1%, have limited availability. Resistors, by comparison, are commonly available with a tolerance of 1% and even 0.1%. Therefore, most of the filter component values can be covered without resorting to parallel or series combinations; but keep in mind that components with tight tolerances are required if a precise filter response is to be achieved.

The 10-kHz Butterworth low-pass filter shown in Figure 1 uses an OPA211 precision operational amplifier, which is well suited for this application because of its wide bandwidth and high gain at the filter's critical frequencies. Other operational amplifiers will also work but must have sufficient gain bandwidth (GBW) to support the filter's performance. More will be mentioned about this later.

Transforming the single-ended-input/output low-pass filter to a fully differential filter is really quite simple. The procedure is as follows: (1) Create a mirror of the single-ended filter circuit; (2) combine the circuit elements that connect to ground; and (3) replace the operational amplifier and its mirror with a fully differential operational amplifier. Viewing the circuit in Figure 2, which shows the single-ended low-pass filter and its mirror, aids understanding of this procedure.

The fully differential amplifier does not require the ground reference that a conventional operational amplifier uses, so the ground points in the circuit are no longer needed. Also, when the mirror was created, an extra input-voltage source and output meter were created; they

Figure 1. A 10-kHz single-ended Butterworth MFB input/output low-pass filter

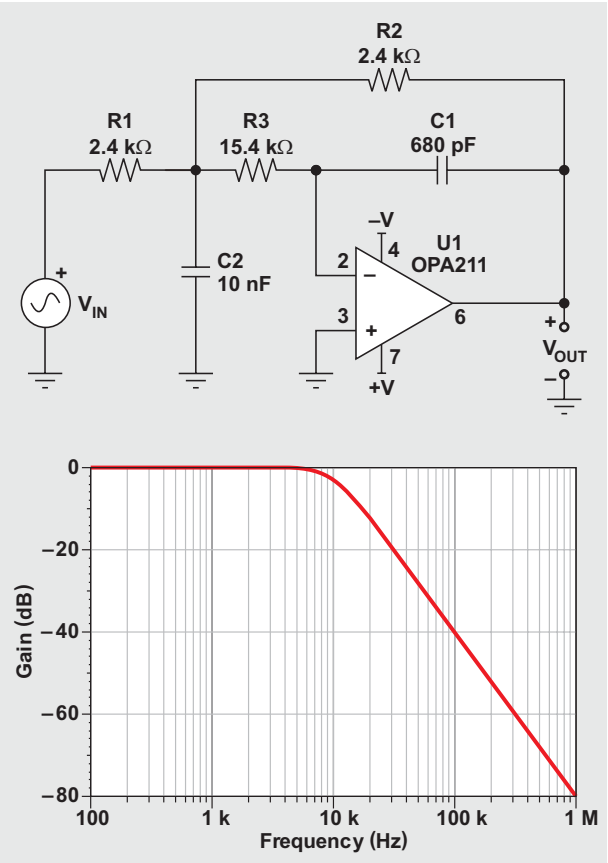
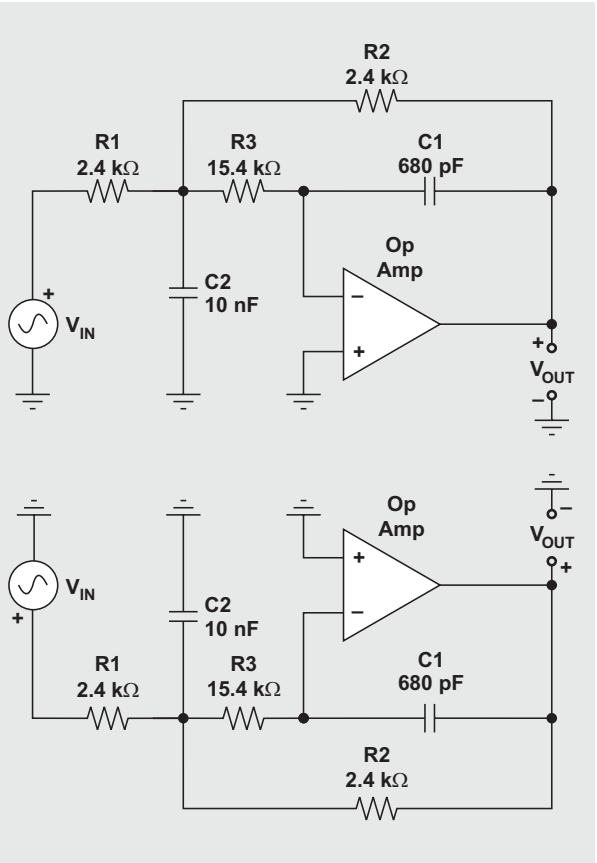


Figure 2. Mirroring the single-ended MFB input/output low-pass filter



are redundant and not required either. The capacitor C2 and the mirrored C2 are required, but their individual reactances can be combined in one capacitor. Once their ground connections are removed and they are connected together, they form a series connection. Therefore, C2 becomes common to both sides of the filter's input circuit, and its value is half of the original value. In the original low-pass filter, C2 had a value of 10 nF, but once the filter has been transformed, C2's final value is 5 nF. Lastly, the two conventional operational amplifiers are removed and replaced with one fully differential operational amplifier. In this case, a high-performance audio OPA1632 is selected. The transformed fully differential second-order low-pass filter is shown in Figure 3. A plot of gain versus frequency shows that the response is exactly the same for the fully differential and the single-ended filters.

By now it may be apparent why the value of C2 was preset to 10 nF. When a low-pass filter undergoes the transformation process, the capacitor ends up at half the original value. Selecting a capacitor value of 10 nF or 20 nF results in a transformed capacitor value of 5 nF or 10 nF, respectively. All of these are standard capacitor values. If C2 had originally been 4.7 nF, the transformed value would have been 2.35 nF, which isn't a standard value. Fortunately, when FilterPro synthesizes a fully differential filter, it always selects standard capacitor values and adjusts the resistor values to provide the correct response.

The transformation procedure may be just as easily applied to high-pass and band-pass filters. The resistors and capacitors of these filters lie in different positions within the MFB circuit than do those of low-pass filters. As a result, instead of the one capacitor and its mirror being reduced to one capacitor, a resistor and its mirror are combined into one resistor. That resistor requires twice the resistance of that used by the single-ended filter.

Figure 3. A transformed 10-kHz fully differential second-order Butterworth low-pass filter

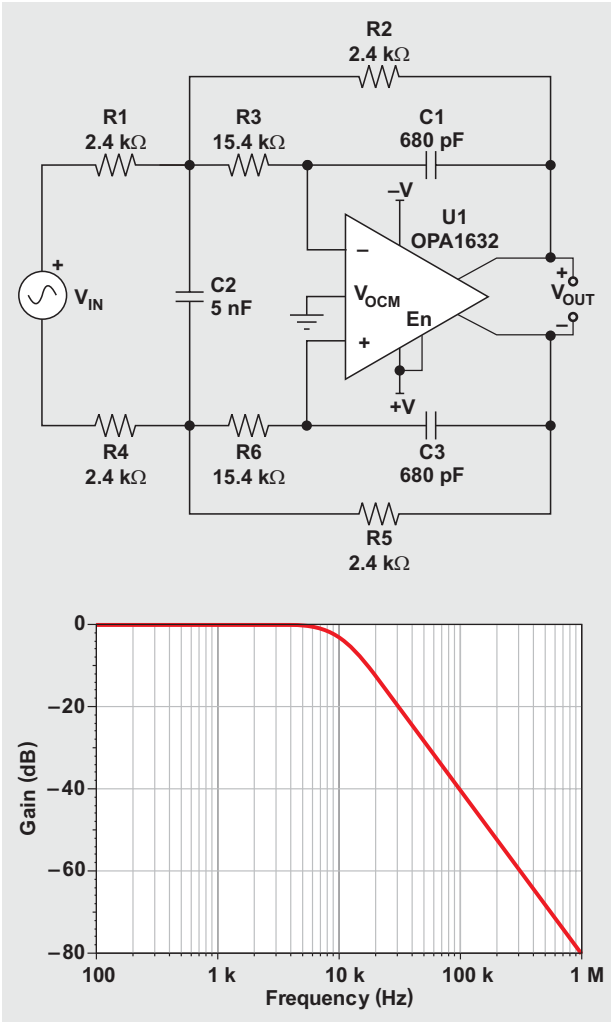


Figure 4. A 10-kHz (Q = 10) fully differential second-order Butterworth band-pass filter

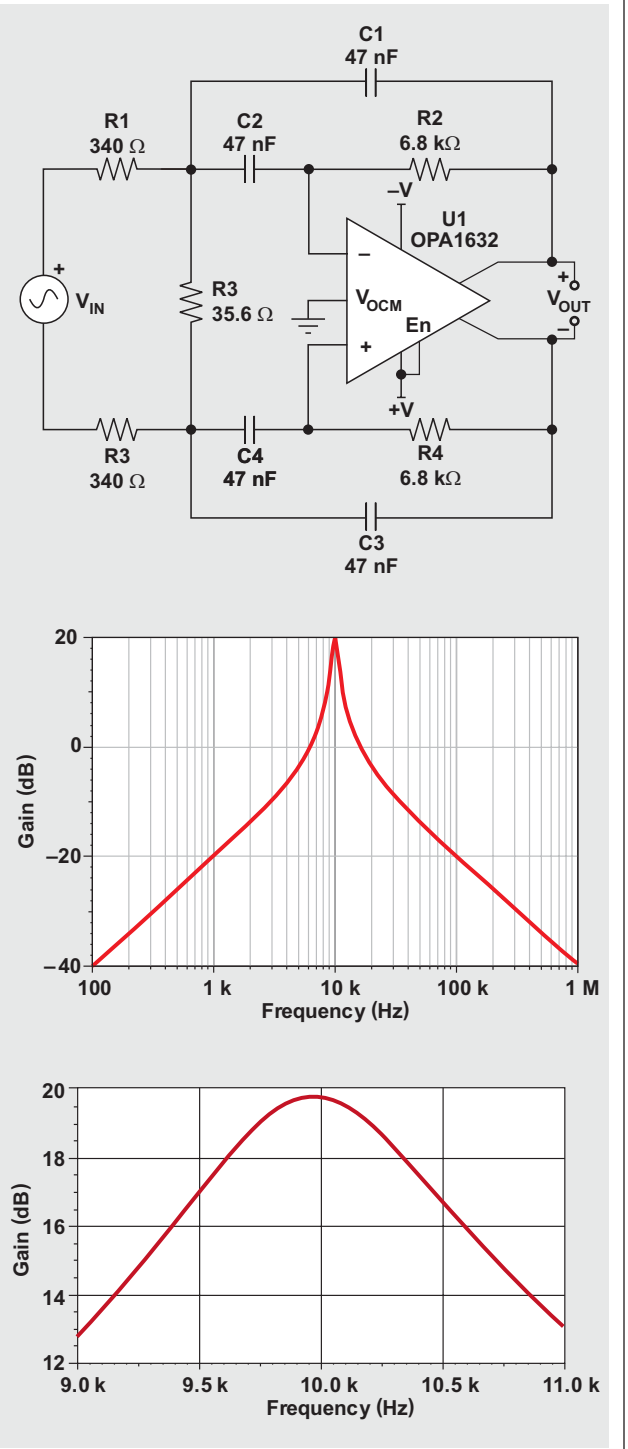


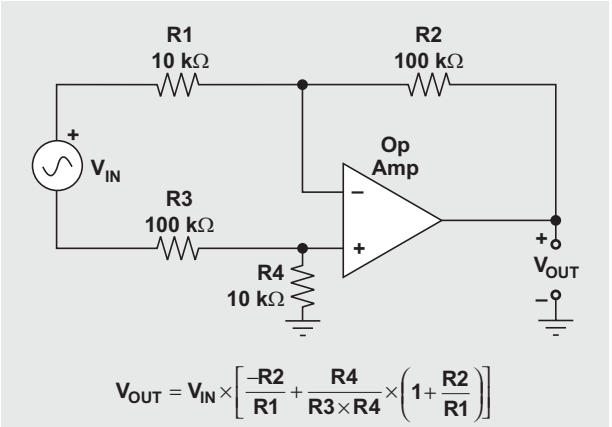
Figure 4 provides an example of a band-pass filter with a center frequency of 10 kHz, a –3-dB bandwidth of 1 kHz, and a gain of 10 V/V, with $Q_{bp} = 10$ ($f_C/BW_{-3\ dB}$). This filter was transformed via the same steps described earlier for the low-pass fully differential filter. Keep in mind that R3 is double the resistance required in a single-ended filter.

The differential-input, single-ended-output active filter

Up to this point, single-ended-input/output and fully differential active filters have been discussed. There are times, however, when an application requires a filter function provided by a differential input but requires only a single-ended output. System applications sometimes are configured with the input transducer or sensor entering the circuit differentially, while the remainder of the circuitry after the input stage operates in a single-ended fashion. Certainly the fully differential filter could be employed with one or the other output, but the amplifier involved likely offers more capability than is needed. Numerous fully differential operational amplifiers are available, but their parametric variety is limited when compared to the vast selection offered by conventional operational amplifiers. Thus, for the differential-input, single-ended-output filter, a conventional operational amplifier is a logical and often lower-cost option.

The differential-input, single-ended-output filter can be viewed as having similarities to the difference amplifier, which is comprised of a single operational amplifier and four resistors or impedances. An example schematic for a difference amplifier is shown in Figure 5. Note the differential inverting and noninverting inputs and the single-ended output. The ratios of R2 to R1 and R3 to R4 are

Figure 5. The basic difference amplifier



precisely matched such that the rejection of common-mode signals is maximized, and the amplification of differential signals is achieved with high gain accuracy. When it comes to the filter's case, the components are arranged to provide the differential filter function and to maintain input balance, just as the difference amplifier does.

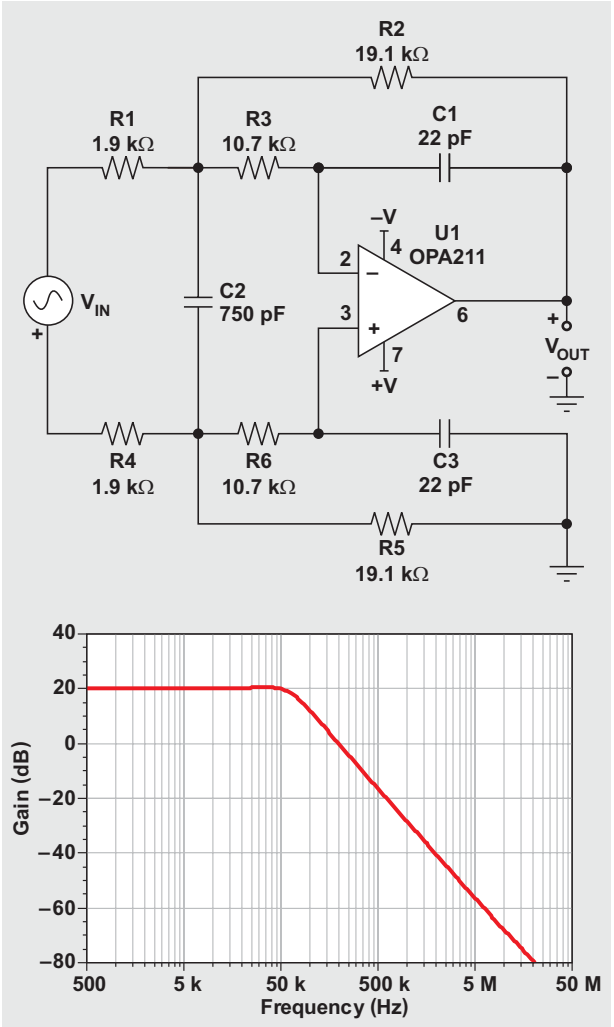
The procedure for transforming the single-ended filter to the differential-input, single-ended-output filter is the same as it was for creating the fully differential filter. A conventional operational amplifier replaces the fully differential operational amplifier and, since there is a single output, the circuit is connected a little differently. Instead of connecting from a differential output back to the noninverting input, the lower feedback network simply connects to ground. Viewing Figure 6 makes the connection easy to understand. The circuit and response are shown for a 50-kHz differential-input, single-ended-output, second-order 0.5-dB Chebyshev filter that has a gain of +10 V/V. The differential-input, single-ended-output configuration can be just as easily applied to band-pass and high-pass filters.

Considerations for practical active filters

Using filter software such as FilterPro can make designing filters straightforward and easy, but be aware that the component values resulting from such software or even from manual calculations may not always be completely satisfactory. The resistor and capacitor values derived may place impractical loading on the sensors that drive the filter, or on the operational amplifiers used in and/or around the filter circuit. This includes the input and feedback resistors in the filter. When using fully differential operational amplifiers such as the OPA1632, the designer should review the data sheet before using the feedback resistor value returned by a filter program or calculation. The OPA1632 is a very low-noise operational amplifier with a noise spectral density of about 1.3 nV/$\sqrt{\text{Hz}}$ (10 kHz). There may be the temptation to use large-value resistors to minimize capacitances, but those resistors can easily produce noise on their own that exceeds that of the OPA1632. The capacitance associated with amplifier input in conjunction with a large feedback resistance creates a pole in the response that degrades the amplifier's closed-loop bandwidth and phase margin. Therefore wideband amplifiers like the OPA1632 most often use small-value feedback resistors to preserve the amplifier's bandwidth. The same precautions must be observed whether the operational amplifier is conventional or fully differential.

Circuit designers are sometimes surprised to find that the filter response of the actual filter is not as expected. The filter exhibits inexact gain, incorrect cutoff or center

Figure 6. A 50-kHz, differential-input, single-ended-output, second-order 0.5-dB Chebyshev low-pass filter (A_V = +10 V/V)



frequencies, or incorrect pass-band or stop-band response characteristics. Most often this is the result of the operational amplifier having insufficient closed-loop gain at frequencies critical to the filter's performance. Surprisingly high GBW may be required of the operational amplifier, especially when a filter's operating frequency is increased, the stage gain is high, and the filter must accurately reproduce the pass-band ripple characteristics. For best MFB performance, it is recommended that any one stage's filter Q be 10 or less.

FilterPro performs a GBW calculation for both the low-pass and high-pass filters. The GBW returned is a simple approximation based on the following:

$$GBW_{Section} = G \times f_n \times Q,$$

where G is the section or stage gain (V/V), f_n is the section's natural frequency, and Q is related to the stage-damping factor, $Q = 1/(2\zeta)$. FilterPro provides the G, f_n, Q, and GBW product (listed as "GBP") in a table that summarizes the filter characteristics of each stage. This simple approximation may be used as a starting point for the other filter responses as well. More exacting GBW results may be obtained from the formulas listed in Reference 2.

Fortunately, some operational amplifiers have SPICE simulation models that accurately model the AC and transient behaviors. That is the case for both the OPA211 and OPA1632 mentioned in this article. Once the particular filter has been defined and synthesized, the filter components and operational amplifiers can be tested with a simulator such as TI's TINA-TI™ or one of the many other SPICE-based simulators.

The test run should provide an accurate account of a particular filter's true AC and transient behaviors. Any unexpected distortions in the filter performance should become evident from the simulations. Using the simulation approach is a good place to start before the actual filter is built and bench tested. All of the filter responses shown in this article were obtained from TINA-TI SPICE simulations.

References

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Document Title	**TI Lit. #**
1. Jim Karki, "Fully differential amplifiers remove noise from common-mode signals," *EDN* (November 9, 2000), pp. 149–156.	—
2. Ron Mancini, Ed., "Op Amps for Everyone," Design Reference, Section 16.8.4, pp. 16-53–16-54	slod006

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