# QIPENG WANG

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#### **EDUCATION**

## Harbin Institute of Technology, China

Aug. 2016 - Jun. 2020

- BEng. in Communication Engineering, GPA: 88.72/100
- GRE: 325 (Quantitative:169 Verbal:156 Analytical Writing:3.5)
- TOEFL: 104 (Reading:27 Listening:27 Speaking:23 Writing:27)
- Core Courses: Foundation of Internet of Things, Computer and Communication Networks, Wireless Ad Hoc Networks, Multimedia Communication Networks

#### **PUBLICATION**

[1] Zhiming Huang, Yifan Xu, Bingshan Hu, Qipeng Wang, Jianping Pan. Thompson Sampling for Combinatorial Semi-bandits with Sleeping Arms and Long-Term Fairness Constraints. Ready for submission. (https://arxiv.org/pdf/2005.06725.pdf)

#### RESEARCH EXPERIENCE

**Department of Computer Science**, University of Victoria, Canada *Mitacs Globalink Research Internship*, Supervisor: Jianping Pan

Jul. 2019 - Oct. 2019

- Proposed a Thompson-Sampling based online learning algorithm with fairness guarantee.
- Simulated the regret bound and compared our work with the existing work.
- Co-authored a paper and submitted it to *IJCAI*.

Communication Research Center, Harbin Institute of Technology, China Jun. 2018 - Present Research Internship, Supervisor: Yulong Gao

- Proposed an online learning based algorithm for dynamic spectrum access in Cognitive Radio Networks
- Simulated the performance of the algorithm using Matlab.
- · Preparing a paper.

#### ACADEMIC PROJECTS

## Modulation Mode Recognition Based on SDR

Apr. 2019 - May 2019

Supervisor: Zhiming Yang

- Applied BP Neural Network to recognize different modulation modes based on SDR platform.
- Achieved high accuracy (over 95%) of recognition in different SNR conditions.
- Presented this project in the class.

#### **AM Transceiver Hardware Platform**

Dec. 2018 - Jan. 2019

Supervisor: Yaqin Zhao

- Led a team of three students and designed the whole framework using Multism.
- Developed the hardware platform and achieved required performance indexes.

# Serial Communication System Based on FPGA

Jun. 2018 - Jul. 2018

Supervisor: Wenchao Yang

• Developed Baud Rate Generator module, Transmitter module, Reciever module using language Verilog HDL based on FPGA.

• Achieved the two-way serial communication between the FPGA and the PC.

## Wearable Navigation Glasses for the Blind

Aug. 2017 - May 2018

Supervisor: Yulong Gao

- Designed the whole framework including Recognition module, Ultra-sound module and Voice broadcast module.
- Developed the Recognition module using OpenCV and improved the edge detection algorithm.
- Won 2nd Prize in Electronic Innovation Competition.

## AWARDS & SCHOLARSHIPS

CSC(China Scholarship Council) Scholarship for Research Internsh	ip		Jun.	2019
HIT Scholarship (for five times)	Mar.	2017 -	May.	2019
Travel Grant for Kaist ECE Camp			Sep.	2018
Won 3rd Prize in National Mathematics Competition			Sep.	2017
Won 2nd Prize in Electronic Innovation Competition at HIT			Jul.	2017
Won 1st Prize in Winter Vacation Social Practice			Feb.	2017

## **SKILLS**

Software Skills: C, Matlab, Verilog, Multism, Simulink, Labview, LaTex

Languages: English, Mandarin

## **ACTIVITIES**

Volunteer in IEEE Pacrim Conference, Victoria	Aug. 2019
Kaist ECE Camp, Korea Advanced Institute of Science and Technology	Sep. 2018
Vice President of Students' Environment Protection Union, HIT	Sep. 2016 - Sep.2017