Cs223-03

Lab03

Osman Buğra Aydın

21704100

25 October 2020

B-) Behavioral SystemVerilog module for 2-to-4 decoder

```
`timescale 1ns / 1ps

module BehavioralTwoToFourDecoder( input a0, a1, output b0, b1, b2,
b3 );

    assign b0 = a0 & a1;
    assign b1 = a0 & ~a1;
    assign b2 = ~a0 & a1;
    assign b3 = ~a0 & ~a1;

endmodule
```

Testbench

```
`timescale 1ns / 1ps
module BehavioralTwoToFourDecoder_tb;

    reg a0, a1;
    wire b0, b1, b2, b3;

    BehavioralTwoToFourDecoder
uut( .a0(a0), .a1(a1), .b0(b0), .b1(b1), .b2(b2), .b3(b3) );

    initial
        begin
            #300

            #30; a0 = 0; a1 = 0;
            #30; a0 = 1; a1 = 0;
            #30; a0 = 0; a1 = 1;
            #30; a0 = 1; a1 = 1;
        end

endmodule
```

C-) Behavioral SystemVerilog module for 4-to-1 multiplexer

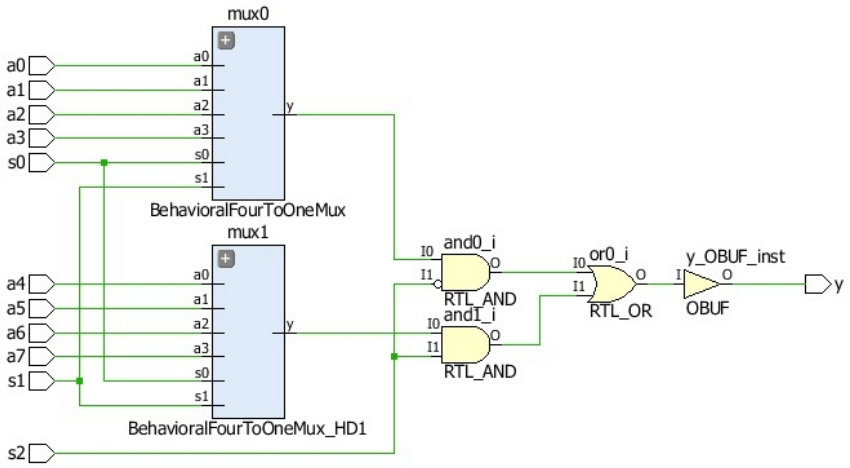
```
`timescale 1ns / 1ps

module BehavioralFourToOneMux( input a0, a1, a2, a3, input s0, s1,
output y );

   assign y = a0 & ( ~s0 & ~s1 ) | a1 & ( s0 & ~s1 ) | a2 & ( ~s0 & s1 ) | a3
& ( s0 & s1 )  ;

endmodule
```

Testbench

```
`timescale 1ns / 1ps

module BehavioralFourToOneMux_tb;

   reg a0, a1, a2, a3, s0, s1;
   wire y;

   BehavioralFourToOneMux uut
( .a0(a0), .a1(a1), .a2(a2), .a3(a3), .s0(s0), .s1(s1), .y(y) );

   initial
      begin
         #300

         #30; a0=1; a1=0; a2=0; a3=0; s0=0; s1=0;
         #30; a0=0; a1=1; a2=0; a3=0; s0=1; s1=0;
         #30; a0=0; a1=0; a2=1; a3=0; s0=0; s1=1;
         #30; a0=0; a1=0; a2=0; a3=1; s0=1; s1=1;
      end

endmodule
```

D-) Structural Module of 8-to-1 MUX

Schematic



SystemVerilog

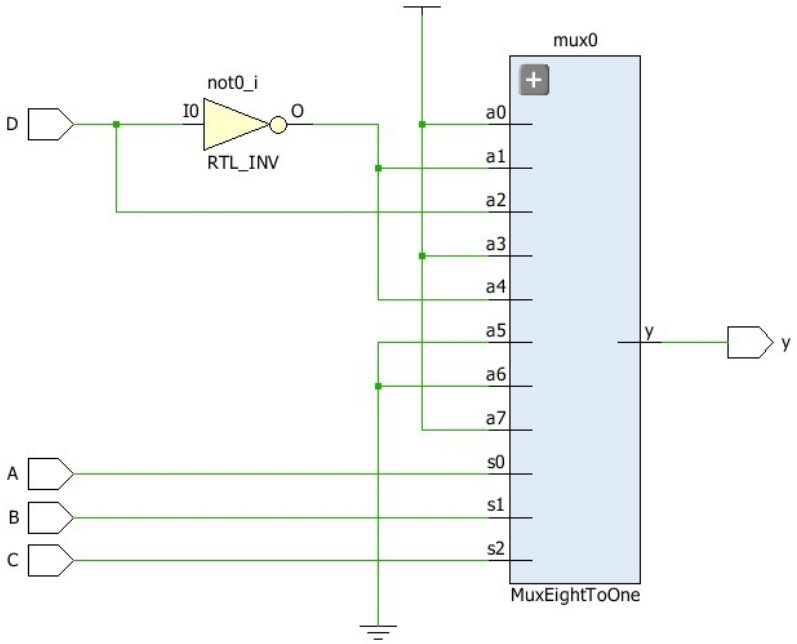
```
`timescale 1ns / 1ps

module MuxEightToOne( input a0, a1, a2, a3, a4, a5, a6, a7, input s0, s1, s2, output y );

    wire w0, w1, w2, w3, w4;

    BehavioralFourToOneMux mux0( a0, a1, a2, a3, s0, s1, w0 );
    BehavioralFourToOneMux mux1( a4, a5, a6, a7, s0 ,s1, w1 );

    not not0( w2, s2);
    and and0( w3, w0, w2 );

    and and1( w4, w1, s2 );

    or or0( y, w3, w4 );

endmodule
```

Testbench

```
`timescale 1ns / 1ps

module MuxEightToOne_tb;

    reg a0, a1, a2, a3, a4, a5, a6, a7;
    reg s0, s1, s2;
    wire y;

    MuxEightToOne
uut( .a0(a0), .a1(a1), .a2(a2), .a3(a3), .a4(a4), .a5(a5), .a6(a6), .a7(a7), .s0(
s0), .s1(s1), .s2(s2), .y(y) );

    initial
        begin
            #300

            #30; a0=1; a1=0; a2=0; a3=0; a4=0; a5=0; a6=0; a7=0; s0=0; s1=0;
s2=0;
            #30; a0=0; a1=1; a2=0; a3=0; a4=0; a5=0; a6=0; a7=0; s0=1; s1=0;
s2=0;
            #30; a0=0; a1=0; a2=1; a3=0; a4=0; a5=0; a6=0; a7=0; s0=0; s1=1;
s2=0;
            #30; a0=0; a1=1; a2=0; a3=1; a4=0; a5=0; a6=0; a7=0; s0=1; s1=1;
s2=0;
            #30; a0=0; a1=0; a2=0; a3=0; a4=1; a5=0; a6=0; a7=0; s0=0; s1=0;
s2=1;
            #30; a0=0; a1=1; a2=0; a3=0; a4=0; a5=1; a6=0; a7=0; s0=1; s1=0;
s2=1;
            #30; a0=0; a1=0; a2=1; a3=0; a4=0; a5=0; a6=1; a7=0; s0=0; s1=1;
s2=1;
            #30; a0=0; a1=0; a2=0; a3=0; a4=0; a5=0; a6=0; a7=1; s0=1; s1=1;
s2=1;

        end

endmodule
```

E-) F(A,B,C,D)=∑(0,1,3,4,7,8,10,11,15) Function

Schematic



SystemVerilog

```
`timescale 1ns / 1ps

module SpecialFunction( input A, B, C, D, output y );

    wire notD;

    not not0( notD, D );

    MuxEightToOne mux0( 1, notD, D, 1, notD, 0, 0, 1, A, B, C, y );

endmodule
```

Testbench

```
`timescale 1ns / 1ps


module SpecialFunction_tb;

    reg A, B, C, D;
    wire y;

    SpecialFunction uut( .A(A), .B(B), .C(C), .D(D), .y(y) );

    initial
        begin
            #300

            #30; A=0; B=0; C=0; D=0;
            #30; A=1; B=0; C=0; D=0;
            #30; A=0; B=1; C=0; D=0;
            #30; A=1; B=1; C=0; D=0;
            #30; A=0; B=0; C=1; D=0;
            #30; A=1; B=0; C=1; D=0;
            #30; A=0; B=1; C=1; D=0;
            #30; A=1; B=1; C=1; D=0;
            #30; A=0; B=0; C=0; D=1;
            #30; A=1; B=0; C=0; D=1;
            #30; A=0; B=1; C=0; D=1;
            #30; A=1; B=1; C=0; D=1;
            #30; A=0; B=0; C=1; D=1;
            #30; A=1; B=0; C=1; D=1;
            #30; A=0; B=1; C=1; D=1;
            #30; A=1; B=1; C=1; D=1;

        end

endmodule
```