Profile Information
RV-VLSI ID: 1ADADB263506

Career Objective

- To make a career in the field of VLSI that provides the scope for continuous learning, growth, responsibility and ownership.

Core Competancy

- Sound knowledge on the complete ASIC Design Flow.
- Excellent communication skills with talent for problem solving.
- Knowledge/Experience of Physical Design concepts.
- Good understanding of Digital electronics and the field of Digital Systems Design.
- TCL and Perl scripting.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design - Physical Design	RV-VLSI Design Center	2015	-
Degree	Electrical and Electronics	Adichunchanairi Institute Of Technology	2011	70
PUC	-	Aurobindo Pre University	2007	65
SSLC	-	Poorna Prajna Education Centre	2005	90

Project Details

Project Title	Block Level Implementation Of Torpedo Processor using 180nm Technology
Institue Name	RV-VLSI Design Centre
Project Description	Block level implementation of Torpedo sub-system with an intent to capture the various aspects and challenges of Physical Design flow.
Tools Used	Synopsys IC Compiler
Challenges	Creating the optimized floorplan. Synthesis of power rails so as to meet the IR drop constraints. Timing closure of setup post 43k cells placement. Generating the optimized clock tree, meeting the target skew and fixing hold or setup violation.

Project Title	Static Timing Analysis using Synopsys-PrimeTime
Institue Name	RV-VLSI Design Centre
Project Description	Static timing analysis plays a vital role in facilitating the fast and reasonably accurate measurement of circuit timing. Project intended a detailed study of timing calculation and timing report analysis.
Tools Used	Synopsys-PrimeTime

Challenges	Understanding the timing arcs and their delay representation in the delay table. Performing timing calculation. Analyzing the timing report of register-to-register, input port-to-register, register-to-output port, input port-to-output port.