Profile Information
RV-VLSI ID: 1ADADB263529

Career Objective

- To become a productive and energetic full custom layout engineer by working on present as well as advanced process nodes.

Core Competancy

- Capability to debug special type of lvs errors like short errors,open errors,property errors.
- Experience of formal verification to produce clean gds standard cell.
- Understanding the CMOS fabrication concepts.
- Realizing the need to check and understand foundary document before laying out.
- Need for dfm.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design - Full Custom	RV-VLSI Design Center	2015	-
Degree	Electronics and Communication	South East Asian college of engineering and technology	2014	68
PUC	-	KV NAL	2010	73(CBSE)
SSLC	-	KV NAL	2008	68(CBSE)

Project Details

Project Title	To verify and understand lvs errors in standard cells
Institue Name	RV-VLSI
Project Description	Standard cell layout was given already in ICStudio, the main objective was to understand and verify lvs errors for the given layout.
Tools Used	Tool used for the verification of lvs was on Caliber by Mentor Graphics.
Challenges	1)understanding open and short errors was interesting as well challenging.. 2)Resolving the connectivity errors like soft check errors was another challenge factor. 3)To understand errors in power and ground nets to be first priority.

Project Title	To layout 9 Track standard cells using 90nm to provide lvs and drc clean gds.
Institue Name	RV-VLSI
Project Description	Technology used to design the Standard cells is 90nm process.Standard cells were designed to provide clean lvs and drc gds library.The cells were designed to provide least parasitic by using multiple contacts when possible and by efficient routing.
Tools Used	Layout design was performed in PYXIS(ICStudio) by Mentor Graphics ,while the verification of the layout was done using Caliber tool.

Challenges	1)Efficient routing while considering large and complex layouts. 2)Routing to be done in order to reduce parasitic. 3)Best floor planning within the PRboundary was challenging.

Project Title	To layout 7 Track standard cells using 38nm to provide lvs and drc clean gds.
Institue Name	RV-VLSI
Project Description	Technology used to design the Standard cells is 28nm process.Standard cells were designed to provide clean lvs and drc gds library.The cells were designed to provide least parasitic and routing within the given PRboundary constraints.
Tools Used	Layout design was performed in PYXIS(IC Studio) by Mentor Graphics ,while the verification of the layout was done using Caliber tool.
Challenges	1)Poly routing was challenging. 2)The need to put poly and contacts on the grid was challenging. 3)Use of metal1 without the use of higher metal to provide efficient route was challenging.

Project Title	2 stage opamp layout floor plan design using 180nm
Institue Name	RV-VLSI
Project Description	2-stage op-amp layout is designed with appropriate floor planning. The layout is done in a way to avoid mismatches. Layout is designed by considering matching techniques like centroid , dispersion , compactness and symmetry.
Tools Used	Layout design was performed in PYXIS(IC Studio) by Mentor Graphics ,while the verification of the layout was done using Caliber tool.
Challenges	1)Floorplanning considering matching techniques was an challenge within the given area parameters. 2)Considering matching techniques like centroid,dispersion,compactness and symmetry together was an challenging issue.. 3)Least parasitic layout design

Project Title	Layout design of Leaf Cells used in 6TSRAM Memory Compiler using 28nm
Institue Name	RV-VLSI
Project Description	This project is yet to be completed, as of now understood the basics of 6T sram.
Tools Used	Layout design was performed in PYXIS(IC Studio) by Mentor Graphics ,while the verification of the layout was done using Caliber tool.
Challenges	Though the project is yet to be completed the challenges expected are 1)placing the pins across the periphery of the cells to provide efficient connection. 2)efficient routing within the given area.

Project Title	To review 180nm, 90nm and 28nm process rule file
Institue Name	RV-VLSI
Project Description	To review and understand the drc file, lvs file and foundary document files for all the three process node technology.
Tools Used	Jazz semiconductors-foundary document.
Challenges	1)Is challenging and interesting to understand the variations in all three process node technologies while referring the rule files .e 2))variations in all three process node technologies.

Project Name	DESIGN TO TEST SUBSYSTEM OF DATA HANDLING REMOTE TERMINAL (DHRT) USING FPGA WITH THE IMPLEMENTATION OF MIL STD 1553B INTERFACE.
Institute Name	South East Asian college of engineering and technology
Project Description	It is working reference for testing of subsystems(telemetry, telecommanding,BDH signals,AOCE) of satellite using fpga which is configured using VHDL.
Challenges	Generation of 40KHz clock was little challenging for storage and playback subsystem.
Tools	Software tool used was Modelsim from Mentor Graphics for VHDL programming