Profile Information
RV-VLSI ID: 1ADADB263507

Career Objective

- As a fresher, my objective to join a reputed organization use my knowledge and skills for the growth of the organization and enhance my own skill

Core Competancy

- Good understanding of CMOS Transistor fundamentals.
- Have knowledge and experience working with floorplan, placement, clock tree synthesis, routing and optimization
- Good Knowledge in understanding and resolving timing violations (hold and setup) of various timing paths (STA)
- Good Knowledge of ASIC flow and the stages involved in physical design flow.
- Exposure to industry standard EDA tools like IC Compiler, Prime Time and Hercules from Synopsys
- Basic knowledge of power reductions techniques.
- Good knowledge of Linux and Scripting using Perl and Tcl for automation.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-
Degree	Electronics and Communication	Jaya Engineering College	2014	6.3
PUC	-	krishna chaitanya	2010	78
SSLC	-	Ravindhra bharathi	2008	65

Project Details

Project Title	Torpedo Block
Institue Name	RV-VLSI Design Center
Project Description	Physical Design and Implementation of block level design consisting of 32macros,43K standard cells and operate on 400 MHz incorporated with 5Clocks,with a supply voltage of 1.8V with 5% max IR drop and power budget of300mW implemented with 6 layers
Tools Used	ICCompiler, Prime Time, Hercules from Synopsys, Calibre from Mentor Graphics.
Challenges	Placement of macros with restricted orientations and to avoid stacking of macros, have done multiple iterations to come up with an efficient floor plan. Encountered a lot of congestion between and on the macros and on the standard cells.

Project Title	Static Timing Analysis

Institue Name	RV-VLSI Design Center
Project Description	STA for Register and latch based design with different constraints such as variation in skew, uncertainity, input and output delays and also with timing exceptions. Generate setup and hold reports to solve/analyze cause for timing path violations.
Tools Used	Primetime from Synopsys
Challenges	Identifying and Resolving the cause for Setup and Hold violations such as Input transition,Load Capacitance,Insertion delay,Cell delay was challenging.

Project Title	Analysing TCL Scripts
Institue Name	RV-VLSI Design Center
Project Description	Written scripts to extract data from the ICC DB. Analyzed the TCL scripts for the templates of floor plan, power plan,placement,CTS,Routing,and customizing them to our flow.Analyzed reports generated by the IC compiler
Tools Used	Tclsh, TCL tutor, Linux OS
Challenges	Learning TCL from scratch,Understanding each command in the script using man pages.Debugging TCL Scripts, writing TCL to design examples

Project Name	Network Time Display
Institute Name	Jaya Engineering College
Project Description	Objective is to hold time and reduce the timing losses while transferring network packet distributed by Timing Station from one location to another
Challenges	The entire operation carried out during a launch of a rocket is with respect to Countdown Time sent by Timing Station. All data and information collected by various ground stations are time-tagged for accurate correlation and further analysis
Tools	Using C Concepts in a microcontroller