## **Profile Information**

RV-VLSI ID: 1ADADB263524

## **Career Objective**

• Looking for a responsible position as a VLSI design engineer with a view to utilize and enhance my skills and experience towards professional growth

## **Core Competancy**

- Good understanding of the CMOS Design, Digital Design, ASIC design flow.
- Expertise in Synthesis and Physical Design.
- Good knowledge in Static Timing Analysis .
- Good understanding in IR-DROP and OCV.
- Knowledge about device physics.
- Knowledge in basic commands of LINUX.

	Education Details				
Degree	Discipline	School/College	Year of passing	Aggregate	
II I	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-	
Master Degree	VLSI Design and Testing	Centre		7.2	
Degree	Electronics and Communication	R.V.S College of Engineering and Technology	2011	6.33	
PUC	-	Holy Trinity School	2007	82	
SSLC	-	International Indian School	2005	83.4	

## **Project Details**

Project Title	Block level implementation of Torpedo system
Institue Name	RV-VLSI
II I AAIE I IEAA	IC Compilerâ€"Floor Planning, Place & Route, and clock tree synthesis PrimeTimeâ€"Static Timing Analysis and Crosstalk Analysis

Project Name	Emergency Management System using GPS and GSM Technology
Institute Name	R.V.S College of Engineering and Technology
	A module that helps monitoring a vehicle 24X7 and providing exact location at the time of crisis to emergency system
Challenges	Understanding about embedded C, interfacing of controller with sensor
Tools	Hardware used: LCD display, 8051 microcontroller, vibrator sensor Software used: Keil compiler

Project Name	A Low Computational Complexity based MIMO-OFDM system
Institute Name	Nehru College of Engineering and Research Centre
Project Description	A low computational algorithm that reduces the iteration time through the sub- channel. An OFDM is included across the transceiver to reduce the high level complexity of the transceiver.
Challenges	Interfacing of the MIMO-OFDM module
Tools	Software used: Xilinx ISE 9.1e