Profile Information

Name: KISHORE P **Email:** kishore.p085@gmail.com

Career Objective

- To obtain a position of responsibilities that utilizes my skills and keen to work in an environment where I can enrich my knowledge in Physical Design

Core Competancy

- Good knowledge of ASIC flow
- Well versed in STA, Floor planning, APR, CTS
- Ability to analyse timing reports
- Good understanding in RTL design and verification using verilog
- Good knowledge of CMOS concepts
- Good knowledge of digital design concepts

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design - Physical Design	RV-VLSI Design Center	2015	-
Master Degree	VLSI & ES	Bangalore Institute of Technology	2015	70.19
Degree	Electronics and Communication	A.P.S. College of Engineering	2013	67.63
PUC	-	Nisarga indp PU college	2009	81.16
SSLC	-	Christaraja high school	2007	81.44

Project Details

Project Title	Block level physical design of Torpedo subsystem using 180nm technology
Institue Name	RV-VLSI
Project Description	Torpedo subsystem is block level physical design of an image processor. It has 32macros with supply voltage of 1.8v with 45mv max of IR drop, 300mW power budget and operated at 400MHz. It has 5 clocks. FAB:Jazz Semiconductor, 180nm technology is used
Tools Used	Synopsis IC Compiler, Primetime, Hercules
Challenges	Analysing timing reports, Floor planning

Project Name	Voice controlled wireless smart home
Institute Name	A.P.S. College of Engineering
Project Description	Project involves controlling of home electrical devices like Fan, light etc. using our voice commands. It is also used to control wheel chair.
Challenges	Understanding EasyVR module

Tools	Hardware : Atmega8, Atmega328p, EasyVR, Transceiver module Software : Arduino, EasyVR

Project Name	Modified microprogrammable FIR filter architecture for ASIC design and FPGA implementation
Institute Name	Bangalore Institute of Technology
Project Description	The designing of architecture is divided into two parts. Direct form of FIR filter is designed in datapath unit. The whole operation of datapath unit is controlled with control unit. Hence controllability of the architecture is increased.
Challenges	Designing the ROM for control unit.
Tools	Software : Cadence RTL compiler, Xilinx ISE, Matlab Hardware : Spartan - 3 (XC3S400 - PQ208)