

## Profile Information

RV-VLSI ID: 1ADADB216001

## Career Objective

- To contribute my skills sets to the organization to achieve the goals and targets that enhance my professional and personal growth

## Core Competancy

- Good knowledge of CMOS device physics and transistor operation
- Good knowledge of Digital Design Concepts
- Good working experience on 180nm, 90nm & 28nm technology nodes
- Understanding of layout dependent proximity effects like wpe & lod
- Good knowledge of SRAM architecture & layout design
- Good knowledge of CMOS device physics and transistor operation
- Good knowledge of Digital Design Concepts
- Good working experience on 180nm, 90nm & 28nm technology nodes
- Understanding of layout dependent proximity effects like wpe & lod
- Good knowledge of SRAM architecture & layout design

Education Details				
Degree	Discipline	School/College	Year of passing	Aggregate
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2014	-
Degree	Electronics and Communication	Manipal Institute of Technology, Manipal	2013	5.98
PUC	-	Gomatesh Polytechnic, Belgaum	2009	71.07%
SSLC	-	Composite Sports English Medium High School, Chandargi	2006	76.80%

## Project Details

<b>Project Title</b>	"Leaf Cell Design Of Memory Compiler Using 28nm Technology Node"
<b>Institute Name</b>	RV-VLSI DESIGN CENTER
<b>Project Description</b>	The project consists of designing different blocks used in constructing memory cell: 1)Sense Amplifier 2)Precharge block 3)Controller 4)Pre-decoder 5)Final decoder 6)Input and output driver
<b>Tools Used</b>	ICstudio from Mentor Graphics- 1)Pyxis (Schematic and Layout editor) 2)Calibre (DRC, LVS, PEX check)
<b>Challenges</b>	1)Making complete layout within the given PR-Boundary 2)Placing all contacts and poly <sup>™</sup> s on grid following all DRC rules 3)Proper routing keeping word lines (WL) in horizontal and bit lines (BL) at vertical directions 4)Using dedicated metals at pa

<b>Project Title</b>	"Standard Cell Library Design Using 28nm Technology Node"
<b>Institute Name</b>	RV-VLSI Design Center
<b>Project Description</b>	Design Schematic and Layout of Standard Cells like: 1) INVX12) INVX23) AND2X14) NAND2X15) NAND2X26) NAND2X37) NOR3X18) NOR3X29) NOR3X410) OR3X111) OR3X212) OR3X4
<b>Tools Used</b>	ICstudio from Mentor Graphics-1) Pyxis (Schematic and Layout editor)2) Calibre (DRC, LVS, PEX check)
<b>Challenges</b>	1) Making the layout within the PR-Boundary. 2) Placing of polys and contacts on grid.3) Reducing the parasitics.4) To make optimized layout with proper routing.

<b>Project Title</b>	"Standard Cell Library Design Using 90nm Technology Node"
<b>Institute Name</b>	RV-VLSI Design Center
<b>Project Description</b>	Design Schematic and Layout for Standard cells library:1) Combinational : Half Adder: HADDX2 , Mux:MUX21X2, AOI : AOI221X2(Schematic entry, layout, DRC, LVS check) 2) Sequential : DFFX1, DFFX2 (Schematic entry, layout, DRC, LVS check)
<b>Tools Used</b>	ICstudio from Mentor Graphics-1) Pyxis (Schematic and Layout editor).2) Calibre (DRC, LVS, PEX check).
<b>Challenges</b>	1) Completing the layout within the PR-Boundary maintaining all DRC rules. 2) Placing metal pins on grid maintaining proper distance among them.3) Reducing the parasitics by avoiding poly routing.4) Identifying the missing ports and missing instances

<b>Project Title</b>	"DRC and LVS Test Cases and Design of Analog Layout Using 180nm Technology Node"
<b>Institute Name</b>	RV-VLSI Design Center
<b>Project Description</b>	Floor planning and layout design of 2stage operational amplifier using 180nm technology using device matching techniques, Worked on 180nm DRC and LVS test cases, From a given layout, finding out the DRC and LVS errors and rectifying them.
<b>Tools Used</b>	ICstudio from Mentor Graphics-1) Pyxis (Schematic and Layout editor)2) Calibre (DRC, LVS, PEX check)
<b>Challenges</b>	1) Making an optimized floor plan. 2) Transistors matching with the help of common centroid and inter-digitized technique.3) Making effective use of dummy transistors.4) Recognizing the sensitive transistors and protecting them.

<b>Project Name</b>	“Implementation of fuzzy control system for ankle joint movements”
<b>Institute Name</b>	Manipal Institute of Technology, Manipal
<b>Project Description</b>	The sensor unit detects the gait phase during walking & the controller controls dorsiflexion & plantar flexion based on the output signals from sensors
<b>Challenges</b>	Getting correct signal of dorsiflexion & plantar flexion while walking Understanding of LabView Software and NI-DAQ system
<b>Tools</b>	LabView (Software), NI-DAQ, Gyro Sensor