Profile Information
RV-VLSI ID: 1ADADB252928

Career Objective

- To be an integral part of a respected organization where I can exploit myself in the field of VLSI and to keep myself updated with emerging technology

Core Competancy

- Good understanding of ASIC and FPGA design flow.
- Very good knowledge of writing RTL models in Verilog.
- Strong background in Digital Logic Design and System Verilog .
- Developing self-checking testbench architecture using System Verilog and UVM.
- Writing Constraint Random and Directed test.
- Possess skill to understand existing UVM environment.
- Good knowledge of test plan and verification methodologies.
- Good knowledge of OOPS concepts and basic C programming.
- Familiar with PERL Scripting language.
- Familiar with Synthesis and Static Timing Analysis concepts.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-
Master Degree	Microelectronics and Control systems	PES Institute of Technology	2014	72.24
Degree	Electrical and Electronics	KLE Institute of Technology	2012	70.00
PUC	-	P.C Jabin college	2008	70.00
SSLC	-	St. Anotny's Public School	2006	76.64

Project Details

Project Title	RTL design of FIFO using verilog
Institue Name	RV-VLSI
Project Description	To design the write, read and reset functionality of FIFO.
Tools Used	Questa Sim
Challenges	To update read and write pointer and to develop code for almost full and almost empty test case.

Project Title	RTL Verification of RAM using System Verilog for high functional and code coverage.
Institue Name	RV-VLSI

Project Description	RTL design of a RAM was verified according to the specifications. Different Test cases were verified inorder to achieve high functional and code coverage.
Tools Used	Mentor Graphics Questa sim
Challenges	understanding architecture of RAM in System Verilog. writing covergroups for better functional coverage. Running regression and data integrity of driver and monitor.

Project Title	RTL Verification of UART protocol using System Verilog for high functional and code coverage.
Institue Name	RV-VLSI
Project Description	RTL design of a Universal Asynchronous Receiver Transmitter protocol was verified according to the specifications. Different Test cases were verified inorder to achieve high functional and code coverage.
Tools Used	Mentor graphics Questa sim with UVM library
Challenges	To increase code coverage. To understand the waveform and synchronization of the testbench components accordingly in the transcript of the RTL compiler.

Project Title	RTL Verification of RAM using UVM for high functional and code coverage.
Institue Name	RV-VLSI
Project Description	RTL design of a RAM was verified according to the specifications. Different Test cases were verified inorder to achieve high functional and code coverage.
Tools Used	Mentor graphics Questa sim
Challenges	To understand UVM based architecture and to configure the testbench. To write different testcases in order to achieve high functional and code coverage.

Project Title	RTL Verification of UART protocol using UVM for high functional and code coverage.
Institue Name	RV-VLSI
Project Description	RTL design of a Universal Asynchronous Receiver Transmitter protocol was verified according to the specifications. Different Test cases were verified inorder to achieve high functional and code coverage.
Tools Used	Mentor Graphics Questa sim with UVM library files.
Challenges	To understand sequence library and running multiple sequences in regression without the use of sequence library.

Project Name	Intelligent Irrigation system
Institute Name	KLE Institute of Technology
Project Description	The project is designed with a concern to save electricity, water and labour.
Challenges	Interface between microcontroller board and GSM module
Tools	KEIL

Project Name	Stochastic Noise Coefficient estimation of MEMS based Tri-Axial Angular Rate Sensor.
Institute Name	PES Institute of Technology

Project Description	The Aim of the project is to calculate the stochastic errors which constitute high random noises present in the tri-axial Angular rate Sensor. Modelling of these noises are done using Allan Variance, Power Spectral Density, Expectation Maximization
Challenges	Collecting the data at Zero rate condition.
Tools	Matlab, ADIS16405(gyroscope), ADISUSBZ(Evaluation board)