Profile Information

RV-VLSI ID: 1ADADB252908

Career Objective

- Seeking a Challenging position as a Physical Design Engineer that utilizes my proficiency of EDA tools.

Core Competancy

- Good Knowledge of ASIC flow and the stages involved in physical design flow.
- Have excellent knowledge and experience working with floorplan,placement,clock tree synthesis,routing and optimization.
- Good Knowledge in understanding and resolving timing violations(hold and setup) of various timing paths (STA).
- Good working knowledge of Linux, and Scripting using Perl and Tcl for automation.
- Understanding of Reliability issues like EM, Cross-talk, and Antenna effect.
- Ability to debug DRC and LVS errors (PG shorts,opens and soft checks) at block level.
- Good experience in sign-off closure-Timing with signal integrity,OCV AOCV and,MCMM,Power and Physical verification.
- Exposure to industry standard EDA tools like IC Compiler, Prime Time and Hercules from Synopsys.
- Good knowledge of CMOS concepts and Circuit theory.
- Good Knowledge of Digital Design concepts

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-
Degree	Electrical and Electronics	SRI CHANDRASEKHARENDRA SARASWATHI VISWA MAHA VIDYALAYA	2013	7.31
PUC	-	N.V.R JUNIOR COLLEGE	2009	86
SSLC	-	SASI E/M HIGH SCHOOL	2007	83

Project Details

Project Title	Torpedo Block
Institue Name	RV-VLSI Design Center
Project Description	Physical Design and Implementation of block level design consisting of 32macros,43K standard cells and operate on 400 MHz incorporated with 5Clocks,with a supply voltage of 1.8V with 5% max IR drop and power budget of300mW implemented with 6 layer
Tools Used	ICCompiler, Prime Time, Hercules from Synopsys, Calibre from Mentor Graphics.

Challenges	Placement of macros with restricted orientations and to avoid stacking ofmacros, have done multiple iterations to come up with an efficient floor plan.Encountered a lot of congestion between and on the macros and on thestandard cells..

Project Title	Static Timing Analysis
Institue Name	RV-VLSI Design Center
Project Description	STA for Register and latch based design with different constraints such asvariation in skew,uncertainity,input and output delays and also with timingexceptions. Generate setup and hold reports to solve/analyze cause for timingpath violations.
Tools Used	Primetime from Synopsys
Challenges	Identifying and Resolving the cause for Setup and Hold violations such asInput transition,Load Capacitance,Insertion delay,Cell delay was challenging.

Project Title	Analysing, Writing and debugging TCL Scripts
Institue Name	RV-VLSI Design Center
Project Description	Written scripts to extract data from the ICC DB.Analyzed the TCL scripts for the templates of floor plan,power plan,placement,CTS,Routing,and customizing them to our flow.Analyzed reports generated by the IC compiler.Challenges Learning TCL from scratch,Understanding each command in the script using man pages.Tools TCL tutor,Linux OS
Tools Used	Tclsh, TCL tutor, Linux OS
Challenges	Debugging TCL Scripts, writing TCL to design examples

Project Name	DETERMINATION OF POWER SYSTEM VOLTAGE STABILITY BY MODAL ANALYSIS
Institute Name	SRI CHANDRASEKHARENDRA SARASWATHI VISWA MAHA VIDYALAYA
Project Description	APC-based â€œpower factoryâ€ software prototype application was developed to assist power system the assessments and analysis or the voltage instability or the power network. In IEEE 14 bus system the modal analysis is to prove the accurate estimate or the system proximity to the voltage stability and correctly predict the critical buses and calculated amount of reactive power required to make the system stable. The power system has severe consequences including a voltage instability & low vo
Challenges	By devellping the powerfactory software prototype by performing modal analysis the accurate eastimation of system proximity in voltage instability.the eigen values had been after connecting the fact devices(TSC) and thus weak bus had determined.
Tools	powerfactory