Profile Information
RV-VLSI ID: 1ADADB252916

Career Objective

- Seeking a Challenging position as a Engineer that utilizes my proficiency of EDA tools.

Core Competancy

- Good Knowledge of ASIC flow and the stages involved in physical design flow and full custom flow.
- Have excellent knowledge and experience working with floorplan,placement,clock tree synthesis,routing and optimization.
- Good Knowledge in understanding and resolving timing violations(hold and setup) of various timing paths under OCV&MCMM.
- Good working knowledge of Linux, and Scripting using Perl and Tcl for automation.
- Understanding of DFM Reliability issues like EM, Cross-talk, and Antenna effect.
- Ability to debug DRC and LVS errors (PG shorts,opens and soft checks) at block level.
- Exposure to industry standard EDA tools like IC Compiler, Prime Time and Hercules from Synopsys.
- Ability to design a layout with good floor plan,optimized area,reducing parasitics and knowlegde of SRAM memory.
- Understanding of Device matching Techniques for analog circuits like interdigitization,dispersion,centroid matching.
- Good knowledge of IC fabrication process, CMOS concepts and Circuit theory,Digital Design concepts.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-
Master Degree	Industrial Electronics	KLSVDRIT Haliyal	2014	76.3
Degree	Electronics and Communication	JSS Academy of Technical Education Bengaluru	2012	73.67
PUC	-	Bangur Nagar Composite Pre-University College	2008	80.16
SSLC	-	St.Michael's Convent High School	2006	78.72

Project Details

Project Title	Process Documents Overview
Institue Name	RV-VLSI DESIGN CENTRE
Project Description	Review of various process documents-Data flow Diagram,Technology files, .lib files,DRC and LVS rules files, Antenna rules file and Spice models.

Project Title	Scripting
Institue Name	RV-VLSI DESIGN CENTRE
Tools Used	Tcl,PERL
Challenges	To write PERL script to calculate total resistance and capacitance for a particular net from PEX file.Extraction of timing information from timing reports,such as violating paths,number of paths in report,start point,end point and slack.

Project Title	Static Timing Analysis
Institue Name	RV-VLSI DESIGN CENTRE
Project Description	STA for Register and latch based design with different constraints such as variation in skew,uncertainity,input and output delays and also with timing exceptions. Generate setup and hold reports to solve/analyze cause for timing path violations.
Tools Used	Primetime from Synopsys
Challenges	Identifying and Resolving the cause for Setup and Hold violations such as Input transition,Load Capacitance,Insertion delay,Cell delay was challenging.

Project Title	Torpedo Block
Institue Name	RV -VLSI DESIGN CENTRE
Project Description	Physical Design and Implementation of block level design consisting of 32 macros,43K standard cells and operate on 400 MHz incorporated with 5 Clocks,with a supply voltage of 1.8V with 5% max IR drop and power budget of 300mW implemented with 6 layers of metal.
Tools Used	IC Compiler,Prime Time and Calibre
Challenges	Placement of macros with restricted orientations and to avoid stacking of macros, have done multiple iterations to come up with an efficient floor plan. Encountered a lot of congestion between and on the macros and on the standard cells.

Project Title	Physical Verification(DRC and LVS) of D-Flip flop in 180nm technology
Institue Name	RV-VLSIDESIGN CENTRE
Tools Used	ICStudio from Mentor Graphics: Pyxis - Schematic and Layout Editor ,Calibre - DRC and LVS Checks
Challenges	Fixing discrepancies like shorts and open was challenging . Fixing nets and instance errors was challenging

Project Title	90nm Standard Cell Library Design(9tracks)
Institue Name	RV-VLSIDESIGN CENTRE
Tools Used	ICStudio from Mentor Graphics: Pyxis - Schematic and Layout Editor ,Calibre - DRC and LVS Checks
Challenges	Placing Poly and Contact on grid was challenging .Routing by using only M1 layer was difficult for complex circuits.Fixing Bad device extraction error was challenging

Project Name	Asynchronous ADC Based on Level Crossing Technique

Institute Name	JSS Academy of Technical Education Bengaluru
Project Description	The main objective is to convert the analog signal into digital domain based on irregular sampling of the signal and asynchronous design.
Challenges	Design of current mirror circuits for current steering DAC,Two stage OpAmp Design,Comparator Design and development of Successive Approximation Register(SAR) Algorithm.
Tools	Cadence/Virtuso,LT Spice