Profile Information
RV-VLSI ID: 1ADADB263522

Career Objective

- Seeking a position as a full-custom layout design engineer, in an environment that offers to showcase acquired skills so as to have a continued growth

Core Competancy

- Good exposure to the full custom flow. Worked on 180nm, 90nm and 28nm respectively.
- Good knowledge of ASIC design flow and stages involved in Full Custom.
- Skilled in Layout optimization techniques.
- Good in debugging skills in DRC and LVS errors such as net errors,property errors,bad devices.
- Capable of designing high performance analog layouts.
- Understanding of reliability issues as Antenna effects, crosstalk and via doubling.
- Good understanding of MOS device physics and IC fabrication process.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-
Master Degree	VLSI & ES	T John Institute Of Technology, Bangalore	2014	80
Degree	Telecommunications	PES Institute Of Technology, Bangalore	2012	62.5
PUC	-	Royal Composite PU College,Chintamani	2007	74
SSLC	-	Sri Raghavendra Educational Trust, Chintamani	2005	76

Project Details

Project Title	Design and physical verification of 9 track standard cells in 90nm CMOS technology
Institue Name	RV- VLSI Design Center
Project Description	Standard cell library is a collection of combinational and sequential cells which is required for any type of higher level design. Designed standard cells with height constraint of 2.88 um with different drive strengths.
Tools Used	IC station from Mentor Graphics- 1.Pyxys(schematic and layout editors) 2.Calibre (DRC,LVS and PEX check)

Project Title	Physical verification of D Flip flop in 90nm CMOS technology

Institue Name	RV- VLSI Design Center
Project Description	To read the foundry document and clear associated DRC and LVS errors.
Tools Used	IC station from Mentor Graphics- 1.Pyxys(schematic and layout editors) 2.Calibre (DRC,LVS and PEX check)

Project Title	Foundry Document Overview.
Institue Name	RV- VLSI Design Center

Project Title	Layout design and physical verification of Two stage diffrential Op-Amp in 180nm CMOS technology
Institue Name	RV- VLSI Design Center
Tools Used	IC station from Mentor Graphics- 1.Pyxys(schematic and layout editors) 2.Calibre (DRC,LVS and PEX check)

Project Name	Zigbee Based On Drip Irrigation System
Institute Name	PES Institute Of Technology, Bangalore
Project Description	To develop and to test an automation system having a low cost equipment and feedback type controller for site-specific management of irrigation system
Challenges	To understand the complete working of Drip Irrigation System. Zigbee Wireless Sensor Networks. Programming with Embedded C.
Tools	Zigbee, Wireless Sensor Networks Embedded C.

Project Name	Large Data Acquisition And Synchronization using NTP
Institute Name	T John Institute Of Technology, Bangalore
Project Description	1) Development of VIâ€™s for AIT-429,NI-8431/16 ports,NI-6511 and NI-6363. 2) Involved in Test case, Test Script development. 3) HSI testing with respect to the high-level requirements in compliance
Challenges	
Tools	Labview