Profile Information
RV-VLSI ID: 1ADADB252909

Career Objective

- To prove myself dedicated, worth and energetic as a team engineer in a progressive organization that gives me scope to apply my knowledge and skills.

Core Competancy

- Good understanding of fundamentals of Transistors and CMOS device operation.
- Good exposure to technology by undergoing additional training in VLSI.
- Good knowledge on Device matching techniques and optimization techniques.
- Worked on 180nm, 90nm and 28nm technology nodes.
- Ability to interpret different kind of LVS errors such as stamping conflict,incorrect nets, shorts ,opens & fixing them.
- Good understanding of Electromigration, Electrostatic Discharge (ESD), latch up and signal integrity issues.
- Good understanding of DFM rules such as antenna effects, metal density, EOL and via doubling.
- Good understanding of layout proximity effects such as WPE and LOD.
- Hands on experience in Xilinx ISE, Tanner EDA tool suite, Mentor Graphics IC studio.
- Good knowledge of STA and Physical Design flow.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-
Master Degree	VLSI	MVGR College of Engg.	2013	71.20
Degree	Electronics and Communication	St Theresa institute of engg. and technology	2007	58.2
PUC	-	M.S.N Junior college	2003	76.5
SSLC	-	Pragathi Residential High School	2001	60.33

Project Details

Project Title	Layout design and Physical verification of Standard cells in 90nm CMOS technology (9-Tracks)
Institue Name	RV -VLSI Design Centre
Project Description	Standard cell library is a collection of combinational and sequential cells which is required for any type of higher level design.
Tools Used	ICstudio (Mentor Graphics), Calibre (DRC, LVS, XRC)

Challenges	1. Placing the complete layout within the given PR-Boundary. 2. Making the layout as small as possible by Source & Drain sharing. 3. Routing with only Metal1 especially in sequential cells was quite challenging . 4. Reducing parasitics.

Project Title	Physical verification of D flip flop in 180nm technology
Institue Name	RV -VLSI Design Centre
Project Description	To read the foundry document and clear associated DRC/LVS errors.
Tools Used	ICstudio (Mentor Graphics), Calibre (DRC, LVS, XRC)
Challenges	1.Understanding of Netlist. 2.To clear different types of DRC/LVS errors. 3.Understanding of transistor folding techniques.

Project Title	Analog Op-Amp Layout(90nm)
Institue Name	RV -VLSI Design Centre
Project Description	In this project we designed layout of op-amp using device matching techniques such as common centroid,symmetry etc.
Tools Used	ICstudio (Mentor Graphics), Calibre (nm DRC , nm LVS).
Challenges	1.Effective floor plan with matching techniques like common centroid, inter-digitization and dispersion. 2.Keeping width of transistor same to maintain symmetry.

Project Title	Design and physical verification of SRAM leaf cells layout in 28nm CMOS technology
Institue Name	RV -VLSI Design Centre
Project Description	the layout design of different blocks of SRAM using source - Drain sharing technique . The different blocks include the leaf -cells ,precharge ,sense amplifier, Din,Dout,Control block .
Tools Used	ICstudio (Mentor Graphics), Calibre (DRC, LVS, XRC).
Challenges	1.Efficient routing while maintaining metal density. 2.Multiple floor plan to arrive at optimized area utilization. 3.Clearing LVS errors such as stamping conflicts,opens and shorts,property errors. 4.Proper pin placement to abut with other blocks.

Project Name	Hydro Graphic Survey using DGPS.
Institute Name	St Theresa institute of engg. and technology
Project Description	The limitations of GPS can be reduced by using DGPS to get more accurate results advanced systems such as WAAS can be used.
Challenges	Deciding signal frequency,Area etc
Tools	Zigbee model.

Project Name	Leakage power reduction in cmos circuits using leakage controlled pmos techinqe in nano scale.
Institute Name	MVGR College of Engg.

Project Description	We propose a technique called LCPMOS for designing CMOS gates which significantly cuts down the leakage current without increasing the dynamic power dissipation.
Challenges	1.Reducing area and power for LPCMOS Technique compared to CMOS tecnologies. 2.Reduction of leakage current.
Tools	Tanner EDA tools