Profile Information

Name: HemaSaranya Sanagavarapu
Email: hemasaranya573@gmail.com
Phone: 9686753322
Address: #28/A, 5th main , 18th cross
NS Palya
Bangalore
Karnataka-560076

Career Objective

- To achieve excellence in working as a Layout engineer where my challenging quests are used to maximize the growth of the organization.

Core Competancy

- Theoretical knowledge on CMOS Fabrication Process.
- Understanding of Layout versus Schematic errors such as Short , Open and soft check.
- Knowledge on CMOS concepts.
- Theoretical understanding on Design for manufacturability concepts like End of line , LOD, Via Doubling ,Metal Density.
- Understanding the importance and knowledge on Device matching techniques.
- Basic knowledge on Static Timing Analysis.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design - Full Custom	RV-VLSI Design Center	2015	-
Degree	Electronics and Communication	Kotthamasu sambasivarao and Saraswathamma Women's Engineering College	2012	73.39
PUC	-	Sri Chaitanya Jr.College	2008	84.50
SSLC	-	Haritha Bala Kuteer	2006	72.66

Project Details

Project Title	VERIFICATION AND CORRECTION OF LVS ERROS IN GIVEN DFF LAYOUT
Institue Name	RV-VLSI DESIGN CENTRE
Project Description	Understanding the LVS errors of the given DFF layout which was done in 180nm technology and correcting them according to the schematic given.
Tools Used	PYXIS Layout editor CALIBER Verification Tool
Challenges	Understanding the errors in the given layout. Fixing the LVS errors.

Project Title	GEOMETRY EDITING OF STANDARD CELLS IN 90NM TECHNOLOGY
Institue Name	RV-VLSI DESIGN CENTRE

Project Description	Designing of schematics from given spice net list. Designing layouts by looking at the schematic. Running DRC, LVS and compatibility checks and fixing the errors.
Tools Used	PYXIS Layout Editor for layout design. CALIBER Verification tool
Challenges	Drawing the 9 track Place and Route Boundary. Placing of the Metal1 Pin according to the given compatibility rule Routing using metals according to the given DRC file.

Project Title	DESIGN OF OPAMP FLOORPLAN AND LAYOUT USING DEVICE MATCHING TECHNIQUES IN 180NM TECHNOLOGY
Institue Name	RV-VLSI DESIGN CENTRE
Project Description	Designing floor plan for Operational Amplifier by using device matching techniques and designing a layout of OpAmp which should be LVS and DRC clean.
Tools Used	PXYIS LAYOUT for geometry editing. CALIBER for verification
Challenges	Designing the floor plan using device matching techniques. Routing using metal layers.

Project Title	MEMORY LAYOUT DESIGN OF SRAM
Institue Name	RV-VLSI DESIGN CENTRE
Project Description	Layout design for Static Read Only Memory blocks and leaf cells which should be DRC,LVS and compatability clean.
Tools Used	PYXIS FOR LAYOUT DESIGN CALIBER FOR VERIFICATION
Challenges	Design of basic gates as there were many DRC rules. Placing of polygon and contact on the grid.

Project Name	Radio Frequency Identification (RFID) system BASED ATTENDANCE SYSTEM
Institute Name	Kotthamasu sambasivarao and Saraswathamma Women's Engineering College
Project Description	RF-ID system uses radio waves to retrieve attendance from a device called a tag or transponder produces the attendance reports in required format.
Challenges	Study of PHILLIPS 8051 micro Controller and understanding its register programming model. Understanding of LCD Display, NV memory, RS 232 Serial Communicator. Storing the reports into a PC through RS-232 serial port.
Tools	PHILLIPS 8051 micro controller, LCD Display unit, NV memory, RS-232 Serial Communicator, and associated circuitry. KEIL Compiler Software.