

## Profile Information

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## Career Objective

- To face new challenges in the field of physical design engineering which will truly test my skills and help myself and the organization to flourish.

## Core Competancy

- Good software and scripting skills Perl, Tcl to enhance design automation and flow and physical synthesis improvements.
- Good hands-on experience with Floor planning, power planning, placement, timing optimization.
- Good understanding of static timing analysis (STA), EM/IR and sign-off flows
- Good knowledge of Verilog RTL coding and Digital Design Concepts
- Good working knowledge of Linux, and C programming
- Good knowledge about ASIC Design flow.
- Good understanding of fundamentals of Transistors and circuit theory
- Basic knowledge of power reduction techniques.
- Hands on experience on physical verification DRC and LVS using Hercules
- Good knowledge of design and verification of Memory elements.

Education Details				
Degree	Discipline	School/College	Year of passing	Aggregate
PG Diploma	ASIC Physical Design (PD) for Deep Submicron process nodes	RV-VLSI Design Center	2015	-
Master Degree	VLSI DESIGN	VIT University	2015	8.9
Degree	Electronics and Communication	Gogte Institute of Technology	2012	76.7
PUC	-	SHIVANAND COLLEGE, KAGWAD	2008	80.33
SSLC	-	JAWAHAR NAVODAYA VIDYALAYA, BELGAUM	2006	67.3

## Project Details

<b>Project Title</b>	Block level physical design of torpedo subsystem
<b>Institute Name</b>	RV-VLSI DESIGN CENTRE

<b>Project Description</b>	Torpedo sub block includes 32 macros, 43275 standard cells ,it has total of 5 clocks (3 propagated and 2 generated), 6 metal layers are used, Fab: jazz semiconductor, 180 nm technology node is used.
<b>Tools Used</b>	ICC, Prime Time, Hercules from Synopsys, Calibre from Mentor Graphics
<b>Challenges</b>	Placement of macros during Floor plan, deciding number of power straps to get IR drop (VDD+VSS) less than 5% of 1.8 performing EM analysis, Timing driven placement , DFM Analysis , fixing Antenna Violations, Also analysing and writing TCL scripts.

<b>Project Title</b>	Synthesis and performing Static Timing Analysis
<b>Institute Name</b>	RV-VLSI DESIGN CENTRE
<b>Project Description</b>	Synthesis of many designs and performing STA and analyzing timing reports for all kinds of timing paths. Writing SDC's to create/generate clocks, to declare false paths, multi cycle paths, constraining various timing paths.
<b>Tools Used</b>	Design Compiler and Prime Time from Synopsys.
<b>Challenges</b>	Fixing of Setup and Hold violations .Determination of false paths in the design, understanding of delays caused by various cells and nets, considering OCV and removal of common path reconvergence pessimism.

<b>Project Title</b>	ASIC IMPLEMENTATION OF HIGH THROUGHPUT PID CONTROLLER
<b>Institute Name</b>	VIT UNIVERSITY
<b>Project Description</b>	The PID (proportional+integral+digital) controller is one the heavy system where lots of power is dissipated. In order to reduce the power consumed and enhance the speed Hand-Carlson adder and a 8-level pipelined form of multiplier have been used.
<b>Tools Used</b>	NCsim, RC Compiler, Encounter SOC, Modelsim.

<b>Project Title</b>	SYNCHRONOUS FIFO: RTL Design and Verification.
<b>Institute Name</b>	VIT UNIVERSITY
<b>Project Description</b>	Synchronous FIFO acts as buffer interface bridge in most of the device which are interfaced.
<b>Tools Used</b>	Cadence-NCsim, Cadence Code-coverage.

<b>Project Name</b>	LOW COMPLEXITY HARDWARE SHARING ARCHITECTURE OF DEBLOCKING FILTER FOR VP8 AND H.264 VIDEO STANDARDS.
<b>Institute Name</b>	Gogte Institute of Technology
<b>Project Description</b>	Reduce the complexity of Deblocking Filter we have derived architecture shared between H.264 and VP8 .
<b>Challenges</b>	Study H.264 and VP8 video compression standard.Implementation in Matlab and check the picture signal to noise ratio (PSNR). Implemented RTL in Verilog and checked the gate count and quality of image
<b>Tools</b>	Matlab, quartus II, Modelsim

<b>Project Name</b>	MULTI-STAGE NOISE SHAPING ARCHITECTURE USING A SIGMA-DELTA ADC
<b>Institute Name</b>	VIT University

<b>Project Description</b>	The multistage noise shaping modulator which offer least noise is used for the design of sigma delta ADC
<b>Challenges</b>	Design of Two stage operational Amplifier, Summer, integrating-circuitry. Design of latched-comparator, 1-bit DAC. Assembling of all the above component to get Multi Stage Noise shaping Modulator Design of sigma delta ADC
<b>Tools</b>	Cadence Virtuoso