

Profile Information

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Career Objective

- To obtain a position within the company that will allow me to utilize my skills and knowledge in Physical design for the benefit of the company

Core Competancy

- Good understanding of fundamentals of CMOS Transistors and circuit theory understanding of fundamentals of CMOS Transist
- Basic knowledge of ASCII flow (RTL to GDSII) understanding of fundamentals of CMOS Transistors and circuit theory
- Good knowledge of Digital Design Concepts. understanding of fundamentals of CMOS Transistors and circuit theory
- Good exposure to technology by undergoing additional training in VLSI.
- Efficient in placement of high count macros during floor planning.
- Good understanding of fundamentals of CMOS Transistors and circuit theory
- Basic knowledge of ASCII flow (RTL to GDSII)
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- Efficient in placement of high count macros during floor planning.

Education Details				
Degree	Discipline	School/College	Year of passing	Aggregate
PG Diploma	Advanced Diploma in ASIC Design - RTL Verification	kiran	2015	-
Degree	Electrical and Electronics	B.L.D.E.A College Of Engineering & Technology	2015	70.94
PUC	-	KCP science college Bijapur, Karnataka Karnataka Pre-University	2010	74.83
SSLC	-	Vivekananda high school sarwad, Bijapur, Karnataka Karnataka Secondary Education Examination	2008	89

Project Details

Project Title	Block level physical design of torpedo subsystem
Institute Name	RV-VLSI Design Centre

Tools Used	IC Compiler from Synopsys (for physical implementation), Prime Time from Synopsys (for STA), Hercules from Synopsys (for DRC)
Challenges	Placement of macros with restricted orientations and to avoid stacking of macros, have done multiple iterations to come up with an efficient floorplan. Deciding number of power straps to get IR drop (VDD+VSS) less than 5% of 1.8V

Project Name	BE Project Name
Institute Name	B.L.D.E.A College Of Engineering & Technology
Project Description	BE PProject desc
Challenges	asdf asdf asdf sadf
Tools	asdfasdf