

Profile Information

Name: BIJESH AK Email: akbijesh@gmail.com

Phone: 9538130954 Address: Alokkoottathil Ho Perambra PO Kozhikode DT

Perambra

Karnataka-673525

Career Objective

Looking for an opportunity to work as a physical design engineer. The core skills acquired and experience in semiconductor industry will append moment

Core Competancy

- Good understanding in VLSI Design flows.
- Good understanding of fundamentals of Transistors and circuit theory
- Good knowledge of Digital design Concepts
- Understanding in STA and analyzing timing reports.
- Hands on experience in APR flow with Synopsys IC compiler

Education Details					
Degree	Discipline	School/College	Year of passing	Aggregate	
PG Diploma	Diploma in RTL Design and Verification (VLSI Front End)	RV-VLSI Design Center	2015	-	
Master Degree	Microelectronics & VLSI Design	NIT Calicut NATIONAL INSTITUTE OF TECHNOLOGY	2014	7.97	
Degree	Electronics and Communication	MEA Engineering College	2006	62.6	
PUC	-	PHSS Perambra Kerala State	2002	78.6	
SSLC	-	PHSS Perambra Kerala State	2000	91.6	

Project Details

Project Title	Physical design of a block level subsystem in 180 nm technology
Institue Name	RV-VLSI Design Centre
Tools Used	Synopsys Primetime, Synopsys IC Compiler
Challenges	nitial challenge was to derive the effective floor plan and power plan. Understanding of the design and data flow of the design helped to get a good start point for the floor-plan. Through the iterative process, arranging macros by considering

Project Title	Static Timing Analysis
Institue Name	RV-VLSI Design center
Tools Used	Synopsys DesignCompiler, PrimeTime