Profile Information
RV-VLSI ID: 1ADADB252911

Career Objective

- Looking for an opportunity to work as a Physical Design Engineer in a dynamic work environment.

Core Competancy

- Basic understanding of MOS Transistors fundamentals
- Good knowledge of Digital Design Concepts
- Basic knowledge of Verilog HDL coding
- Well versed with GLN to GDS-II flow
- Good at Analysis of Timing Reports
- Good exposure to technology by undergoing additional training in Physical Design with Hands on Project
- Good at handling various Tcl scripts for Design
- Good working knowledge of Linux Operating System

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-
Master Degree	VLSI	Arjun College Of Technology and Sciences	2015	72.40
Degree	Electronics and Communication	Jawaharal Nehru Institute Of Technology	2013	79.88
PUC	-	TSR National Junior College	2009	90.7
SSLC	-	N P Subba Reddy Central School	2007	84.83

Project Details

Project Title	Automatic Place and Route of a SoC Block
Institue Name	RV-VLSI Design Center
Project Description	Torpedo sub-block includes 32 macros, 43243 standard cells with supply voltage of 1.8V, working at an operating frequency of 400MHz, it has total of 5 clocks 3 propagated and 2 generated, Design uses 5 metal layers.Fab: Jazz Semiconductor
Tools Used	ICCompiler, PrimeTime, Hercules from Synopsys and Calibre from Mentor Graphics
Challenges	Placement of Macros with congestion free Floor Planning. Deciding number of power straps to get IR drop (VDD+VSS) less than 5% of 1.8V. Identifying useful skew and fixing the violations

Project Title	Timing Analysis with OCV
Institue Name	RV-VLSI Design Center
Project Description	Timing reports has been generated for different designs for MCMM and analysed the same. Analysed CRPR effect in timing repports. Understanding the techniques of fixing violations
Tools Used	PrimeTime from Synopsys
Challenges	Understanding signal integrity and cross-talk effects, Timing analysis of latch based designs, effects of clock skew on timing

Project Title	Analysing, Writing and Debugging Tcl Scripts
Institue Name	RV-VLSI Design Center
Project Description	Writing various Tcl scripts to extract information from ICC database, understanding Tcl scripts generated by ICCompiler , writing Tcl scripts to various examples
Tools Used	Tclsh, TCL tutor, ICCompiler
Challenges	Debugging Tcl scripts, writing Tcl to design examples

Project Name	Vehicle Detection And Identification By Using RFID
Institute Name	Jawaharal Nehru Institute Of Technology
Project Description	We developed a hardware circuitry which is capable of detecting the unauthorized vehicles by using Radio Frequency Identification methodology.
Challenges	Interfacing an LCD with Micro-Controller, Getting the samples from RFID as inputs to the Micro-Controller
Tools	Keil uVision, 8051 Micro-Controller, Flash Magic