Profile Information

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Career Objective

- Seeking a challenging position as a Full Custom Layout Design Engineer where i can deliver high performance Layouts

Core Competancy

- Good exposure to full custom flow and worked on 180nm, 90nm and 28nm technology nodes.
- Skilled in Layout optimization techniques and layout parasitic reduction.
- Ability to design high performance analog layouts.
- Good understanding of Device matching Techniques like interdigitation and common centroid technique.
- Proficiency in Memory Leaf cells layout design.
- Very Good debugging skills in physical verification checks like DRC, DFM and LVS including Shorts, Opens, stamping.
- Basic understanding of DFM rules such as antenna, metal density and via doubling.
- Good understanding of Latch up, Electro migration, ESD , WPE , LOD concepts.
- Good understanding of MOS device physics.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-
Degree	Electronics and Communication	Atria Institute Of Technology	2014	67.33%
PUC	-	JSS Comp PU college	2010	84.83%
SSLC	-	Govt. Pre University College	2008	82.08%

Project Details

Project Title	Foundry Document Overview.
Institue Name	RV-VLSI Design Center , Bangalore
Project Description	Review of the process documents which contains description of the process, layer purposes and description of layout design rules.

Project Title	Physical verification of D-flip flop layout in 180 nm CMOS technology.
Institue Name	RV-VLSI Design Center , Bangalore

Project Description	Fixing DRC and LVS errors of given D Flip-Flop layout in 180nm CMOS technology.
Tools Used	Mentor Graphics IC Studio (Pyxis)-Layout viewer and editor, Calibre-DRC and LVS verification tool.
Challenges	Finding shorts and opens was a challenge. By comparing layout netlist with the schematic netlist , finding missing connection was tricky.

Project Title	90nm Standard Cell Library Design.
Institue Name	RV-VLSI Design Center , Bangalore
Project Description	The layout height of the standard cells were fixed to 2.88um and the pitch is 0.32um.The layout of all the cells are done in 9-track and its physical verfication is performed.Layout of standard cells of different driving strengths are designed.
Tools Used	Mentor Graphics IC Studio (Pyxis)-Layout viewer and editor, Calibre-DRC and LVS verification tool.
Challenges	Fitting the Standard cells layout in specified area constraints and solving the related LVS errors. Also, understanding the importance of usage of Standard Cells.Using source-drain sharing technique to reduce area of the cell was a challenge.

Project Title	Analog Layout design of 2 Stage OP-AMP in 90nm.
Institue Name	RV-VLSI Design Center , Bangalore
Project Description	Designing layout of op amp with different floor plans with device matching techniques such as common centroid and interdigitation. Implementing the best one.
Tools Used	Mentor Graphics IC Studio (Pyxis)-Layout viewer and editor, Calibre-DRC and LVS verification tool.
Challenges	In common centroid technique meeting all the rules such as symmetry, dispersion, compactness and coincidence was a challenge. Designing the best interdigitated matching was challenging.

Project Title	Design and physical verification of SRAM leafcells layout in 28 nm CMOS technology.
Institue Name	RV-VLSI Design Center , Bangalore
Project Description	The inputs of the SRAM Memory Compiler has to be designed in this project which includes the leaf cell blocks like Precharge and mux block, sense amplifier , Dout, Din, Scan block, Control block, decoders.
Tools Used	Mentor Graphics IC Studio (Pyxis)-Layout viewer and editor, Calibre-DRC and LVS verification tool.
Challenges	Poly-silicon and contacts should be placed in fixed-pitch grids, so it was a challenge to satisfy both area constraints and fixed-pitch grid.

Project Name	Automatic Insertion of Dummy Metal, to meet the Metal Density Requirements for 28nm process (RV-VLSI Design Center, Bangalore – 2014).
Institute Name	Atria Institute Of Technology

Project Description	The code was written by Understanding Calibre SVRF manual for satisfying Metal density criteria and pattern generation technique in the rule deck, which is run on CalibrenmDRC to look for the violation of metal density in the layout. Density violation area is filled with Dummy metal fills.
Challenges	Understanding the Calibre SVRF manual to develop algorithm was a challenge. Developing an algorithm which will fill dummy metal efficiently was a challenge.
Tools	Mentor Graphics, ICstudio - PYXIS layout , Calibre nmDRC .