Profile Information
RV-VLSI ID: 1ADADB252907

Career Objective

- To be an efficient layout design engineer and to enhance my professional skills in a dynamic and stable workplace.

Core Competancy

- Exposure to 180nm ,90nm and 28nm CMOS technologies for layout designing.
- Ability to clear LVS and DRC efficiently,knowledge about good layout techniques such as transistor folding,well sharing.
- Skill to design area optimized layout with less parasitic.
- Good knowledge about analog layout techniques,device matching,centroid layout technique and DFM.
- Ability to fix LVS errors such as power ground opens and shorts,stamping.
- Good knowledge about basic Device physics, ESD , latchup,Antenna effects,Electromigration effects,well proximity effects
- Supports group decisions and puts group goals ahead of own goals.
- pays close attention to detail , accuracy and completeness.
- Expressing ideas effectively.organizing and delivering information appropriately. Listening actively.
- Adapts to effectively deal with change and diverse people.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-
Degree	Electrical and Electronics	Jawaharlal Nehru national college of engineering	2011	73.5
PUC	-	DVS composite college	2007	70.5
SSLC	-	DVS High School	2005	80.5

Project Details

Project Title	Design and physical verification of SRAM leafcells layout in 28 nm CMOS technology
Institue Name	RV-VLSI
Project Description	SRAM is a semiconductor memory which uses bi stable latching circuitry to store each bit. SRAM has many blocks such as decoders, mux , array,sense amplifier , precharge. All these blocks were floor planned and drawn in 28nm CMOS technology.
Tools Used	IC studio (Schematic and Layout Designing tool) from Mentor Graphics Calibre DRC-H tool from Mentor Graphics Calibre LVS-H tool from Mentor Graphics

Challenges	Floor planning the blocks of SRAM such as precharge , sense amp , etc.. and routing with minimum DRC of the same using limited number of metals was a challenge.clearing few LVS errors such as stamping conflicts,opens and shorts,property errors.

Project Title	Design and physical verification of 9 track standard cells using 90 nm CMOS technology
Institue Name	RV - VLSI
Project Description	Standard cell library is a collection of combinational and sequential cells which is required for any type of higher level design. In this project we designed some standard cells with optimized area technique.
Tools Used	IC Studio(Schematic and Layout viewers) by Mentor Graphics Calibre DRC-H by Mentor Graphics Calibre LVS-H by Mentor Graphics
Challenges	As the hieght of cell is fixed , designing area optimized layout, routing with only one metal in some cells, clearing few LVS errors.

Project Title	Physical verification of D-Flip Flop in 180 nm CMOS processing technology
Institue Name	RV -VLSI
Tools Used	Pyxis layout viewer Calibre DRC tool Calibre LVS tool
Challenges	Solving LVS errors like Unmatched nets and opens and shorts in power and ground connections were challenging.

Project Title	Design and physical verification of two stage Operational amplifier in 90 nm CMOS technology
Institue Name	RV-VLSI
Project Description	An operational amplifier is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. In this project we designed layout of OP AMP using 90 nm CMOS techmology & using device matching technique
Tools Used	Pyxis schematic and layout viewer Calibre DRC-H and LVS-H
Challenges	Floorplanning the device which satisfies almost all matching requirements and routing using only one metal in a minimum area was a challenge. solving stamping conflicts and opens and shorts in the layout.

Project Title	Review of foundry document
Institue Name	RV-VLSI

Project Name	Optimization of usage of energy renewable energy resources using operations research techniques
Institute Name	Jawaharlal Nehru national college of engineering
Project Description	Our project was based on the optimization of energy usages in rural areas using operations research tools and technique.
Challenges	Collecting the data that had to be used for the calculation and optimizing the energy usage and optimizing the available resources for that particular rural area was bit challenging as there are few resources are left to get the energy from.

Tools	Operations research was used for calculations purpose.