Profile Information
RV-VLSI ID: 1ADADB252914

Career Objective

- To become a key technical resource for an organisation, where I am able to explore my full potential, add to my learning curve, as well as contribute.

Core Competancy

- Good knowledge of ASIC design flow and stages involved in Full custom design flow.
- Exposure to 180nm, 90nm and 28nm technology nodes.
- Proficient in solving LVS errors such as net errors,stamping,opens,shorts,bad devices,property errors.
- Understanding of reliability issues as Antenna effects, Crosstalk, Electromigration and via doubling.
- Good understanding of Electrostatic Discharge (ESD), Latch up , Layout proximity effects such as WPE and LOD.
- Good knowledge on Device matching and Layout optimization techniques.
- Excellent knowledge on fundamentals of Transistors and CMOS device operation.
- Hands on experience in Xilinx ISE, Tanner EDA tool suite, Cadence Virtuoso, Mentor Graphics ICstudio.
- Good understanding of Static timing analysis and stages involved in Physical Design flow.
- Good knowledge of Digital Design concepts and IC fabrication process.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design	RV-VLSI Design Center	2015	-
Master Degree	VLSI & ES	BGSIT, B G Nagara	2013	71.6
Degree	Electronics and Communication	Adhichunchanagiri Institute of Technology (AIT), Chikmagalur	2011	63.4
PUC	-	Govt maharajas pu college, Mysore	2007	59.5
SSLC	-	Sri vidyaganapathi high school	2005	81.2

Project Details

Project Title	Design and physical verification of 9 track standard cells in 90nm CMOS technology
Institue Name	RV - VLSI Design Centre

Project Description	Standard cell library is a collection of combinational and sequential cells which is required for any type of higher level design. Designed standard cells with height constraint of 2.88 um with different drive strengths.
Tools Used	IC station from Mentor Graphics- 1.Pyxys(schematic and layout editors) 2.Calibre (DRC,LVS and PEX check)
Challenges	1. Placing the complete layout within the given PR-Boundary. 2. Making the layout as small as possible by Source & Drain sharing. 3. Routing with only Metal1 especially in sequential cells was quite challenging . 4. Reducing parasitics.

Project Title	Layout design and physical verification of Two stage diffrential Op-Amp in 90nm CMOS technology
Institue Name	RV - VLSI Design Centre
Project Description	An op-amp is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. In this project we designed layout of op-amp using device matching techniques such as common centroid,symmetry etc
Tools Used	IC station from Mentor Graphics- 1.Pyxys(schematic and layout editors) 2.Calibre (DRC,LVS and PEX check)
Challenges	1. Floor planning and dummy placement for Sensitive Transistor pair and double guarding for protection. 2. Effective Floor planning with common centroid, inter-digitize, dispersion. 3. Keeping width of finger transistor same for symmetry.

Project Title	Layout design and physical verification of SRAM leaf cell layout at 28nm CMOS technology.
Institue Name	RV - VLSI Design Centre
Project Description	SRAM is a semiconductor memory which uses bi stable latching circuitry to store each bit.The different blocks include the leaf-cells,pre-charge,sense amplifier,Din,Dout,Control block and Decoder block(Project in progress).
Tools Used	IC station from Mentor Graphics- 1.Pyxys(schematic and layout editors) 2.Calibre (DRC,LVS and PEX check)
Challenges	1.Efficient routing while maintaining metal density. 2.Multiple floor plan to arrive at optimized area utilization. 3.Clearing LVS errors such as stamping conflicts,opens and shorts,property errors. 4.Proper pin placement to abut with other blocks.

Project Title	Physical verification of D Flip flop in 180nm CMOS technology
Institue Name	RV - VLSI Design Centre
Project Description	To read the foundry document and clear associated DRC and LVS errors.
Tools Used	IC station from Mentor Graphics- 1.Pyxys(schematic and layout editors) 2.Calibre (DRC,LVS and PEX check)
Challenges	1.Adjusting to new technology node. 2.Understanding of well sharing and device mismatch. 3.Understanding of transistor folding techniques.

Project Name	Gesture based smart control for Home appliances.

Institute Name	Adhichunchanagiri Institute of Technology (AIT), Chikmagalur
Project Description	This project deals with operation of gesture sensors.Used mercury sensors formeasuring the tilting angle.Based on the angle particular action is taken
Challenges	Deciding type of sensor,Signal frequency.
Tools	IF receiver and Transmitter.

Project Name	Design and Implementation of Modified Adaptive Filtering Algorithm For Noise Cancellation in Speech signal on FPGA For minimum resource usage.
Institute Name	BGSIT, B G Nagara
Project Description	This project presents the applicability of a FPGA system for speech processing. Here adaptive filtering technique is used for noise cancellation in speech signal using Least Mean Squares (LMS) algorithm.
Challenges	Filter co-efficient selection, Algorithm to use, Target board selection.
Tools	Xilinx ISE 9.1i Simulator