Profile Information
RV-VLSI ID: 1ADADB263516

Career Objective

- Looking forward to work as a Full Custom Layout Engineer in a challenging environment to prove my potential & seeking to work on lower technology node

Core Competancy

- Clear vision of full custom IC design flow and ASIC design flow.
- Good understanding in MOS theory.
- Thorough Knowledge of IC fabrication process/semiconductor manufacturing.
- Well understanding the impact of DRC violation of the layout in terms of yield.
- Experienced the different types of major errors occurred during LVS physical verification.
- Hands on experience in doing analog layout along with device matching techniques.
- Fundamentals of DFM issues like LOD, EOL, ANT, ESD, latch-up and EM.
- Hands-on-layout in 180nm, 90nm, 28nm technology processes.
- Familiar with EDA tools from Mentor Graphics Pyxis- schematic and layout editor,calibre tools(LVS, DRC and PEX).
- Working knowledge of Linux.

Education Details				
Degree	**Discipline**	**School/College**	**Year of passing**	**Aggregate**
PG Diploma	Advanced Diploma in ASIC Design - Full Custom	RV-VLSI Design Center	2015	-
Degree	Electronics and Communication	Nandi Institute Of Technology And Management Sciences	2015	70.55
PUC	-	krishna Teja Junior College	2010	81.5
SSLC	-	Siddhartha High School	2008	82.33

Project Details

Project Title	LVS error clearance of 180nm D Flip Flop
Institue Name	RV-VLSI DESIGN Center
Project Description	Run Caliber LVS on D- flip flop.
Tools Used	Calibre from Mentor Graphics.
Challenges	*Analyzing hierarchical LVS report structure.*Identifying issues in source netlist for eg., Missing globals like VDD,VSS.*Identifying shorts and opens.*Missing ports, nets and Instances.*Property errors.

Project Title	9 Track STANDARD CELL LIBRARY DESIGN in 90nm process with DRC, LVS and Compatibility clean

Institue Name	RV-VLSI DESIGN Center
Project Description	Architect the layout of the standard cells with different drive strengths and with DRC, LVS and compatibility clean for a standard cell library.Combinational Circuit: INVX1, XOR2X1, NAND4X1,AOI22X2,MUX21X2.Sequential Circuit : D Flip Flop : DFFX2
Tools Used	ICStudio from Mentor Graphics1.Pyxis (Schematic and Layout Editor).2.Calibre(DRC, LVS, Compatibility checks).
Challenges	1.To get a optimized layout by placing the complete layout within the PR-Boundary and maintaining DRC rules.2.Layout optimization techniques for better floor planning.3.To reduce parasitics.4.To make route efficient layout.5.Analyzing LVS results.

Project Title	Two Stage Op-Amp Layout in 180nm process
Institue Name	RV-VLSI DESIGN Center
Project Description	To architect the layout of two-stage Op-amp.
Tools Used	ICStudio from Mentor Graphics1.Pyxis (Schematic and Layout Editor).2.Calibre(DRC, LVS, Compatibility checks).
Challenges	1. Floor planning and dummy placement for sensitive transistor pair and providing guard ring for protection.2. Effective floor planning using interdigitization patterns like centroid matching, symmetry, compact and dispersion.3. Minimum parasitics.

Project Title	Review of 180nm, 90nm and 28nm process technology files.
Institue Name	RV-VLSI DESIGN Center
Project Description	To review and analyze of various process technologies rule files like 180nm, 90nm and 28nm.
Tools Used	Jazz semiconductors document
Challenges	To understand all DRC rules required for layout designing.

Project Title	Leaf cells layout design of SRAM in 28nm technology process
Institue Name	RV-VLSI DESIGN Center
Project Description	To draw the layout of all the leaf cells of 6T SRAM : Undergoing DRC and LVS laef cell layout designing of precharge amplifier block.
Tools Used	ICStudio from Mentor Graphics1.Pyxis (Schematic and Layout Editor).2.Calibre(DRC, LVS, Compatibility checks).
Challenges	1. Efficient routing 2.Multiple floor plans to arrive at optimized area utilization.

Project Name	Driver Drowsiness Detection And Alerting System
Institute Name	Nandi Institute Of Technology And Management Sciences
Project Description	The system involves a real-time driver fatigue monitor(RTOS) and had been validated under real life human fatigue conditions. Accident prevention

Challenges	1.To build a system under Real time operating system. 2.To validate under different real life human fatigue conditions like with/without glasses, with different ethic backgrounds. 3.To make the system reliable,compact,low cost and user friendly.
Tools	Raspberry Pi board(Model B),Linux OS,OpenCV.