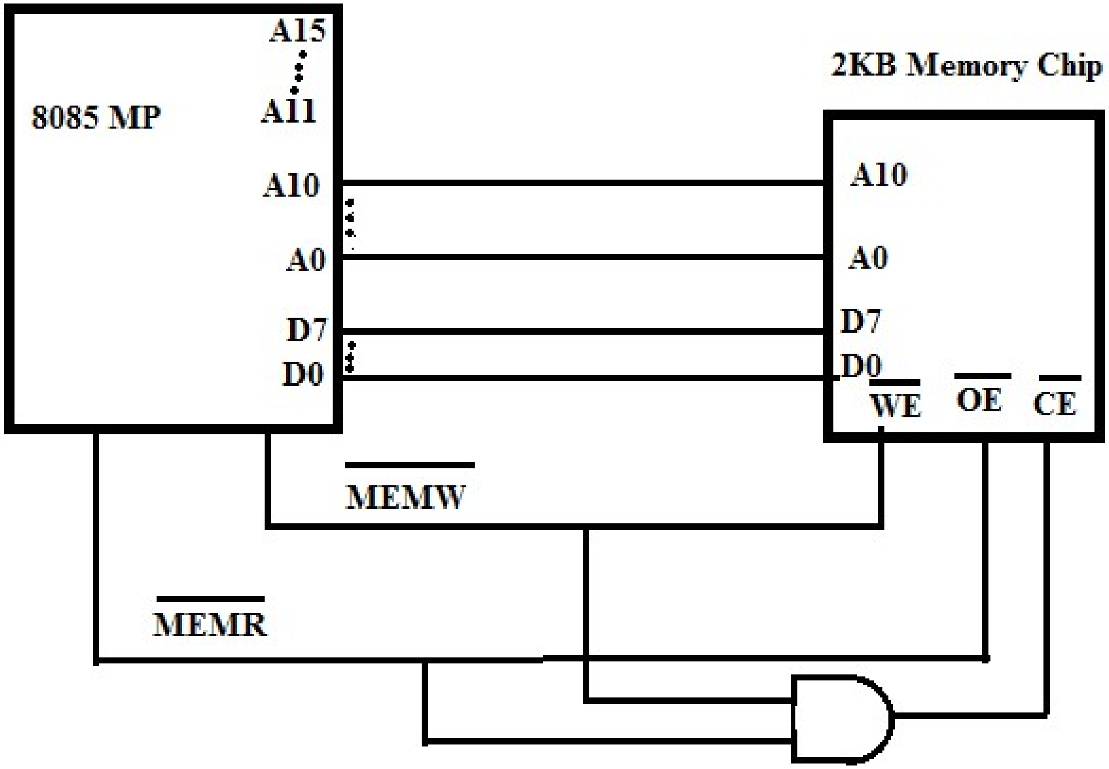
UNIT 5

BASIC I/O, MEMORY R/W AND INTERRUPT OPERATIONS (6 HRS.)

Memory Read/Write Operation



- In the above figure, the lower address lines A0 – A10 of MP are connected to A0– A10 pins of memory (2KB) and D0 – D7 data lines of MP are connected to D0 – D7 of the same memory.
- The memory read control signal MEMR(bar) and memory write control signal MEMW(bar) are connected to OE(bar) and WE(bar) pins of memory for read and write operation respectively.
- When Processor issues MEMW(bar) control signal to memory, then memory stores the data available in data lines into the addressed location. This process is known as ***memory write operation.***
- When MP issued MEMR(bar) control signal to memory, then memory places the data stored in addressed location towards the processor. This process is known as ***memory read operation.***

Memory mapped I/O, I/O Mapped I/O and Hybrid I/O

- I/O interfacing is the link between the processor or CPU and the various I/O peripherals such as the keyboard, printer, mouse, etc.
- Can be done in ***two ways***:

1. ***Memory-Mapped I/O Interfacing***
2. ***I/O Mapped I/O Interfacing (isolated I/O interfacing).***

I/O mapped I/O

- Devices are given a separate addressing region from the memory known as ‘ports’.
- 8-bit address lines for creating this special address space for the I/O devices in 8085, i.e. 2^8=256 bytes of address space (00h-ffh).
- Dedicated address region for ***I/O***s and have dedicated ***I/O*** instructions.
- ***I/O mapped I/Os*** can send/receive data from the processor using ***IN*** and ***OUT*** commands only.
- None of the ***ALU*** operations can be directly applied to the data of the ***I/O mapped I/***O devices.

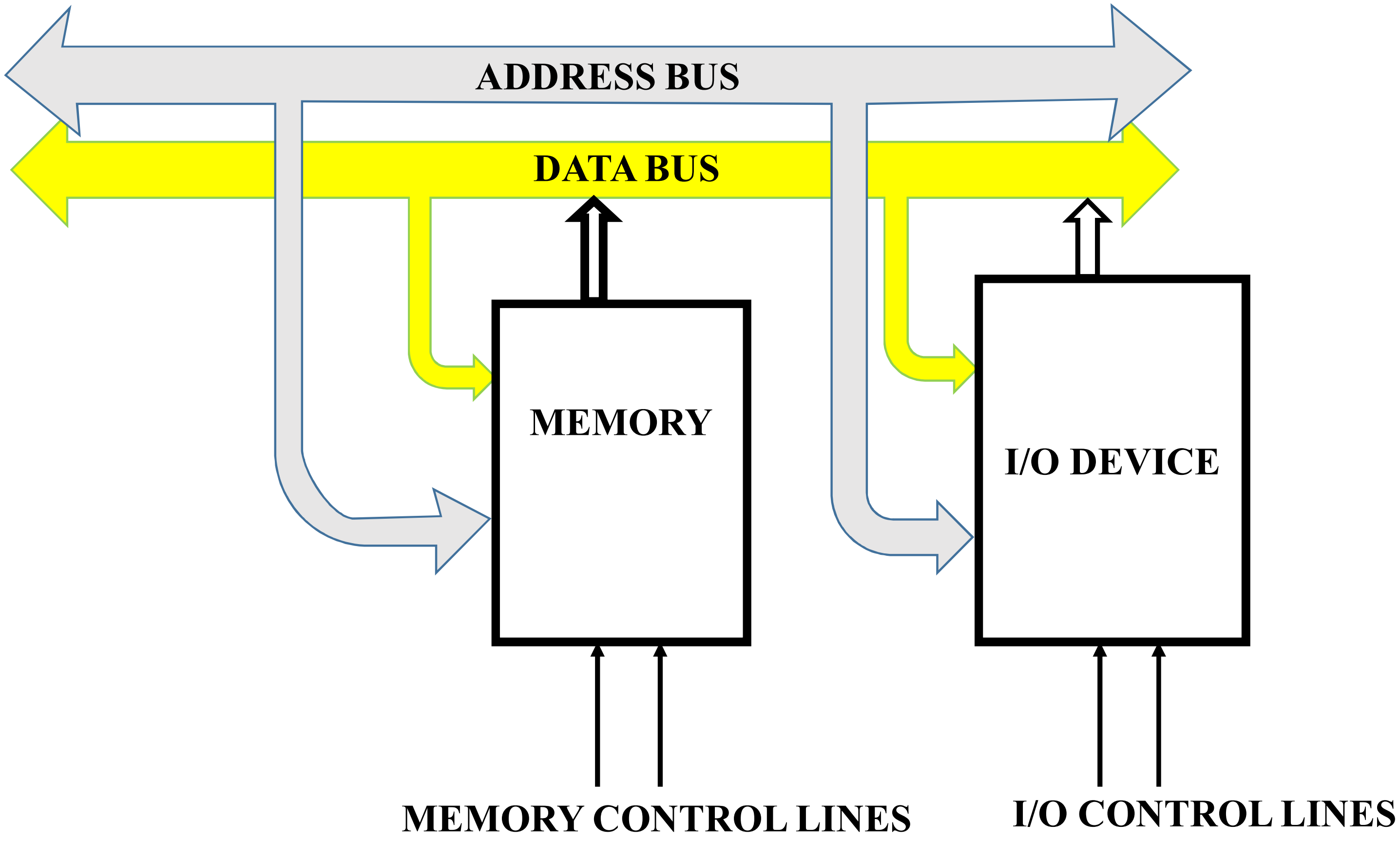


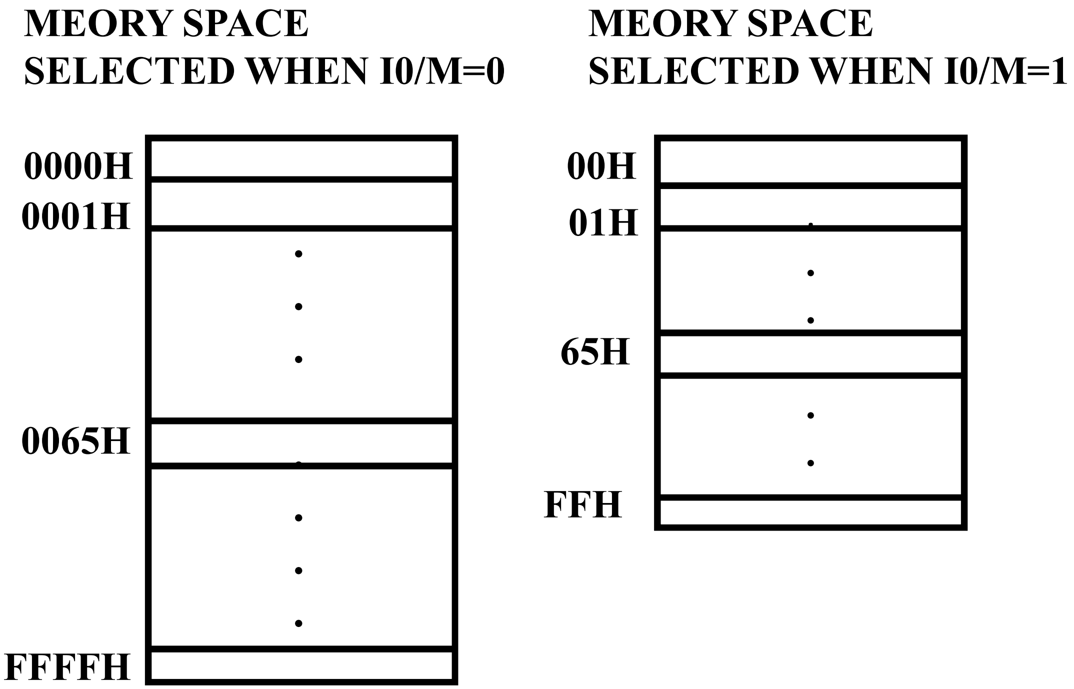
FIG: isolated I/O interfacing

Advantages

- There is minimal logic involved in decoding a discrete address for the interfaced peripheral.
- We get special instructions only for I/O.
- Since these I/Os have a separate address space (8-bits), the entire 64K bytes (16-bit address line) is available just for memory.
- The whole system is smaller and less complicated.
- This method works faster due to lesser delays.

Disadvantages

- Compared to the Memory Mapped I/O, more instructions are required to complete the same task.
- Arithmetic and Logical instructions cannot be applied to the data.
- Less powerful and flexible than memory-mapped I/O.
- We need extra control signal lines to switch between the two different address spaces that are created in I/O mapped I/O. This increases the number of pins.



- We get two separate address spaces when we use IO mapped IO method to interface I/O devices.
- The I/O devices get their own special memory space.
- We can choose which address space to communicate with using the IO/M pin.

Memory Mapped I/O

- The processor treats the I/O devices like any other memory location.
- The ***I/O*** devices are efficiently mapped into the system memory along with the RAM and ROM memory.
- These devices are assigned with a 16-bit address value within the entire address range of the intel 8085 microprocessor.
- Exchange of data takes place with the help of memory instructions.
- The ***I/O*** device information can also be sent to the ***ALU.***
- The ***LOAD*** and ***STORE*** instructions are executed to read from and write to the I/O devices, just like they are utilized for the memory.

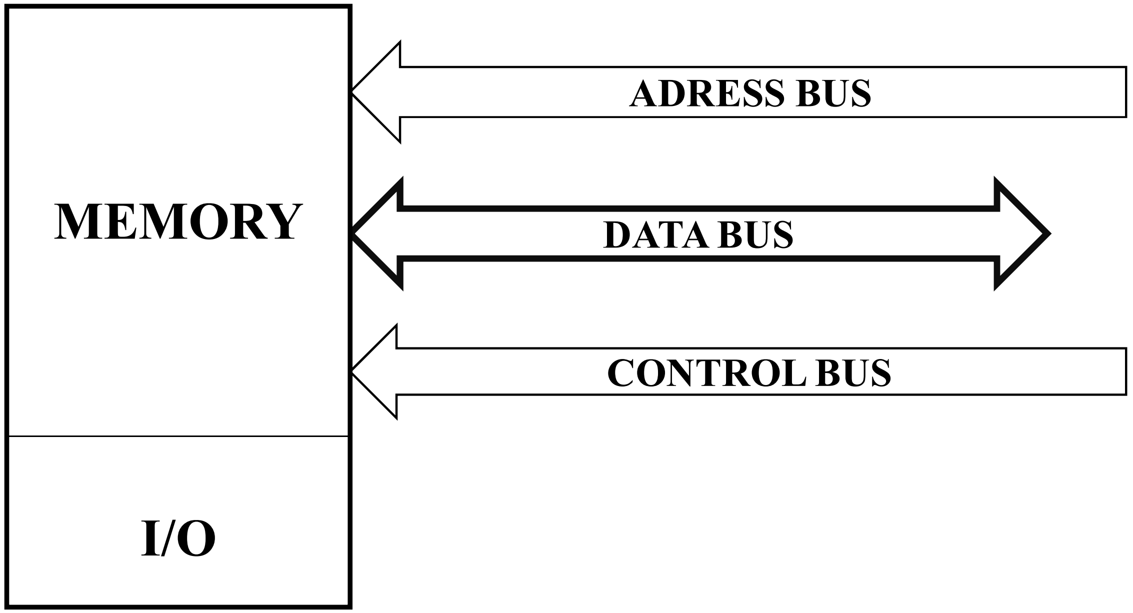


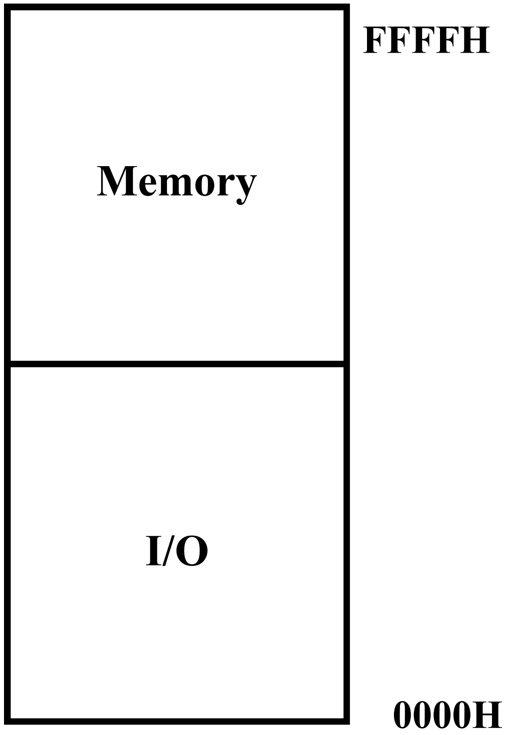
Fig: Memory-Mapped I/O Interfacing

Advantages

- Gives us a ***single address space***, as well as a ***common set of instructions*** to be used for both the memory & I/O operations.
- The memory ***ordering rules*** & memory ***barriers*** can be defined here, which will apply both to the device accesses and normal memory.
- The same ***memory mapping mechanisms*** which are used for other memory can be used to gain ***access to the devices*** as well.
- ***Beneficial*** to use the ***low-latency buses*** in the system.
- The I/O intensive operations can be ***much quicker***.
- ***Separate control*** signals are ***not required*** since there is ***no switching*** between two different address spaces.

Disadvantages

- The working of the ***cache controller*** gets ***complicated***, as the interfaced peripherals differ in their behavior when compared to normal memory.
- The instruction ***scheduling*** becomes ***more difficult*** as the processor cannot recognize if any information is loaded/stored in the memory or in the device.
- The entire address bus has to be ***fully decoded*** for every peripheral.
- The more the system bit configuration, the ***more is the cost*** of adding the machine with extra ***complex hardware***.
- The mode works much ***slower*** than I/O mapped I/O interfacing.



Unified address space for both, memory and I/O

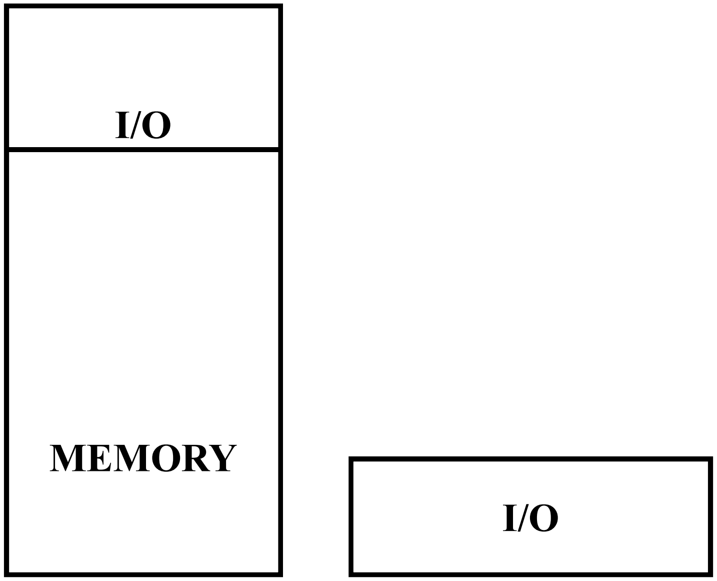
Differences between I/O mapped I/O and Memory-mapped I/O

Memory-Mapped I/O Interfacing	I/O Mapped I/O Interfacing
The I/O devices and memory, both are treated as memory.	Treated separately.
The I/O devices are provided with 16-bit address values (in 8085)	The I/O devices are provided with 8-bit address values. (In 8085)
The interfaced devices are accessed by the memory read or memory write cycles.	The interfaced devices are accessed by the I/O read or I/O write cycles.
The peripherals or the I/O ports are treated as memory locations. Thus, all the instructions related to the memory can be utilized for the data exchange between the processor and the I/O device.	Only the IN and the OUT instructions can be use for transferring information between the I/O device and the processor.

Memory-Mapped I/O Interfacing	**I/O Mapped I/O Interfacing**
In the memory-mapped ports, the information data can be moved to the I/O devices from any register or vice versa.	In the I/O mapped ports, the information bytes can be moved around between the ports and the accumulator register only.
The full memory address space cannot be used solely for addressing memory for interfacing.	The full memory address space can be used solely for addressing memory for interfacing.
Data transfer is possible between any register and I/O device.	Data transfer is possible between the accumulator and I/O device only.
Here, a large number of I/O ports (2^{16} ports) are possible to be used for interfacing.	Only 256 I/O ports i.e., 2^{8} ports, are made available for interfacing.
While executing the memory, write or read cycles, the $IO/\overline{M}$ is set to low ($IO/\overline{M} = 0$).	While executing the I/O write or read cycles, the $IO/\overline{M}$ is set to high ($IO/\overline{M} = 1$).
We can perform arithmetic and logical operations on the data.	We cannot perform arithmetic and logical operations on the data.
more decoder hardware involved	less decoder hardware involved.

Hybrid I/O

- Two address spaces


I/O
MEMORY
I/O