# Unit 3

## Timing Diagram

## T-State:

- It is the time period of a single cycle of the clock frequency.
- It is the basic unit used to calculate the time taken for execution the instruction and program in a processor.

## Machine Cycle:

- The time period (number of T-states) required by microprocessor to perform a read or a write operation either from memory or I/O device.
- In machine cycle various operations like op-code fetch, memory read, memory write, I/O read, I/O write are performed.
- A machine cycle may consist of three to six T-states.

## Instruction Cycle:

- It is the total number of machine cycles required to execute a complete instruction i.e. Fetching and execution of one instruction. The fetch and execute cycles are carried out in synchronization with the clock.

# Machine Cycles of 8085 microprocessor:

The 8085 microprocessor has 5 machine cycles. They are:

## 1. Op-code fetch cycle:

- Each instruction of the processor has one-byte op-code.
- The microprocessor uses this cycle to take the op-code of an instruction from the memory location to processor.
- The op-code is taken from memory and transferred to instruction register for decoding and execution. Hence, every instruction starts with op-code fetch machine cycle.
- The time required to complete this cycle is 4 to 6 T-states. In this time, the first, 3 T-states are used for fetching the op-code from memory and the remaining T-states are used for internal operations by the processor.

## 2. Memory read cycle:

- The microprocessor executes these cycles to read data from memory. The address of memory location is given by instruction.
- The time required to complete the memory read cycle is 3 T-states.

## 3. Memory write cycle:

- The microprocessor executes these cycles to write data to memory. The address of memory is given by instructions.
- The time required to complete the memory write cycle is 3 T-states.

## 4. I/O read cycle:

- The microprocessor executes these cycles to read data from I/O devices.
- The address of I/O port is given by instruction.
- The time required to complete the I/O read cycle is 3 T-states.

## 5. I/O write cycle:

- The microprocessor executes these cycles to write data into I/O devices.
- The address of I/O port is given by instruction.
- The time required to complete the I/O write cycle is 3 T-states.

## 6. Interrupt acknowledge cycle:

- In the response to interrupt request input **INTR**, the microprocessor executes these cycles to get information from the interrupting devices.
- The time required to complete this cycle is 3 T-states.

## Fetch & Execute Operation: Timing Diagram:

- The graphical representation of status of various signals involved during a machine cycle with respect to time is called timing diagram.
- This gives basic idea of what is happening in the system when the instruction is getting fetched and executed, at what instant which signal is getting activated.
- The signals involved during machine cycle are CLK, A15 – A8, AD7 – AD0, IO/ $\overline{M}$, **$\overline{Rd}$, $\overline{WR}$** and **S1, S0**.

| IO/ $\overline{M}$ | S 1 | S0 | Operation |
|---|---|---|---|
| 0 | 0 | 0 | Halt |
| 0 | 0 | 1 | Memory write |
| 0 | 1 | 0 | Memory read |
| 0 | 1 | 1 | Op-code fetch |
| 1 | 0 | 1 | IO write |
| 1 | 1 | 0 | IO read |
| 1 | 1 | 1 | Interrupt acknowledge |

## Timing diagram for op-code fetch cycle:

The op-code fetch timing diagram can be explained as below:

1) The microprocessor places the 16-bit memory address from the program counter on address bus. At time period T1, the higher order memory address is placed on the address lines A15 – A8. At the same time ALE is high, the lower address is placed on the bus AD7 – AD0. The status signal IO/ $\overline{M}$ goes low indicating the memory operation and two status signals S1 = 1, S0 = 1 to indicate op-code fetch operation.
2) At time period T2, the microprocessor sends **Rd**(bar) control line to enable the memory read. When memory is enabled with $\overline{\textbf{Rd}}$ signal, the op-code value from the addressed memory location is placed on the data bus with ALE low.
3) The op-code value is reached at processor register during T3 time period. When data (op-code value) is arrived, the $\overline{\textbf{Rd}}$ signal goes high. It causes the bus to go into high impedance state.
4) The op-code byte is placed in instruction decoder of microprocessor and the op-code is decoded and executed. This happens during time period T4.

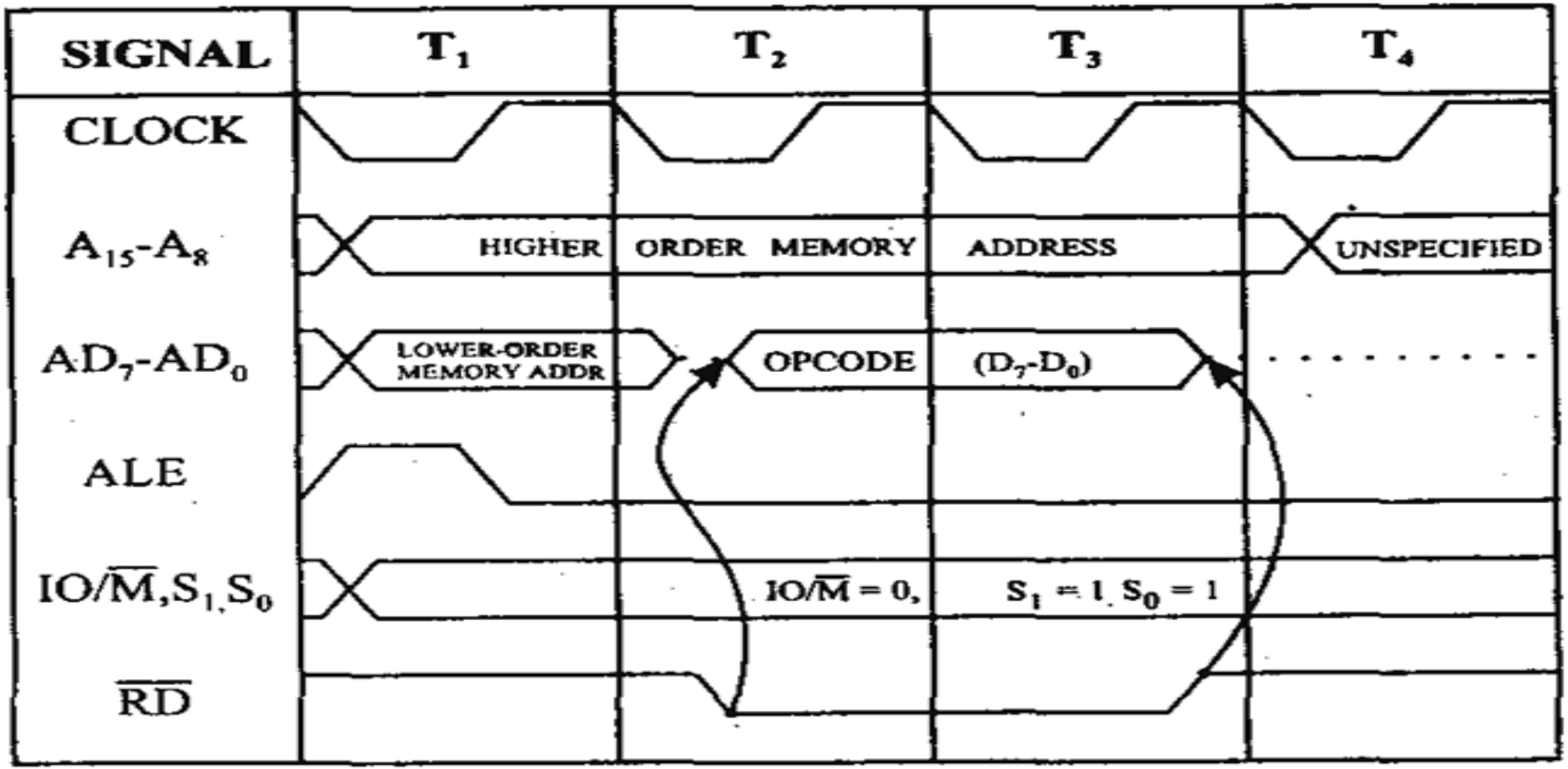


Fig: Timing Diagram for Op-code Fetch Machine Cycle

## **Timing diagram for memory read cycle**:

The memory read timing diagram can be explained as below:

1) The microprocessor places the 16-bit memory address from the program counter on address bus. At time period T1, the higher order memory address is placed on the address lines A15 – A8. At the same time ALE is high, the lower address is placed on the bus AD7 – AD0. The status signal IO/ $\overline{M}$ goes low indicating the memory operation and two status signals S1 = 1, S0 = 0 to indicate memory read operation.
2) At time period T2, the microprocessor sends $\overline{\mathbf{RD}}$(bar) control line to enable the memory read. When memory is enabled with $\overline{\mathbf{RD}}$ signal, the data from the addressed memory location is placed on the data bus with ALE low.
3) The data is reached at processor register during T3 state. When data is arrived, the $\overline{\mathbf{RD}}$ signal goes high. It causes the bus to go into high impedance state.

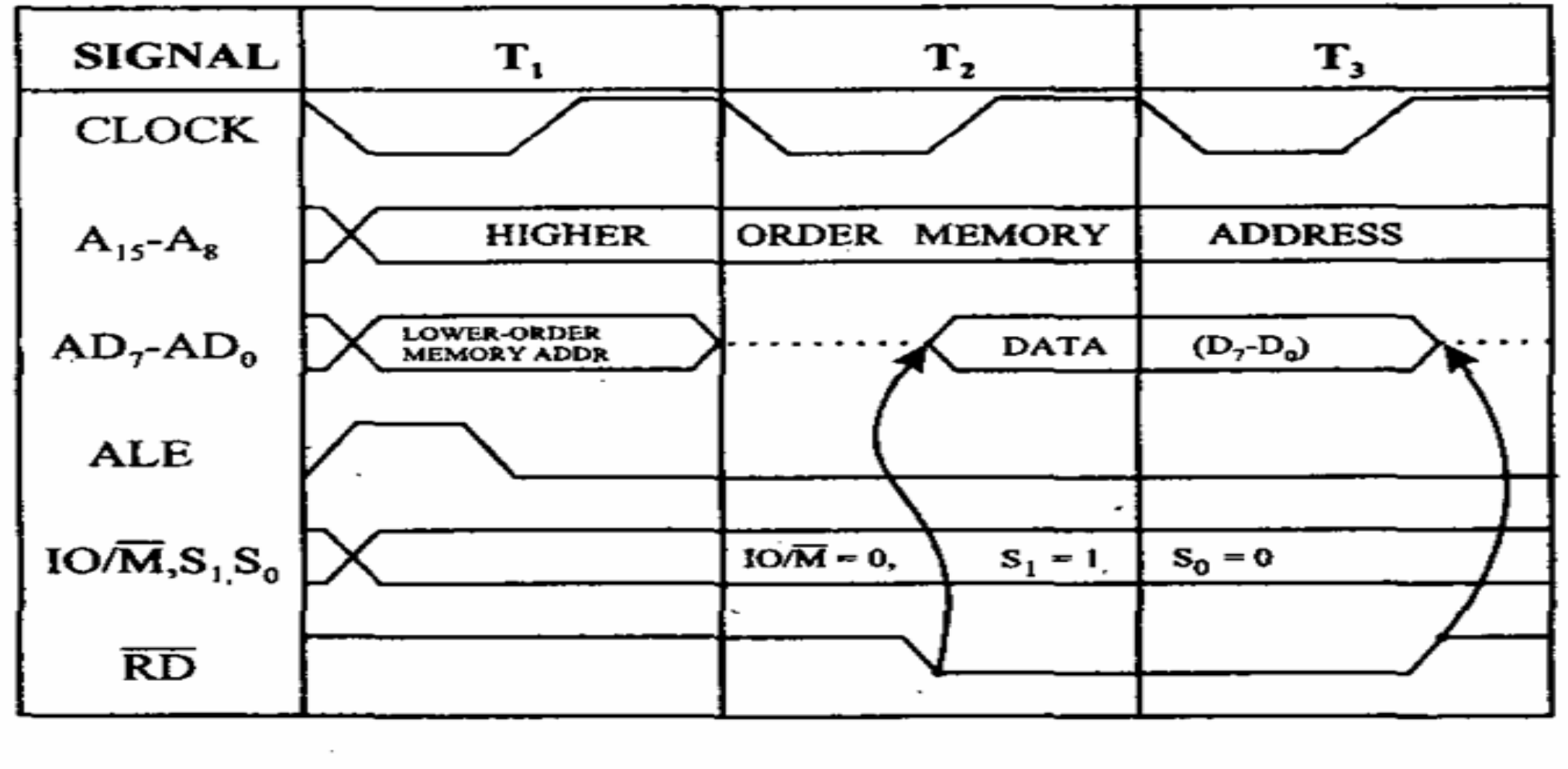


Fig: Timing Diagram for Memory Read Machine Cycle

## Timing diagram for memory write cycle:

The memory write timing diagram can be explained as below:

1) The microprocessor places the 16-bit memory address from the program counter on address bus. At time period T1, the higher order memory address is placed on the address lines A15 – A8. At the same time ALE is high, the lower address is placed on the bus AD7 – AD0. The status signal IO/ $\bar{M}$ goes low indicating the memory operation and two status signals S1 = 0, S0 = 1 to indicate memory write operation.

1) At time period T2, the microprocessor sends $\bar{W}\bar{R}$ control line to enable the memory write. When memory is enabled with $\bar{W}\bar{R}$ signal, the data from the processor is placed on the addressed location with ALE low.

1) The data is reached at memory location during T3 state. When data is reached, the $\bar{W}\bar{R}$ (bar) signal goes high. It causes the bus to go into high impedance state.

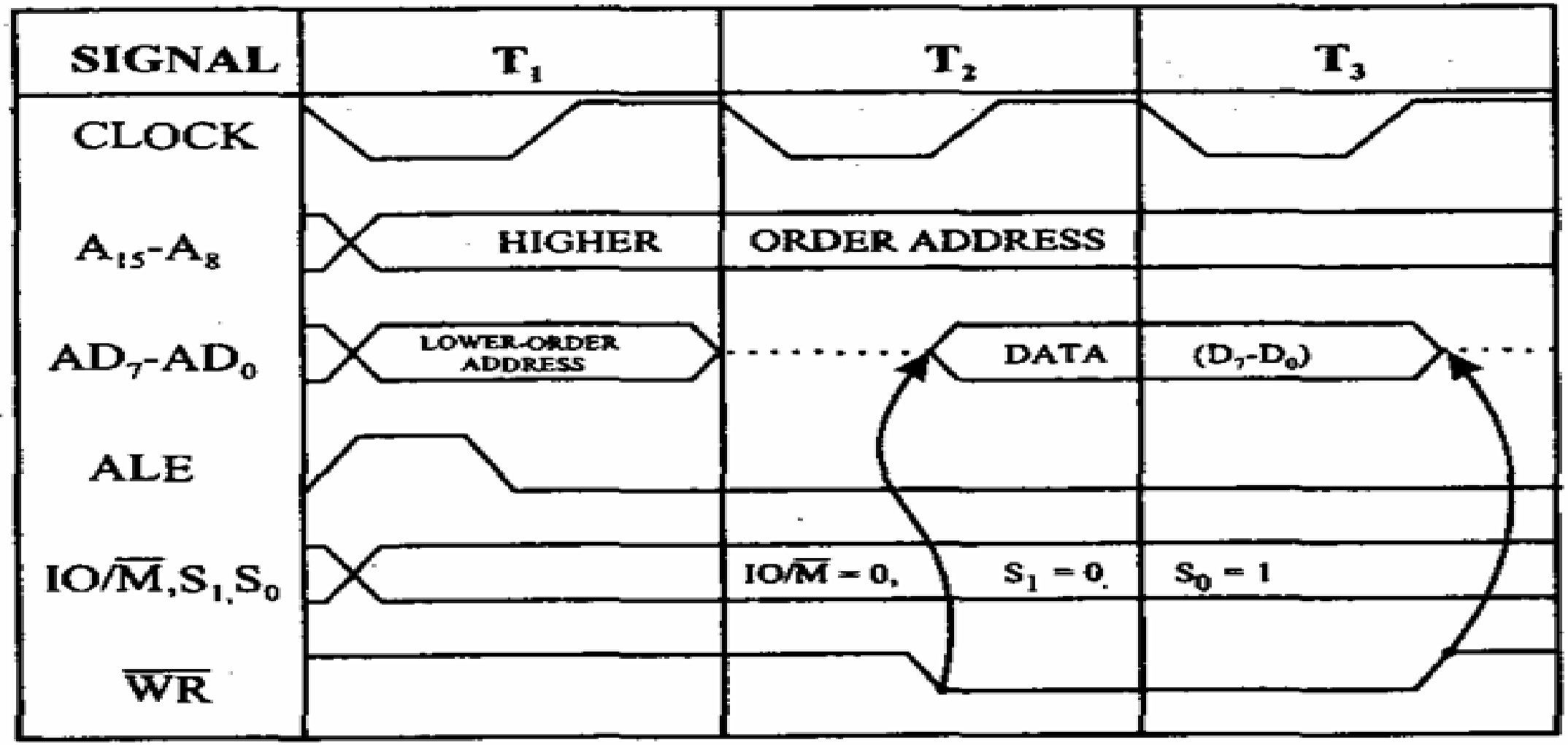


Fig: Timing Diagram for Memory Write Machine Cycle

# Timing diagram for I/O read cycle:

**Operation:**

It is used to fetch one byte from an IO port. It requires 3 T-States.

1) During T1, The Lower Byte of IO address is duplicated into higher order address bus A8-A15. ALE is high and AD0-AD7 contains address of IO device. IO/M (bar) goes high as it is an IO operation.
2) During T2, ALE goes low, RD (bar) goes low and data appears on AD0-AD7 as input from IO device.
3) During T3 Data remains on AD0-AD7 till RD(bar) is low.

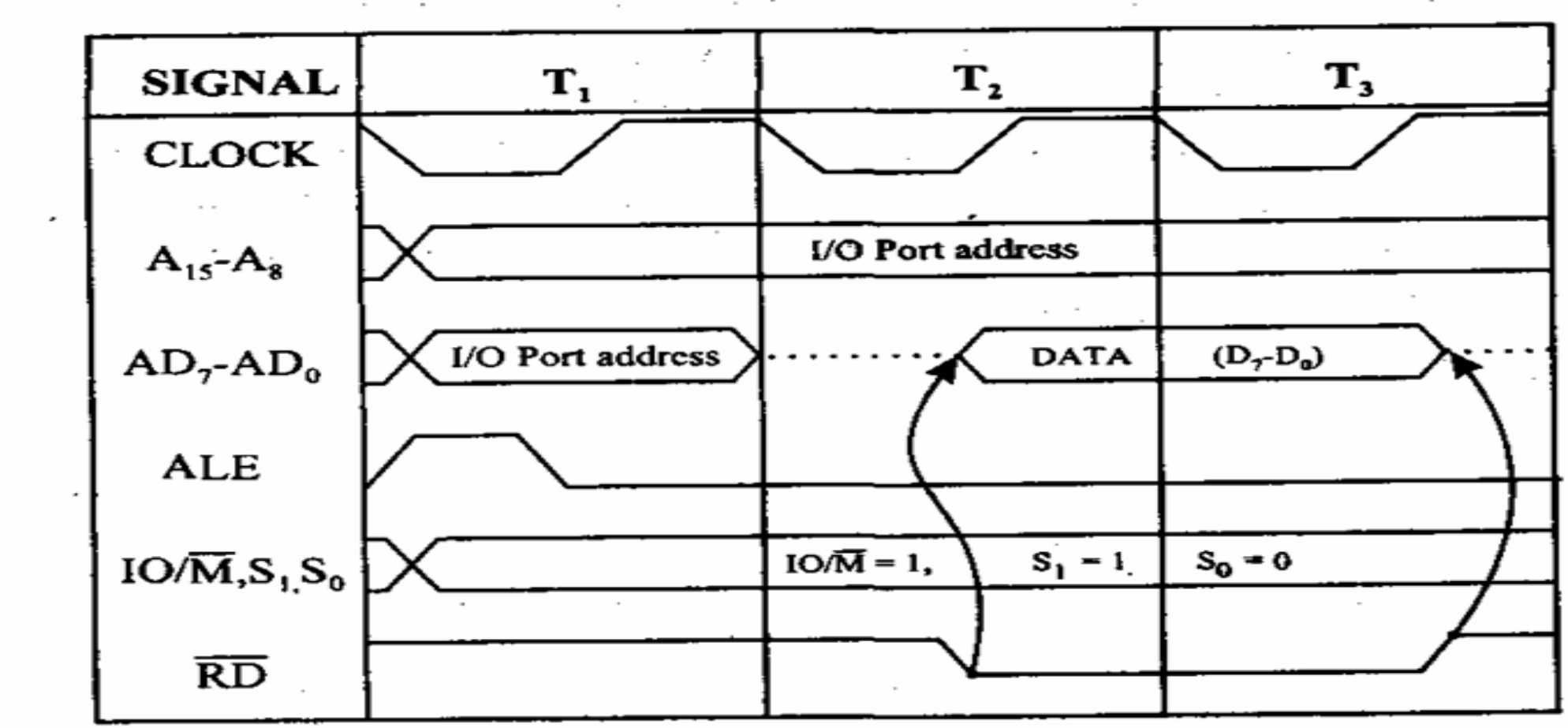


Fig: Timing Diagram for I/O Read Machine Cycle

# Timing diagram for I/O write cycle:

**Operation:**

It is used to writ one byte into IO device. It requires 3 T-States.

1) During T1, the lower byte of address is duplicated into higher order address bus A8-A15. ALE is high and A0-A7 address is selected from AD0-AD7. As it is an IO operation IO/M (bar) goes high.
2) During T2, ALE goes low, WR (bar) goes low and data appears on AD0-AD7 to write data into IO device.
3) During T3, Data remains on AD0-AD7 till WR(bar) is low.

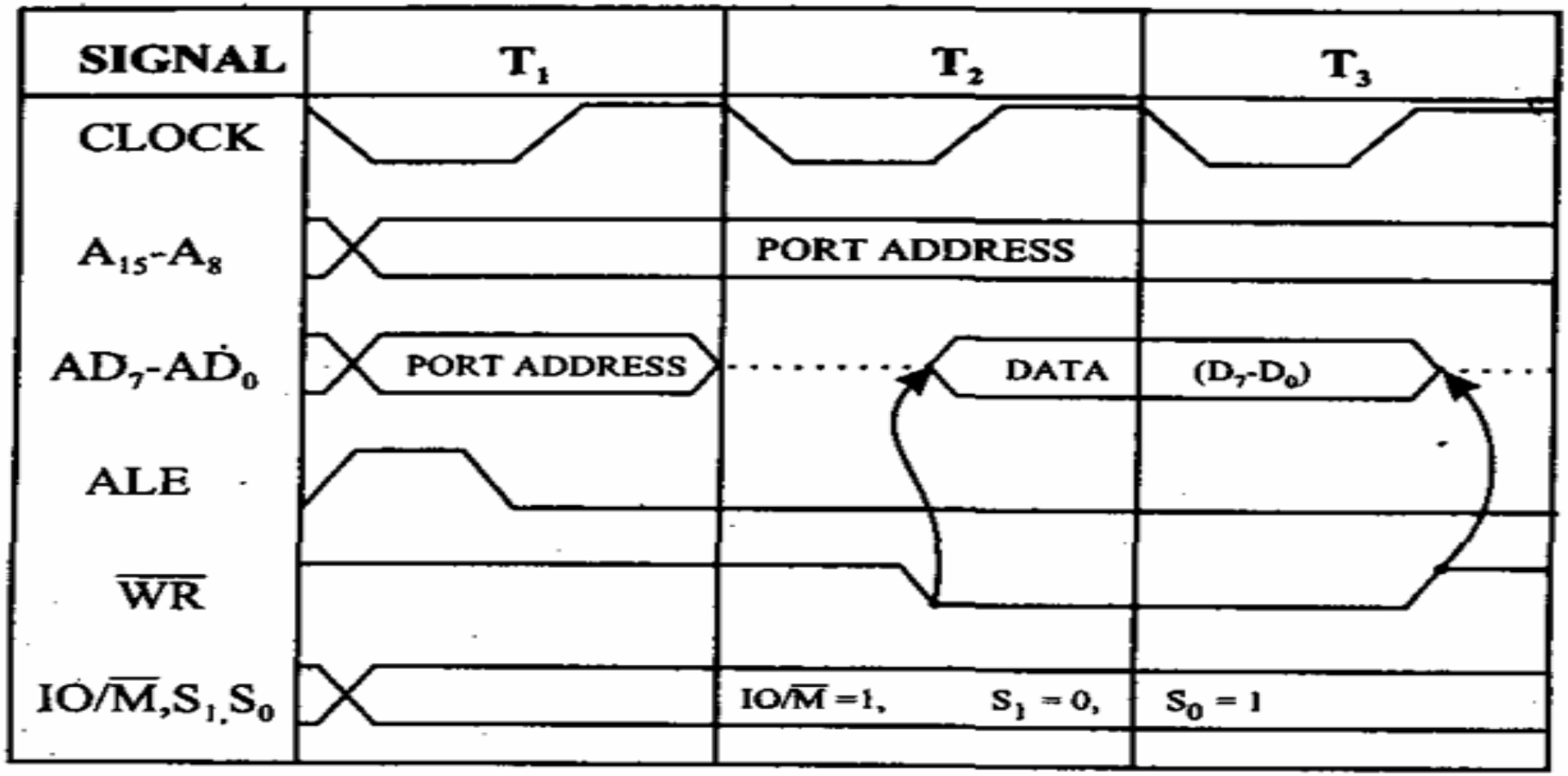


Fig: Timing Diagram for I/O Write Machine Cycle