80386_MICROPROCESSOR

FEATURES OF 80386:

- **Two versions of 80386 are commonly available:**

  1) 80386DX

  2)80386SX

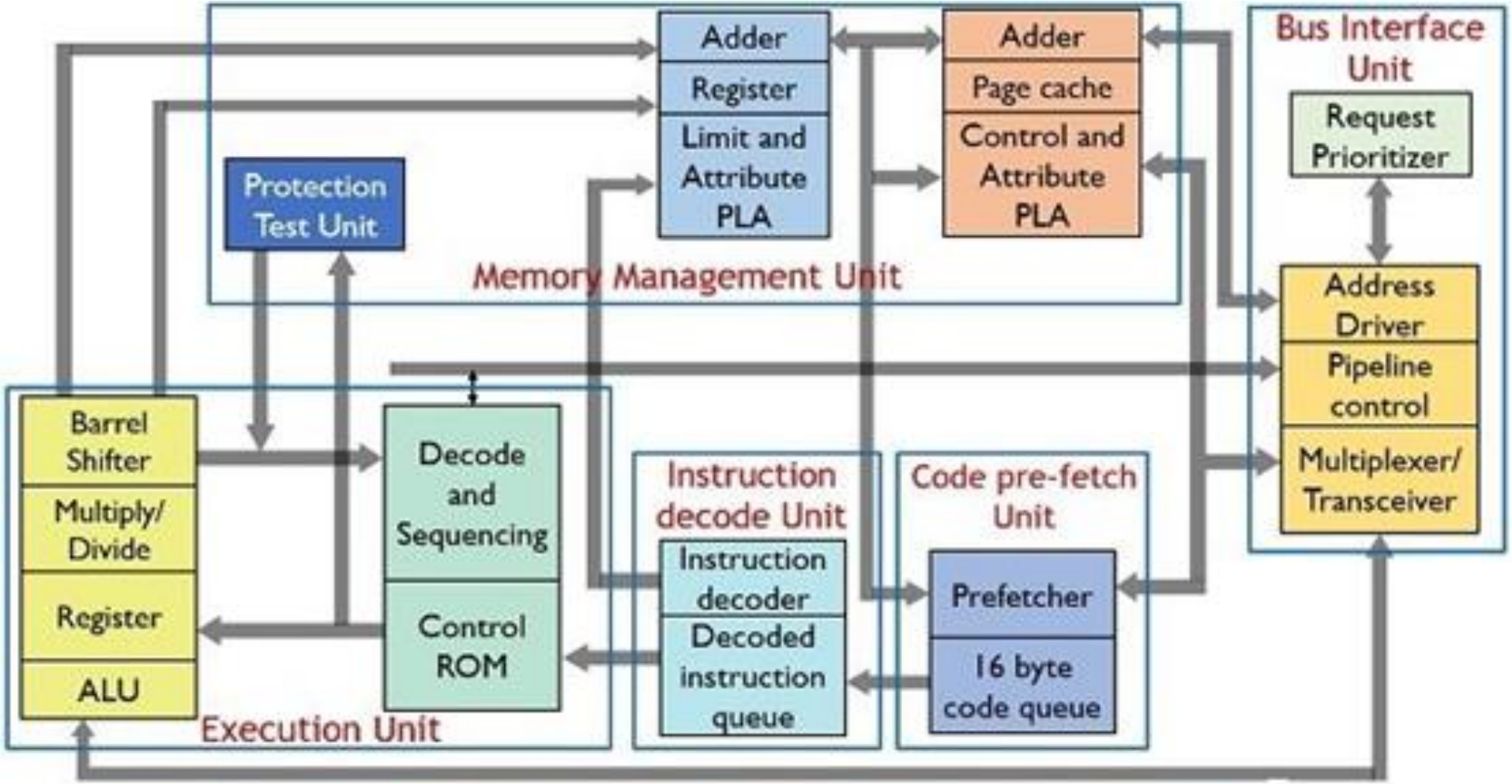
80386DX	*80386SX*
32 bit address bus	**24 bit address bus**
32bit data bus	**16 bit data bus**
Packaged in 132 pin ceramic pin grid array(PGA)	**100 pin flat package**
Address 4GB of memory	**16 MB of memory**

- **80386SX was developed after the DX for application that didn't require the full 32-bit bus version.**

- **It is found in many PCs use the same basic mother board design as the 80286.**
- **Most application less than the 16MB of memory ,so the SX is popular and less costly version of the 80386 microprocessor.**
  - **The 80386 CPU supports 16k no. of segments and thus total virtual memory space is 4GB *16 k=64 Tb**
  - **Memory management section supports**
    - **Virtual memory**
    - **Paging**
    - **4 levels of protection**
  - **20-33 MHz frequency**

ARCHITECTURE OF 80386

- **The Internal Architecture of 80386 is divided into 3 sections:**
  i. ***Central processing unit(CPU)***
  ii. ***Memory management unit(MMU)***
  iii. ***Bus interface unit(BIU)***
- **Central processing unit is further divided into:**
  - ***Execution unit(EU) and Instruction unit(IU)***
- **Execution unit has 8 General purpose and 8 Special purpose registers which are either used for handling data or calculating offset addresses.**



Architecture of 80386 Microprocessor

- **The Instruction unit decodes the opcode bytes received from the 16-byte instruction code queue and arranges them in a 3-instruction decoded instruction queue.**
- **After decoding them pass it to the control section for deriving the necessary control signals. The barrel shifter increases the speed of all shift and rotate operations.**
- **The multiply / divide logic implements the bit-shift-rotate algorithms to complete the operations in minimum time.**
- **Even 32- bit multiplications can be executed within one microsecond by the multiply / divide logic.**

- **The Memory management unit consists of:**
  - ***Segmentation unit and***
  - ***Paging unit.***
- **Segmentation unit allows the use of two address components, viz. segment and offset for relocability and sharing of code and data.**
- **Segmentation unit allows segments of size 4Gbytes at max.**
- **The Paging unit organizes the physical memory in terms of pages of 4kbytes size each.**
- **Paging unit works under the control of the segmentation unit, i.e. each segment is further divided into pages. The virtual memory is also organizes in terms of segments and pages by the memory management unit.**

- **The Segmentation unit provides a 4 level protection mechanism for protecting and isolating the system code and data from those of the application program.**
- **Paging unit converts linear addresses into physical addresses.**
- **The control and attribute PLA checks the privileges at the page level. Each of the pages maintains the paging information of the task. The limit and attribute PLA checks segment limits and attributes at segment level to avoid invalid accesses to code and data in the memory segments.**
- **The Bus control unit has a prioritizer to resolve the priority of the various bus requests. This controls the access of the bus. The address driver drives the bus enable and address signal A0 – A31. The pipeline and dynamic bus sizing unit handle the related control signals.**
- **The data buffers interface the internal data bus with the system bus.**

REGISTER ORGANIZATION:

- **The 80386 has eight 32 - bit general purpose registers which may be used as either 8 bit or 16 bit registers.**
- **A 32 - bit register known as an extended register, is represented by the register name with prefix E.**
- **Example : A 32 bit register corresponding to AX is EAX, similarly BX is EBX etc.**
- **The 16 bit registers BP, SP, SI and DI in 8086 are now available with their extended size of 32 bit and are names as EBP,ESP,ESI and EDI.**
- **AX represents the lower 16 bit of the 32 bit register EAX.**

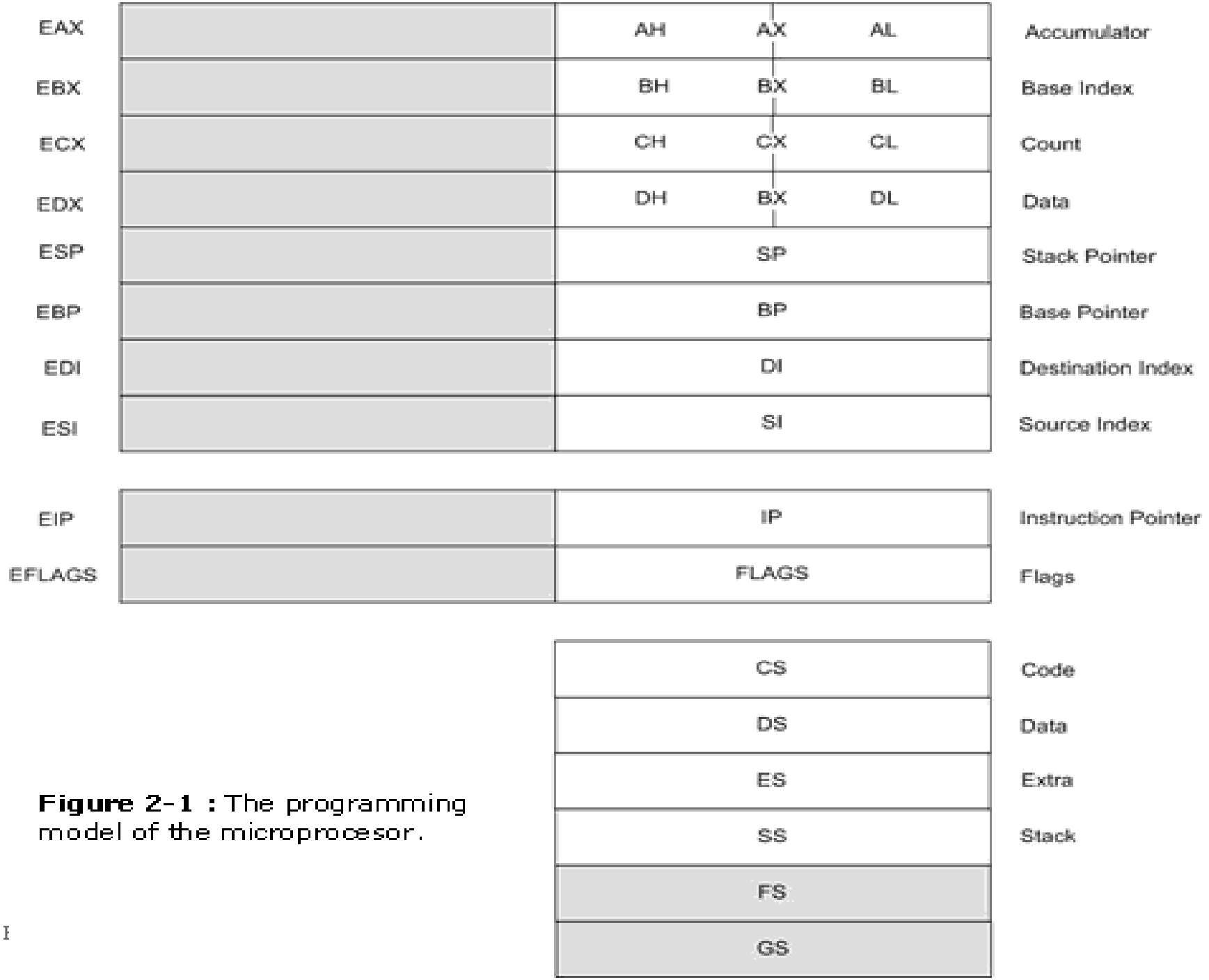


Figure 2-1 : The programming model of the microprocesor.

- **BP, SP, SI, DI represents the lower 16 bit of their 32 bit counterparts, and can be used as independent 16 bit registers.**
- **The six segment registers available in 80386 are CS, SS, DS,ES, FS and GS.**
- **The CS and SS are the code and the stack segment registers respectively, while DS, ES,FS, GS are 4 data segment registers.**
- **A 16 bit instruction pointer IP is available along with 32 bit counterpart EIP.**

FLAG REGISTER OF 80386:

D31-D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved	VM	RF	0	INT	IOPL	IOPL	OF	DF	IF	TF	SF	ZF	0	AF	0	PF	1	CF

- ***The Flag register of 80386 is a* 32 bit register. Out of the 32 bits, Intel has reserved bits D18 to D31, D5 and D3 are reset, while D1 is always set at 1.**
- **Two extra new flags are added to the 80286 flag to derive the flag register of 80386. They are VM and RF flags.**

- **VM - Virtual Mode Flag:**
  - ***If this flag is set, the*** **80386 enters the virtual 8086 mode within the protection mode.**
  - **This is to be set only when the 80386 is in protected mode. In this mode, if any privileged instruction is executed an exception 13 is generated. This bit can be set using IRET instruction or any task switch operation only in the protected mode.**
- **RF- Resume Flag:**
  - **This flag is used with the debug register breakpoints. It is checked at the starting of every instruction cycle and if it is set, any debug fault is ignored during the instruction cycle. The RF is automatically reset after successful execution of every instruction, except for IRET and POPF instructions.**
  - **Also, it is not automatically cleared after the successful execution of JMP, CALL and INT instruction causing a task switch. These instruction are used to set the RF to the value specified by the memory data available at the stack.**

Segment Descriptor Registers:

- This registers are not available for programmers, rather they are internally used to store the descriptor information, like attributes, limit and base addresses of segments.
- The six segment registers have corresponding six 73 bit descriptor registers. Each of them contains 32 bit base address, 32 bit base limit and 9 bit attributes.
- These are automatically loaded when the corresponding segments are loaded with selectors.

Control Registers:

- The 80386 has three 32 bit control registers CR0, CR2 and CR3 to hold global machine status independent of the executed task.
- Load and store instructions are available to access these registers.

System Address Registers:

- *Four special registers are* defined to refer to the descriptor tables supported by 80386.

- **The 80386 supports four types of descriptor table:**
  i. **Global descriptor table (GDT),**
  ii. **Interrupt descriptor table(IDT),**
  iii. **Local descriptor table (LDT) and**
  iv. **Task state segment descriptor (TSS).**
- **Debug and Test Registers:**
  - ***Intel has provide a set* of 8 debug registers for hardware debugging. Out of these eight registers DR0 to DR7, two registers DR4 and DR5 are Intel reserved.**
  - **The initial four registers DR0 to DR3 store four program controllable breakpoint addresses, while DR6 and DR7 respectively hold breakpoint status and breakpoint control information.**
  - **Two more test register are provided by 80386 for page caching namely test control and test status register.**

MEMORY PAGING

- The **memory paging mechanism allows any** physical memory location to be assigned to any linear address.
- **Linear address is defined as the address** generated by a program.
- **Physical address is the actual memory** location accessed by a program.
- With memory paging, the linear address is invisibly translated to any physical address.
- The linear address, as generated by software, is broken into three sections that are used to access the **page directory entry, page table entry, and memory page offset address.**

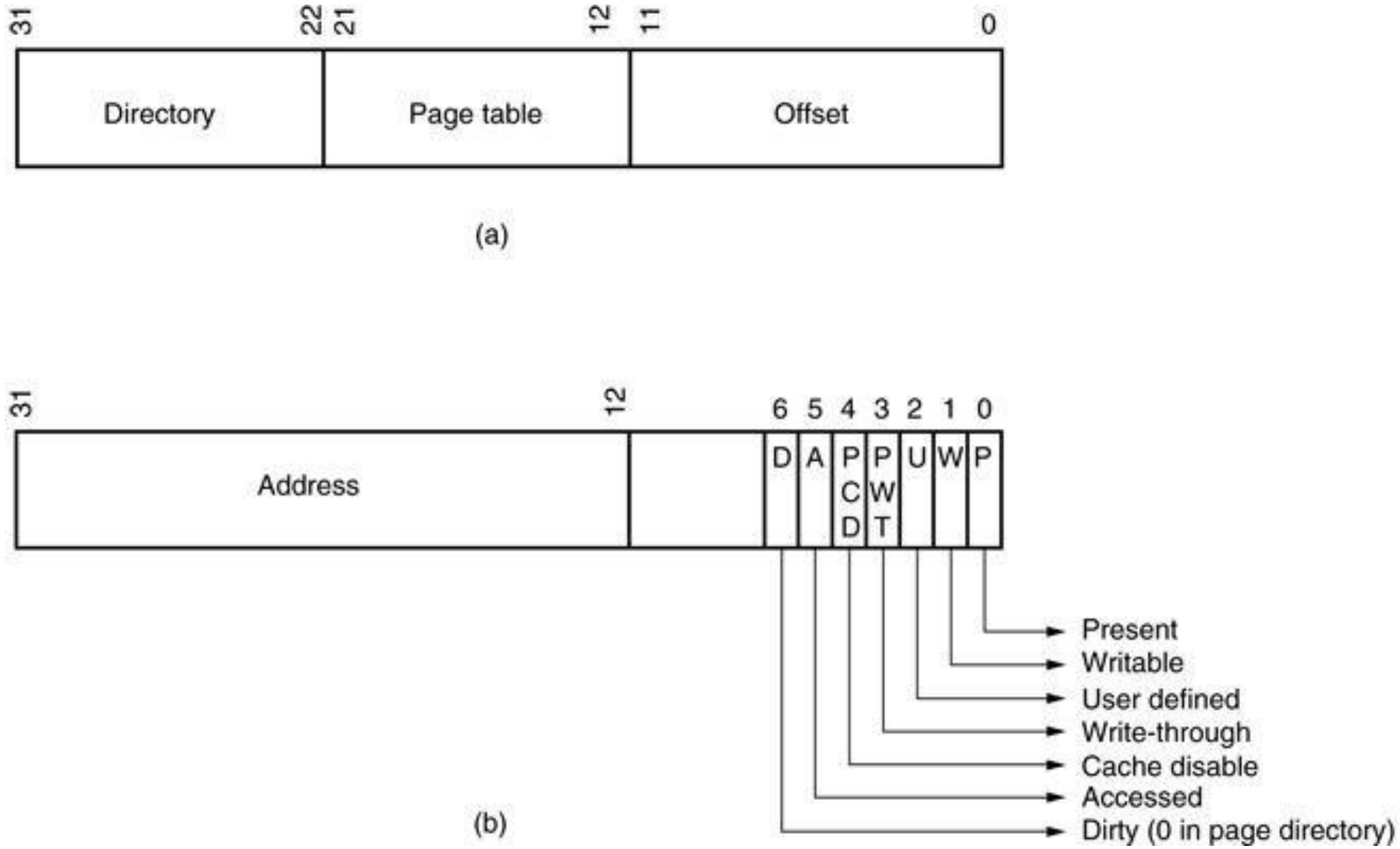


Figure 4: The format for the linear address (a) and a page directory or page table entry (b).

CALCULATING LINEAR ADDRESSES

- Given a segment address, multiply it by 16 (10H) (add a hexadecimal zero to the right), and add it to the offset.
- Example: convert 08F1:0100 to a linear address
  - Adjusted Segment value: 0 8 F 1 0
  - Add the offset: 0 1 0 0
  - Linear address: 0 9 0 1 0

THE PAGE DIRECTORY AND PAGE TABLE

- Only one page directory in the system.
- Page directory and each page table are 4K bytes in length.
- Figure 5 shows the page directory, a few page tables, and some memory pages.
- Intel has incorporated a special type of cache called TLB (**translation look-aside buffer).**
- The 80486 cache holds the 32 most recent page translation addresses.
  - if the same area of memory is accessed, the address is already present in the TLB
  - This speeds program execution

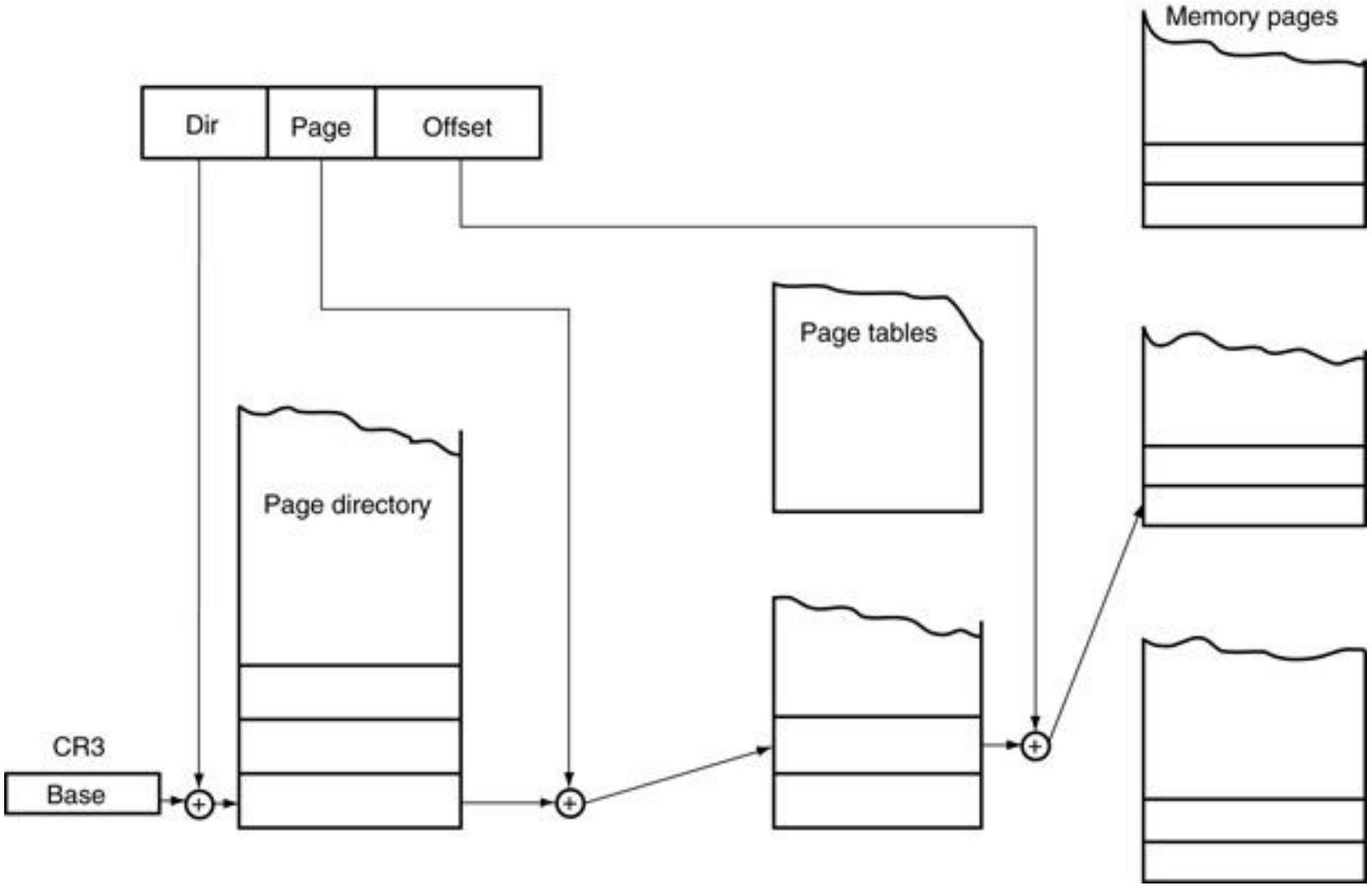
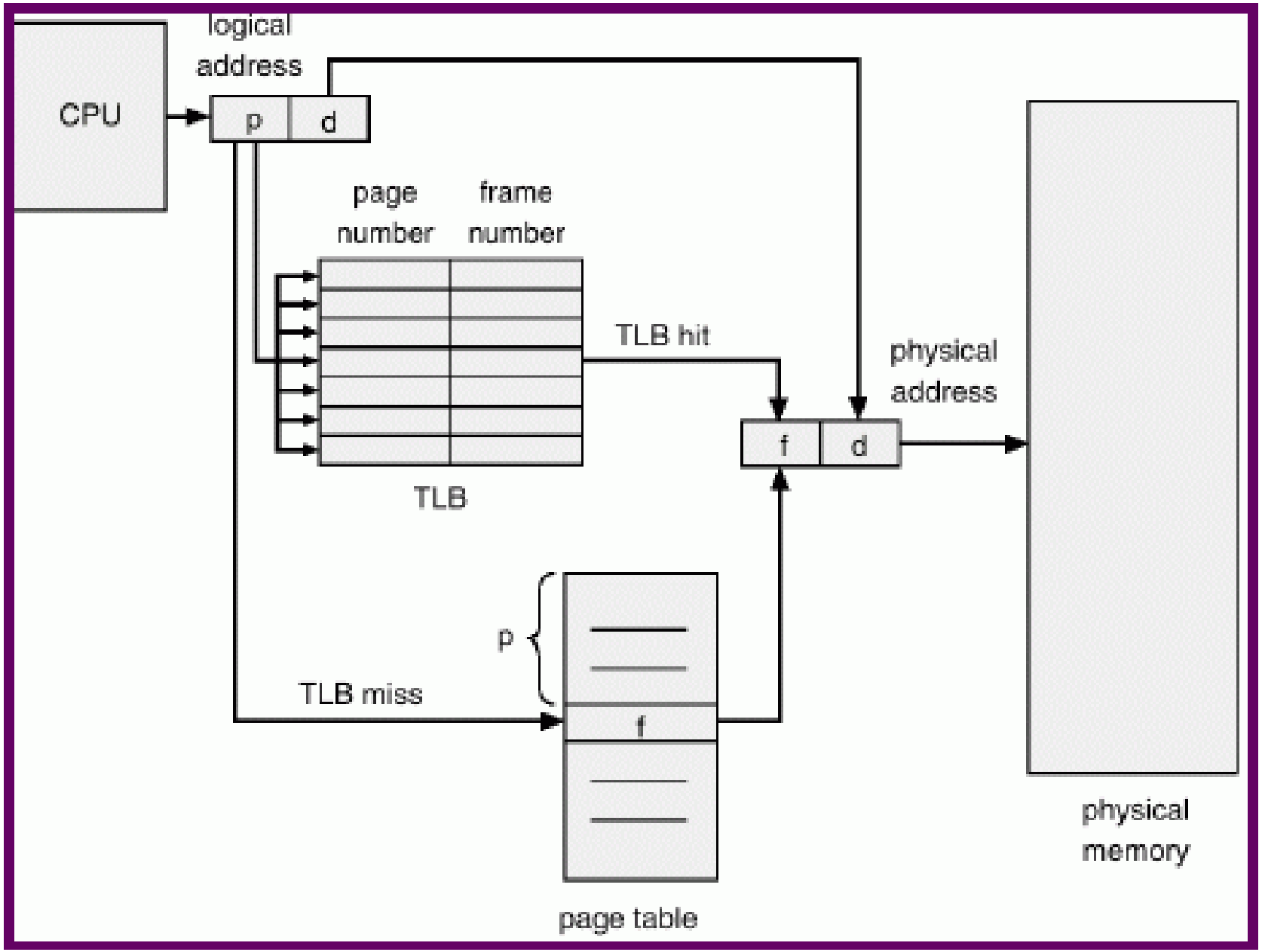


Figure 5: The paging mechanism in the 80386 through Core2 microprocessors.


CPU
logical address
p
d
page number
frame number
TLB hit
physical address
f
d
TLB
p
TLB miss
f
page table
physical memory