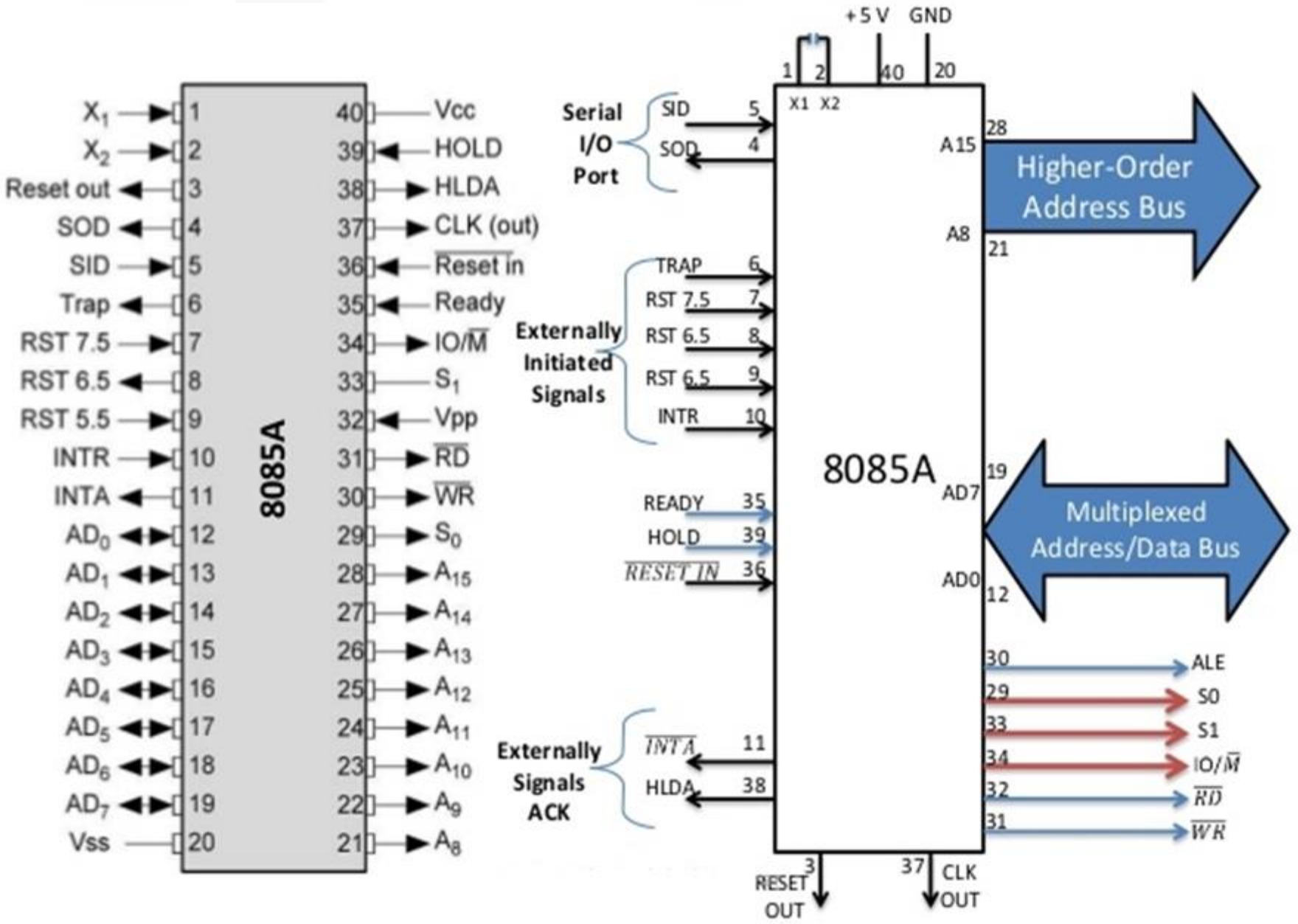
Unit 4

Microprocessor System

8085 PIN DESCRIPTION



8085 is 40 pin IC, DIP package

The total pin can be categorized to six groups:

I. Address Bus

II. Multiplexed Address/Data Bus

III. Control and status signal

IV. Power supply and clock signal

V. Interrupt and externally initiated signals

VI. Serial I/O ports

1. Address Bus

- **16 signal lines that are used as the address bus; however, these lines are split into two segments A_{15}-A_8 and AD_7-AD_0.**
- **A_{15}-A_8 are unidirectional and carries higher order address and the lower order AD_7-AD_0 are multiplexed and bidirectional.**

2. MULTIPLEXED ADDRESS/DATA BUS

- **8-bit data bus.**
- **Multiplexed bidirectional AD_7-AD_0 .**
- **These multiplexed lines are de-multiplexed to work as address bus and data bus separately using Address Latch Enable (ALE).**
- **If ALE=1, AD_7-AD_0 acts as address bus, otherwise it acts as data bus. By default, it acts as data bus.**

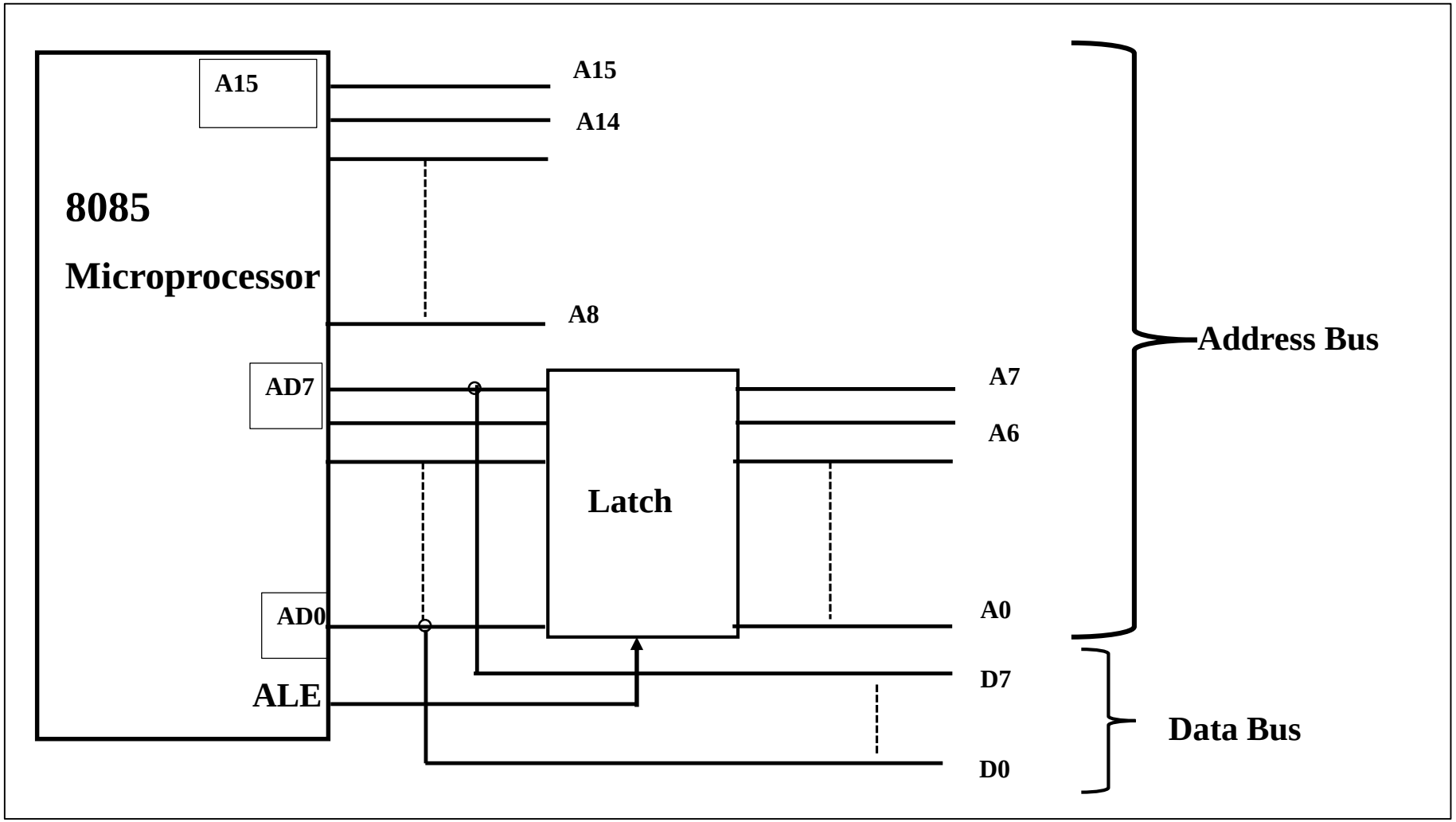


Fig: Time multiplexed address and data bus

3. CONTROL AND STATUS SIGNAL

- **This group of signals includes two control signals ($\overline{RD}$ and $\overline{WR}$).**
- **Three status signals (IO/$\overline{M}$, S_1, S_0) to identify the nature of the operation, one special signal (ALE) to indicate the beginning of operation.**

IO/M'	S_1	S_0	Operation
Z	0	0	HALT
0	0	1	Memory Write
0	1	0	Memory Read
1	0	1	I/O Write
1	1	0	I/O Read
0	1	1	Opcode Fetch

4. Power supply and clock signal

- **VCC: +5V power supply.**
- **VSS: Ground reference.**
- **X_1, X_2: A crystal (or RC, LC network) is connected at these two pins. The frequency is initially divided by 2; there for to operate a system at 3 MHz, the crystal should have frequency of 6 MHz**
- **CLK-clock output: This signal can be as a system clock for other devices.**

5. Interrupt and externally initiated signals

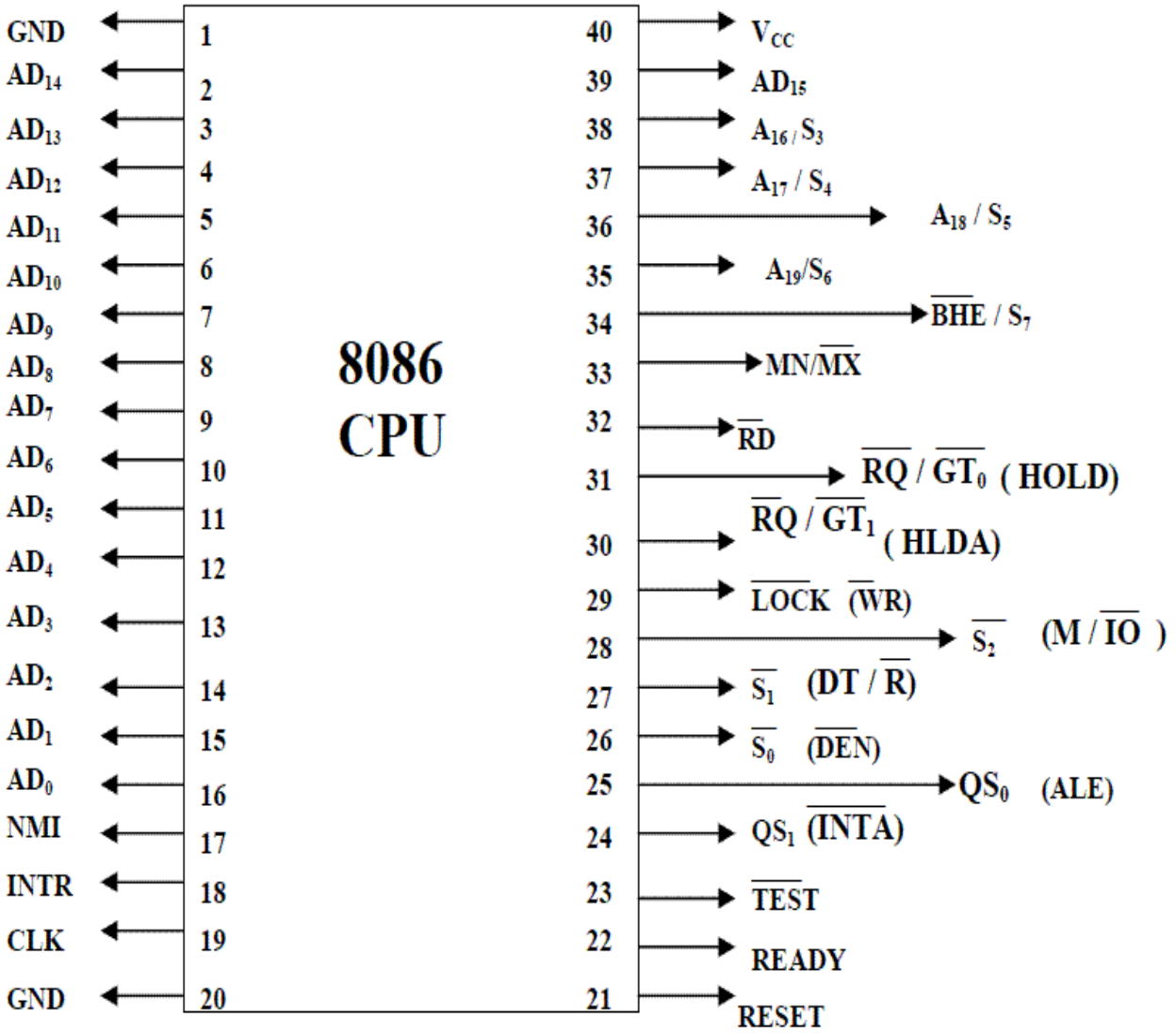
- **The 8085 has 5 interrupt signals that can be used to interrupt a program execution.**
  - **I. INTR (input)**
  - ***II.*** **$\overline{\text{INTA}}$ (output)**
  - **III. RST 7.5, 6.5, 5.5 (inputs)**
  - **IV. TRAP (input)**
  - **V. HOLD (input)**
  - **VI. HLDA (output)**
  - **VII. READY (Input)**
  - **VIII. $\overline{\text{RESETIN}}$**
  - **IX. RESET OUT**

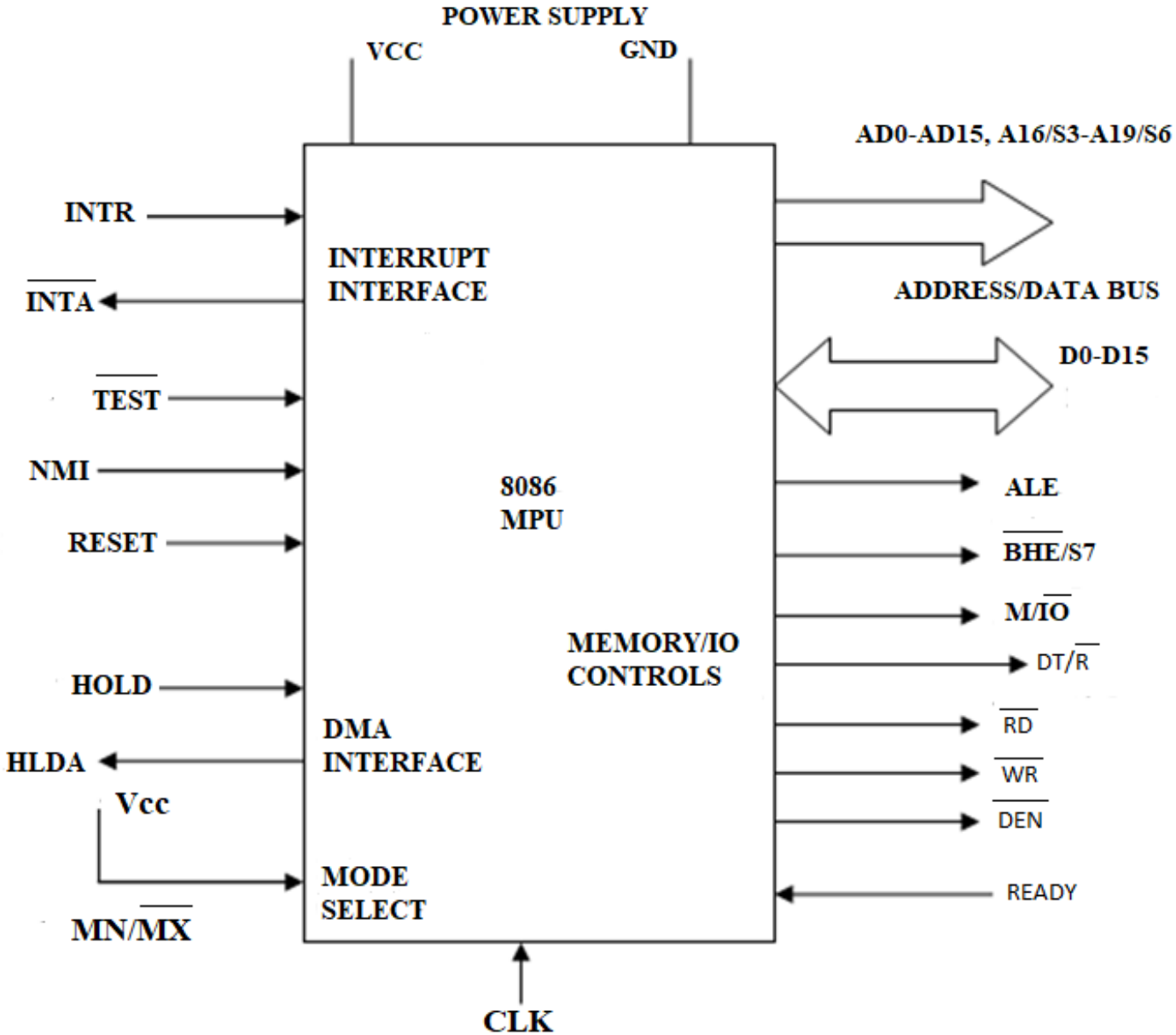
6. Serial I/O ports

- **Two signals to implement the serial transmission: SID (Serial Input Data) and SOD (Serial Output Data).**
- **In serial transmission, data bits are sent over a single line, one bit at a time, such as the transmission over telephone lines.**

Pin configuration of 8086

Pin Diagram of 8086





Signal Groups of 8086

8086 Pin Details

1. **Power supply and frequency signals**
   - It uses 5V DC supply at V_{CC} pin 40, and uses ground at V_{SS} pin 1 and 20 for its operation.
2. **Clock signal**
   - Clock signal is provided through Pin-19. It provides timing to the processor for operations. Its frequency is different for different versions, i.e. 5MHz, 8MHz and 10MHz.
3. **Address/data bus**
   - AD0-AD15. These are 16 address/data bus.
   - AD0-AD7 carries low order byte data and AD8-AD15 carries higher order byte data.
   - During the first clock cycle, it carries 16-bit address and after that it carries 16-bit data.

4. Address/status bus

- A16-A19/S3-S6.
- These are the 4 address/status buses.
- During the first clock cycle, it carries 4-bit address and later it carries status signals.

5. S7/BHE

- BHE stands for Bus High Enable.
- It is available at pin 34 and used to indicate the transfer of data using data bus D8-D15.
- This signal is low during the first clock cycle, thereafter it is active.

6. Read($\overline{RD}$)

- It is available at pin 32 and is used to read signal for Read operation.

7. Ready

- It is available at pin 22.
- It is an acknowledgement signal from I/O devices that data is transferred.
- It is an active high signal. When it is high, it indicates that the device is ready to transfer data. When it is low, it indicates wait state.

8. RESET

- It is available at pin 21 and is used to restart the execution.
- It causes the processor to immediately terminate its present activity. This signal is active high for the first 4 clock cycles to RESET the microprocessor.

9. INTR

- It is available at pin 18.
- It is an interrupt request signal, which is sampled during the last clock cycle of each instruction to determine if the processor considered this as an interrupt or not.

10. NMI

- It stands for non-maskable interrupt and is available at pin 17.
- It is an edge triggered input, which causes an interrupt request to the microprocessor.

11. $\overline{\boldsymbol{TEST}}$

- This signal is like wait state and is available at pin 23.
- When this signal is high, then the processor has to wait for IDLE state, else the execution continues.

12. MN/$\overline{\boldsymbol{MX}}$

- It stands for Minimum/Maximum and is available at pin 33.
- It indicates what mode the processor is to operate in; when it is high, it works in the minimum mode and vice-versa.

Max mode operation pins

13. INTA

- It is an interrupt acknowledgement signal and id available at pin 24.
- When the microprocessor receives this signal, it acknowledges the interrupt.

14. ALE

- It stands for address enable latch and is available at pin 25.
- A positive pulse is generated each time the processor begins any operation. This signal indicates the availability of a valid address on the address/data lines.

15. DEN

- It stands for Data Enable and is available at pin 26.
- It is used to enable Trans-receiver 8286. The trans-receiver is a device used to separate data from the address/data bus.

16. DT/R

- It stands for Data Transmit/Receive signal and is available at pin 27.
- It decides the direction of data flow through the transreceiver. When it is high, data is transmitted out and vice-a-versa.

17. M/$\overline{IO}$

- This signal is used to distinguish between memory and I/O operations.
- When it is high, it indicates memory operation and when it is low indicates the IO operation. It is available at pin 28.

18. WR

- It stands for write signal and is available at pin 29. It is used to write the data into the memory or the output device depending on the status of M/IO signal.

19. HLDA

- It stands for Hold Acknowledgement signal and is available at pin 30.
- This signal acknowledges the HOLD signal.

20. HOLD

- This signal indicates to the processor that external devices are requesting to access the address/data buses.
- It is available at pin 31.

21. QS_1 and QS_0

- These are queue status signals and are available at pin 24 and 25.
- These signals provide the status of instruction queue. Their conditions are shown in the following table −

QS0	QS1	Status
0	0	No operation
0	1	First byte of opcode from the queue
1	0	Empty the queue
1	1	Subsequent byte from the queue

Max mode operation pins

S_0, S_1, S_2

These are the status signals that provide the status of operation, which is used by the Bus Controller 8288 to generate memory & I/O control signals. These are available at pin 26, 27, and 28. Following is the table showing their status −

S2	S1	S0	Status
0	0	0	Interrupt acknowledgement
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

22. LOCK

- When this signal is active, it indicates to the other processors not to ask the CPU to leave the system bus.
- It is activated using the LOCK prefix on any instruction and is available at pin 29.

23. RQ/GT_1 and RQ/GT_0

- These are the Request/Grant signals used by the other processors requesting the CPU to release the system bus.
- When the signal is received by CPU, then it sends acknowledgment. RQ/GT_0 has a higher priority than RQ/GT_1.

BUS STRUCTURE:

- **Microprocessor** uses ***3-types*** of buses to communicate between CPU, memory and IO units:
  1. ***Data Bus***
  2. ***Address Bus***
  3. ***Control Bus***
- ***Communication uses different mechanisms:***
  1. ***Transfer Acknowledge:*** This signal indicates that data have been accepted from or placed on the bus.
  2. ***Bus Request:*** It is used to indicate that a module wants to gain control of the bus.
  3. ***Bus Grant:*** It indicates that a requesting module has been granted for the control of bus.
  4. ***Interrupt Request:*** It indicates that an interrupt has been pending**.**
  5. ***Interrupt Acknowledge:*** it indicates that the pending interrupt has been recognized.

Bus Types:
Two types; synchronous and asynchronous

1. Synchronous bus:

- Transmitter and receivers are synchronized of clock.
- Data bits are transmitted with synchronization of clock.
- Character is received at constant Rate.
- Data transfer takes place in block.
- Start and stop bit are required to establish communication of each character.
- Used in high – speed transmission.

Advantages:

- Involves very little logic and can run very fast

Disadvantages:

- Every device on the bus must ran at the same clock rate. Clock skew limits bus length.
- To avoid clock skew, they cannot be long if they are fast

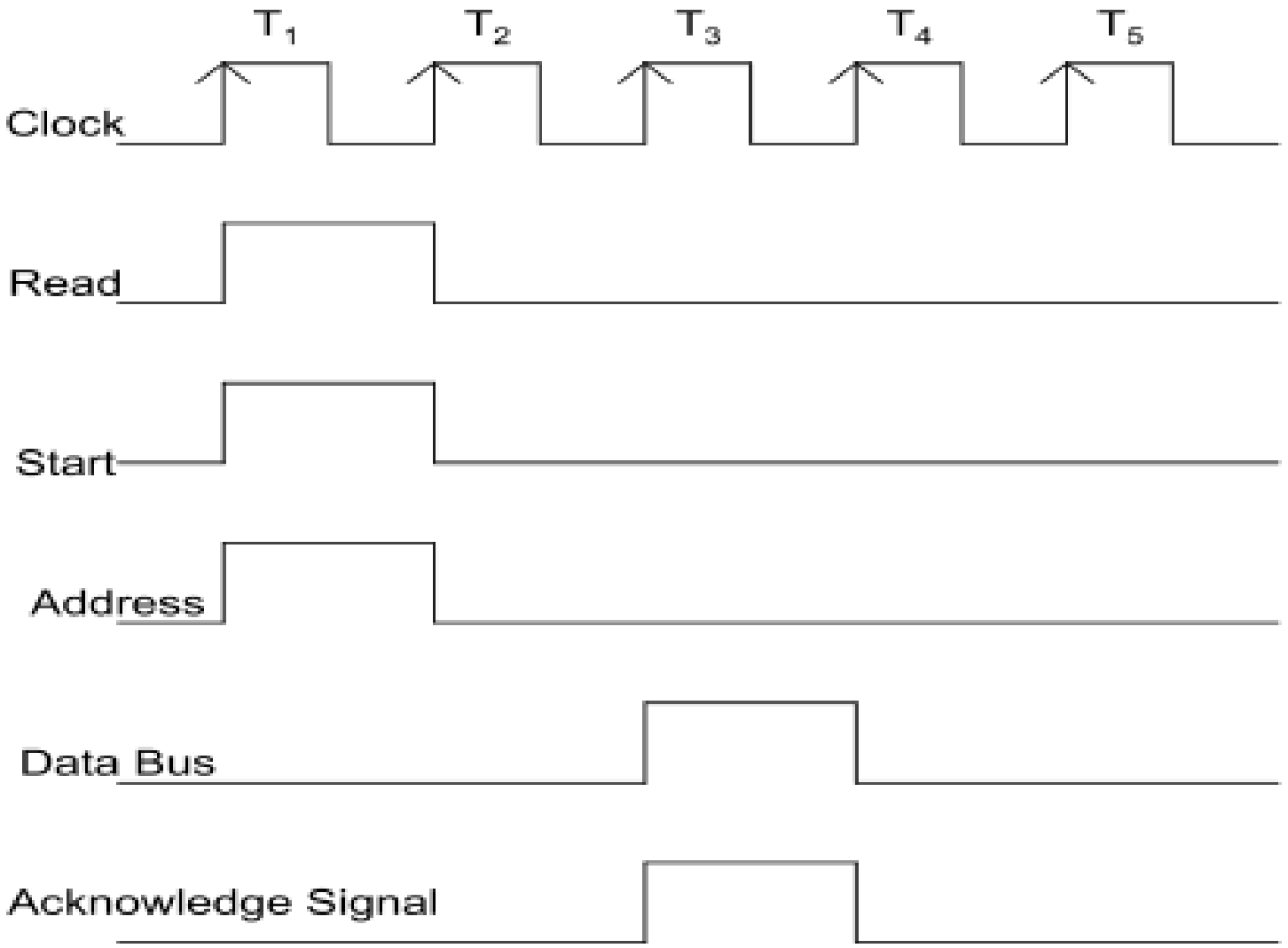


Fig: Synchronous read operation

2. *Asynchronous bus*

- Transmitters and receivers are not synchronized by clock.
- Bit's of data are transmitted at constant rate.
- Character may arrive at any rate at receiver.
- Data transfer is character oriented.
- Start and stop bits are required to establish communication of each character.
- Used in low – speed transmission.

- ***Advantages:***
  - Allow a device to send or received data payloads or various size's data.
  - It is faster than synchronous bus because it doesn't have to wait the bus cycle.

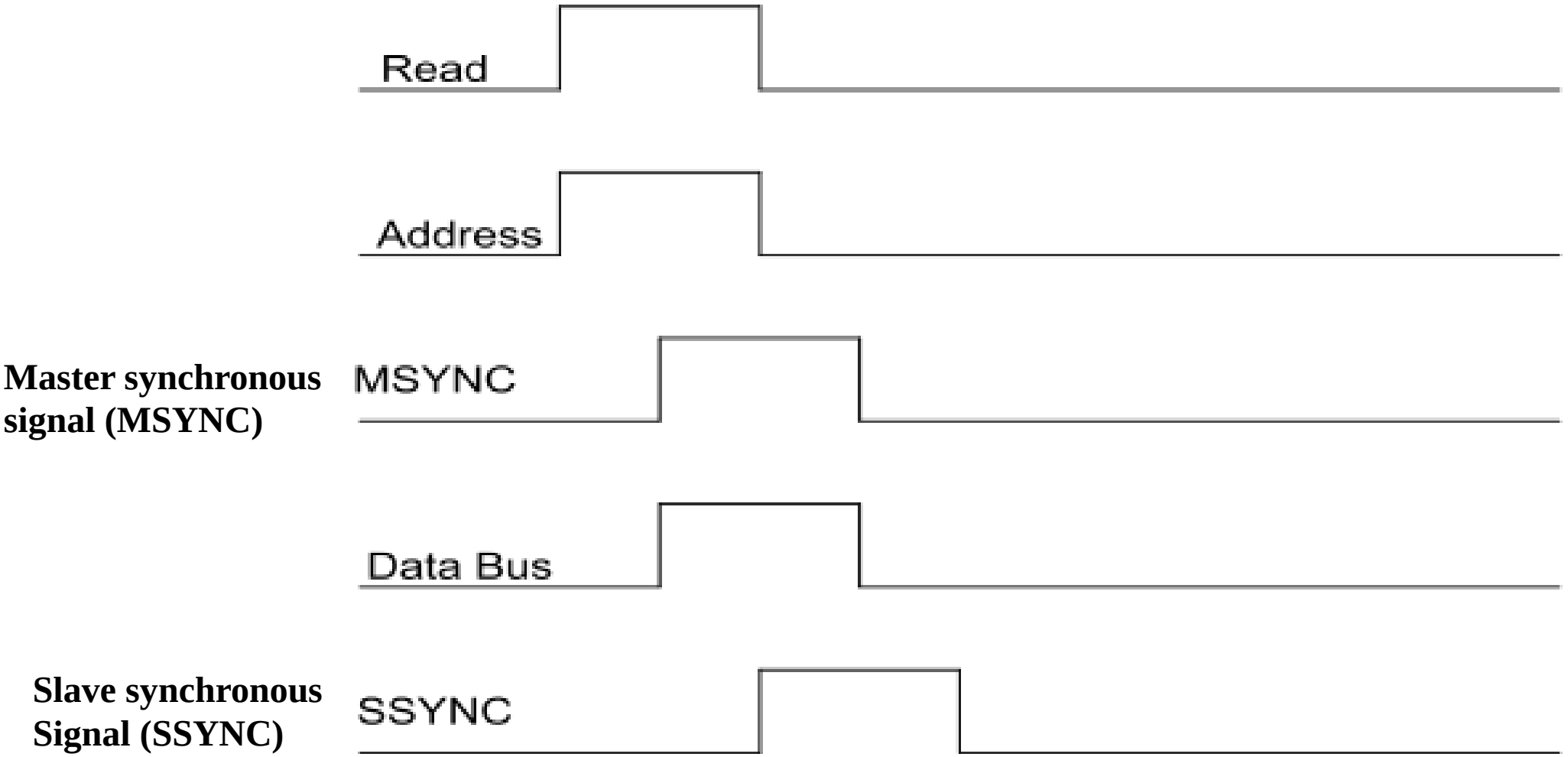


Fig: Asynchronous read operation

Machine cycles and bus timing diagrams:

- Microprocessor operations can be classified into:
  i. Op-Code fetch
  ii. Memory Read/Write
  iii. I/O Read/Write
  iv. Request acknowledgment
- Here, Op-Code fetch is an internal operation and other three are external operations.
- During three operations, microprocessor generates and receives different signals. These all operations are terms as machine cycle.

T-State:

- It is the time period of a single cycle of the clock frequency.
- It is the basic unit used to calculate the time taken for execution the instruction and program in a processor.
- T=1/f; where T is time and f is frequency.

Machine Cycle:

- The time period (number of T-states) required by microprocessor to perform a read or a write operation either from memory or I/O device.
- In machine cycle various operations like op-code fetch, memory read, memory write, I/O read, I/O write are performed.
- A machine cycle may consist of three to six T-states.

Instruction Cycle:

- It is the total number of machine cycles required to execute a complete instruction i.e. Fetching and execution of one instruction. The fetch and execute cycles are carried out in synchronization with the clock.

Machine Cycles of 8085 microprocessor:

The 8085 microprocessor has 5 machine cycles. They are:

1. Opcode fetch cycle (4T)
2. Memory read/write cycle (3T)
3. I/O read/write cycle (3T)
4. Interrupt

1. Op-code fetch cycle:

- Each instruction of the processor has one-byte op-code.
- The microprocessor uses this cycle to take the op-code of an instruction from the memory location to processor.
- The op-code is taken from memory and transferred to instruction register for decoding and execution. Hence, every instruction starts with op-code fetch machine cycle.
- The time required to complete this cycle is 4 to 6 T-states. In this time, the first, 3 T-states are used for fetching the op-code from memory and the remaining T-states are used for internal operations by the processor.

2. Memory read cycle:

- The microprocessor executes these cycles to read data from memory. The address of memory location is given by instruction.
- The time required to complete the memory read cycle is 3 T-states.

3. Memory write cycle:

- The microprocessor executes these cycles to write data to memory. The address of memory is given by instructions.
- The time required to complete the memory write cycle is 3 T-states.

4. I/O read cycle:

- The microprocessor executes these cycles to read data from I/O devices.
- The address of I/O port is given by instruction.
- The time required to complete the I/O read cycle is 3 T-states.

5. I/O write cycle:

- The microprocessor executes these cycles to write data into I/O devices.
- The address of I/O port is given by instruction.
- The time required to complete the I/O write cycle is 3 T-states.

6. Interrupt acknowledge cycle:

- In the response to interrupt request input **INTR**, the microprocessor executes these cycles to get information from the interrupting devices.
- The time required to complete this cycle is 3 T-states.

Fetch & Execute Operation: Timing Diagram:

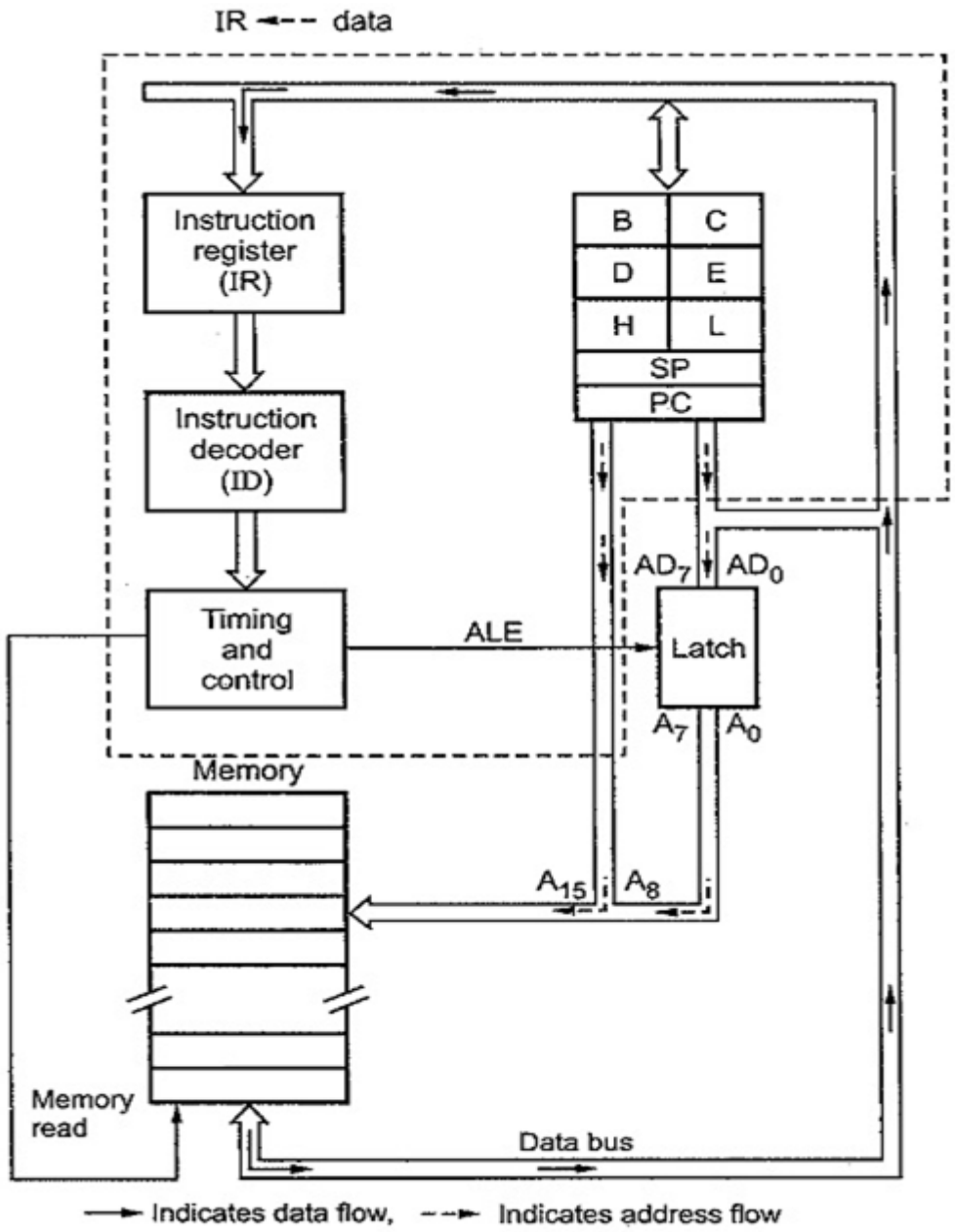
- The graphical representation of status of various signals involved during a machine cycle with respect to time is called timing diagram.
- This gives basic idea of what is happening in the system when the instruction is getting fetched and executed, at what instant which signal is getting activated.
- The signals involved during machine cycle are CLK, A15 – A8, AD7 – AD0, IO/ $\overline{M}$, **$\overline{Rd}$, $\overline{WR}$** and **S1, S0**.

IO/ $\overline{M}$	S 1	S0	Operation
0	0	0	Halt
0	0	1	Memory write
0	1	0	Memory read
0	1	1	Op-code fetch
1	0	1	IO write
1	1	0	IO read
1	1	1	Interrupt acknowledge

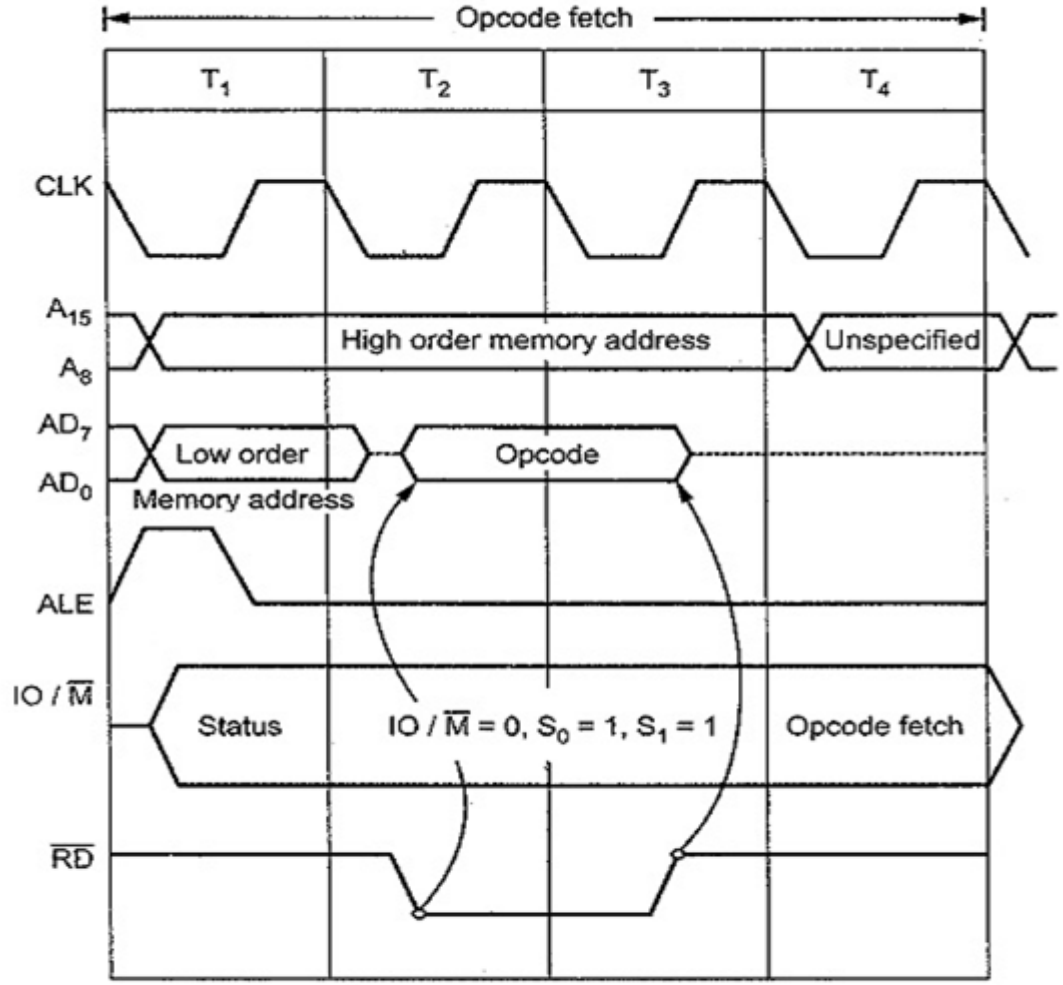
Timing diagram for op-code fetch cycle:

The op-code fetch timing diagram can be explained as below:

1) The microprocessor places the 16-bit memory address from the program counter on address bus. At time period T1, the higher order memory address is placed on the address lines A15 – A8. At the same time ALE is high, the lower address is placed on the bus AD7 – AD0. The status signal IO/ $\overline{M}$ goes low indicating the memory operation and two status signals S1 = 1, S0 = 1 to indicate op-code fetch operation.
2) At time period T2, the microprocessor sends **Rd**(bar) control line to enable the memory read. When memory is enabled with $\overline{\textbf{Rd}}$ signal, the op-code value from the addressed memory location is placed on the data bus with ALE low.
3) The op-code value is reached at processor register during T3 time period. When data (op-code value) is arrived, the $\overline{\textbf{Rd}}$ signal goes high. It causes the bus to go into high impedance state.
4) The op-code byte is placed in instruction decoder of microprocessor and the op-code is decoded and executed. This happens during time period T4.

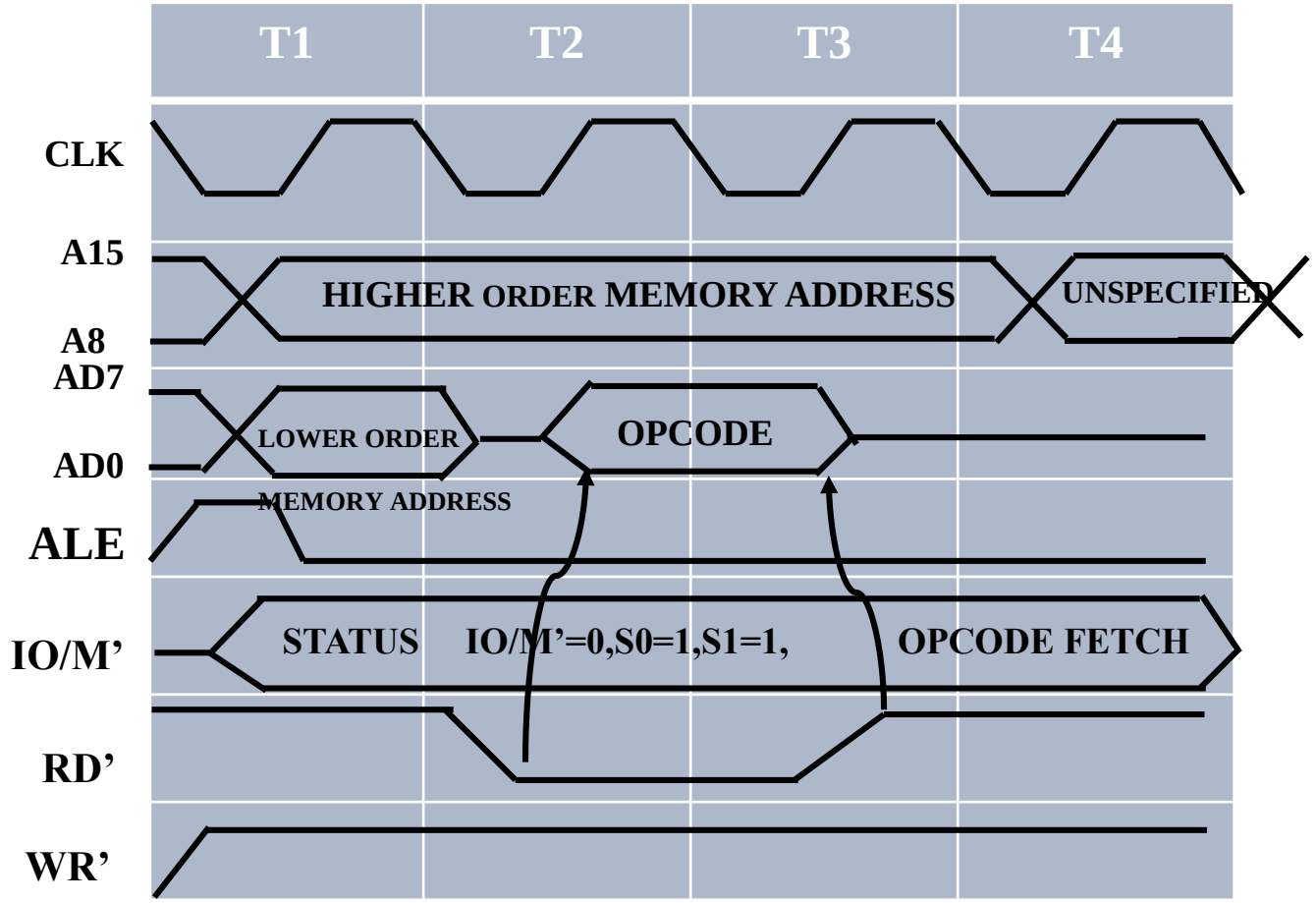


(a) Data (opcode) flow from memory to micrprocessor



(b) Opcode fetch machine cycle

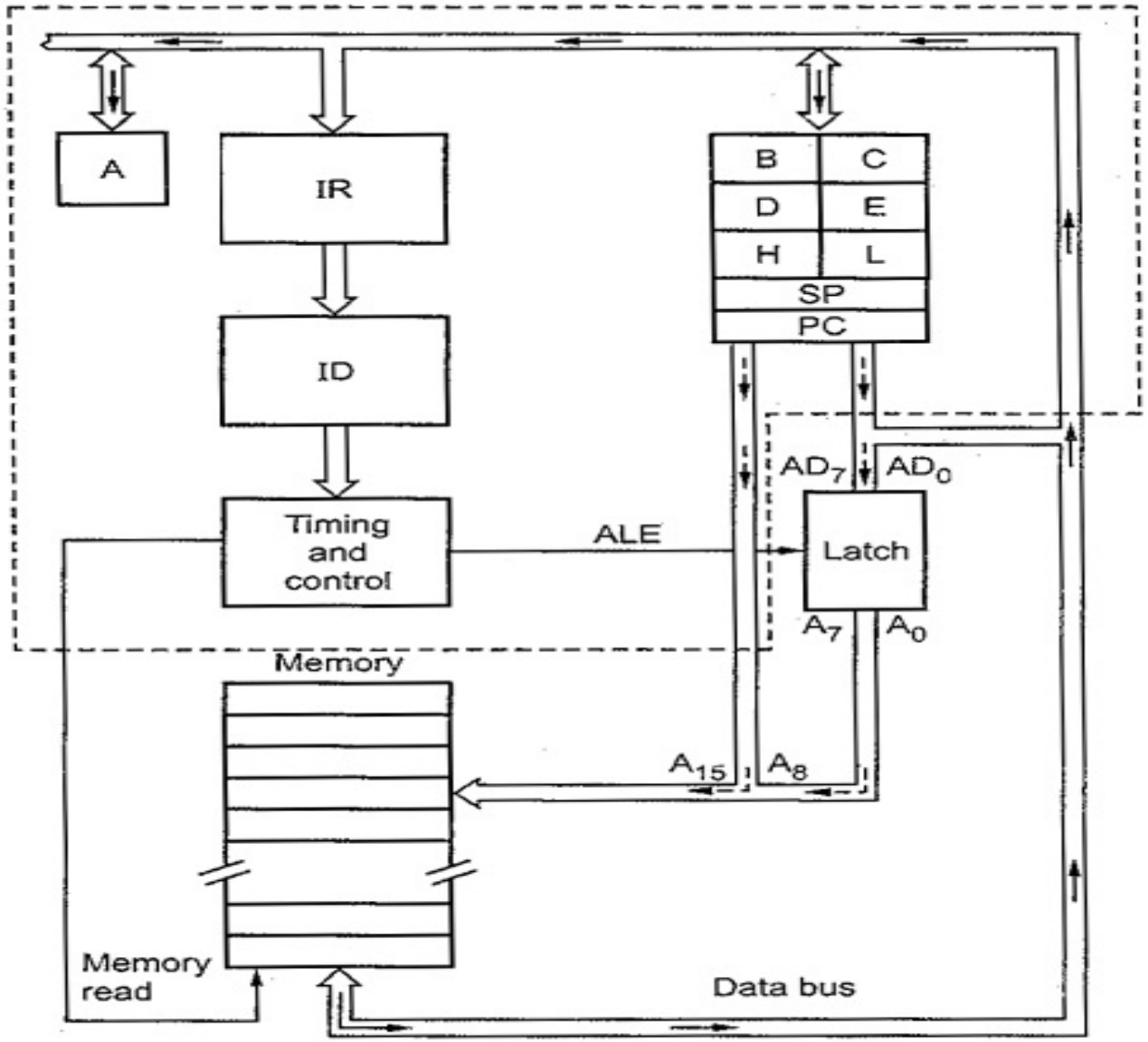
OPCODE FETCH CYCLE



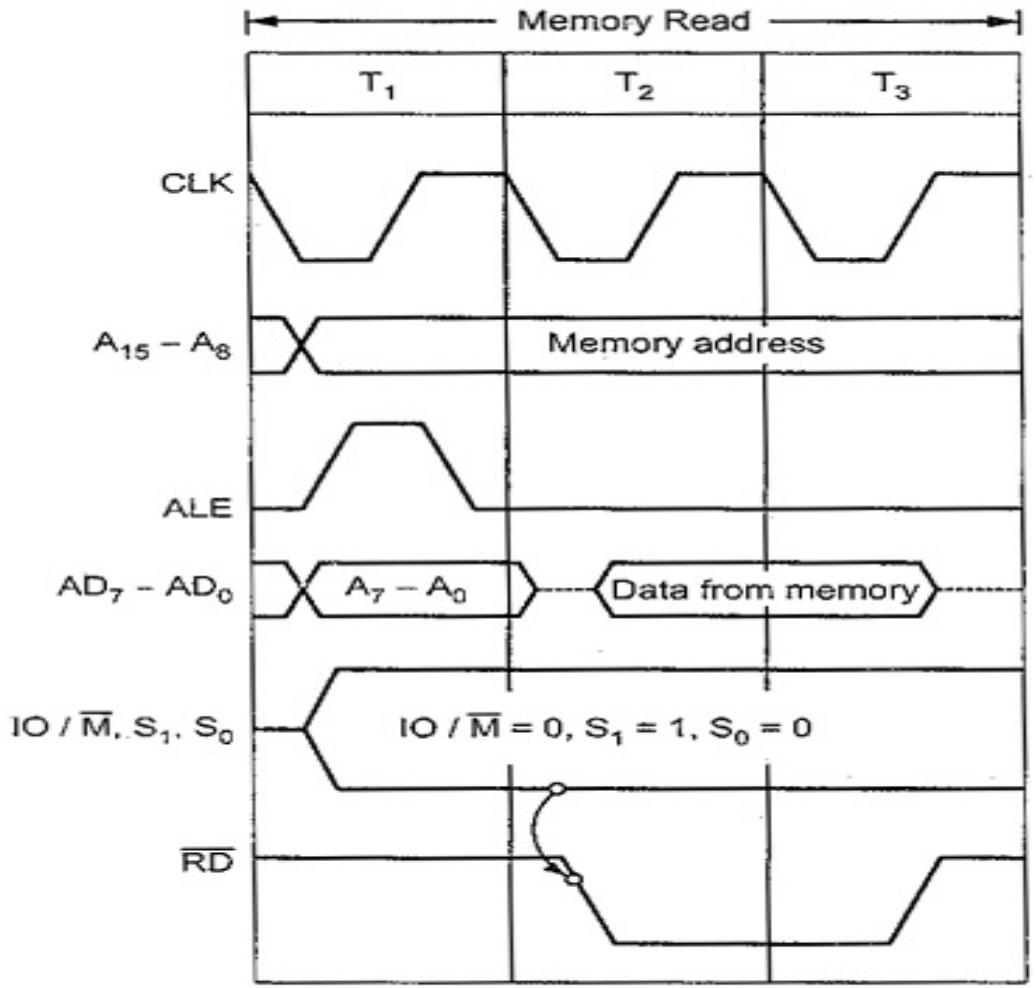
Timing diagram for memory read cycle:

The memory read timing diagram can be explained as below:

1) The microprocessor places the 16-bit memory address from the program counter on address bus. At time period T1, the higher order memory address is placed on the address lines A15 – A8. At the same time ALE is high, the lower address is placed on the bus AD7 – AD0. The status signal IO/ $\overline{M}$ goes low indicating the memory operation and two status signals S1 = 1, S0 = 0 to indicate memory read operation.
2) At time period T2, the microprocessor sends $\overline{\mathbf{RD}}$(bar) control line to enable the memory read. When memory is enabled with $\overline{\mathbf{RD}}$ signal, the data from the addressed memory location is placed on the data bus with ALE low.
3) The data is reached at processor register during T3 state. When data is arrived, the $\overline{\mathbf{RD}}$ signal goes high. It causes the bus to go into high impedance state.



(a) Data flow from memory to microprocessor



(b) Memory read machine cycle

Fig: Timing Diagram for Memory Read Machine Cycle

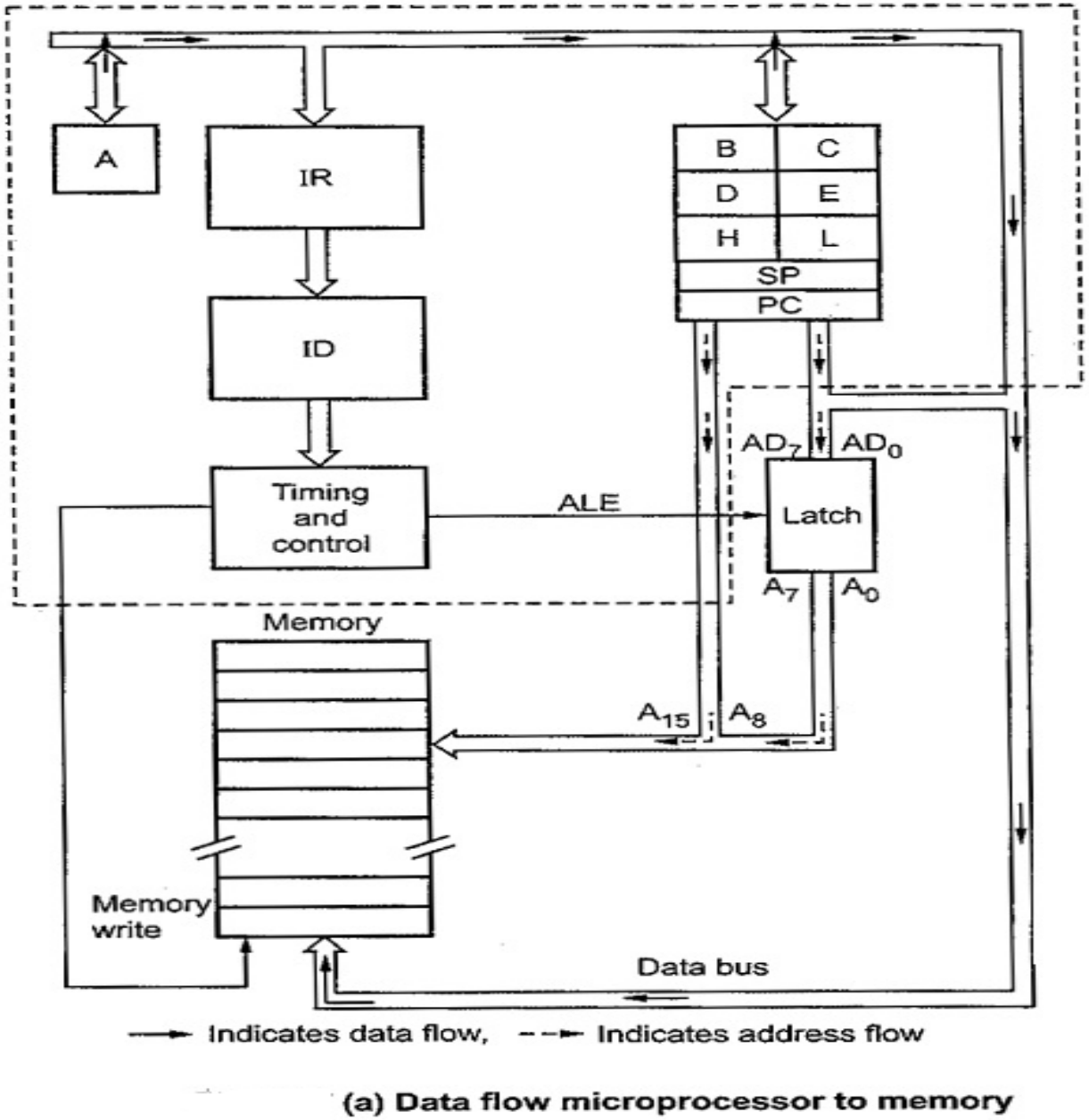
Timing diagram for memory write cycle:

The memory write timing diagram can be explained as below:

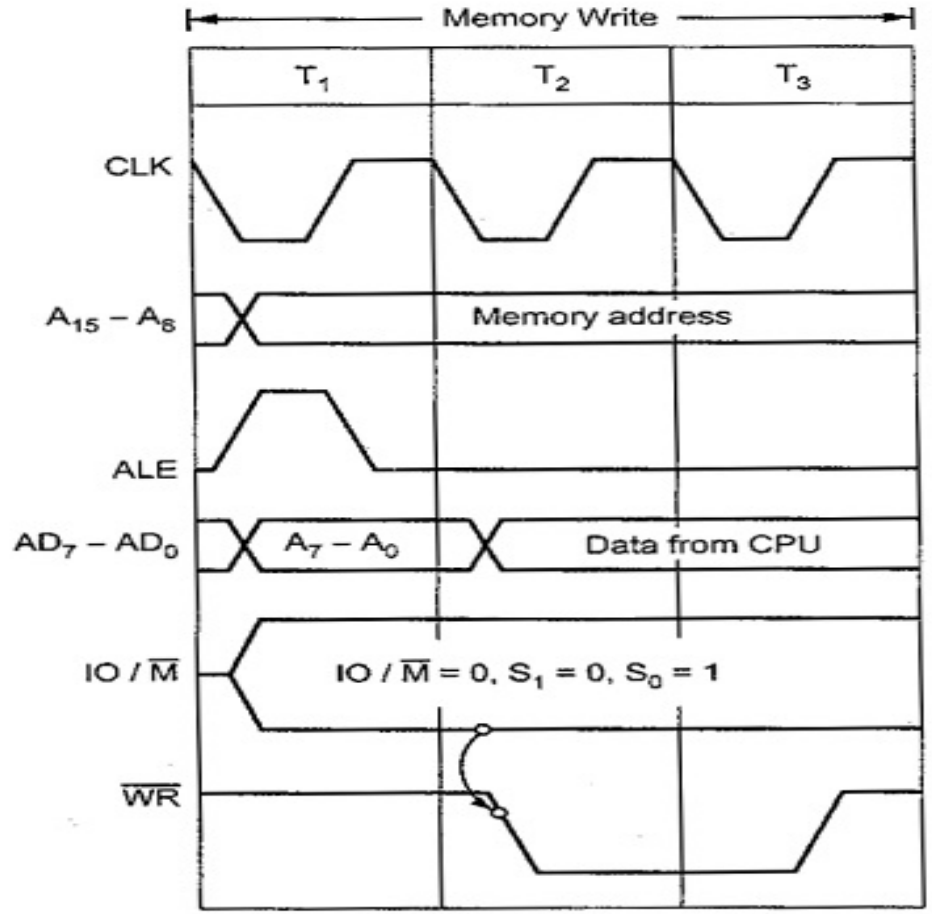
1) The microprocessor places the 16-bit memory address from the program counter on address bus. At time period T1, the higher order memory address is placed on the address lines A15 – A8. At the same time ALE is high, the lower address is placed on the bus AD7 – AD0. The status signal IO/ $\bar{M}$ goes low indicating the memory operation and two status signals S1 = 0, S0 = 1 to indicate memory write operation.

1) At time period T2, the microprocessor sends $\bar{W}\bar{R}$ control line to enable the memory write. When memory is enabled with $\bar{W}\bar{R}$ signal, the data from the processor is placed on the addressed location with ALE low.

1) The data is reached at memory location during T3 state. When data is reached, the $\bar{W}\bar{R}$ (bar) signal goes high. It causes the bus to go into high impedance state.



(a) Data flow microprocessor to memory



(b) Memory write machine cycle

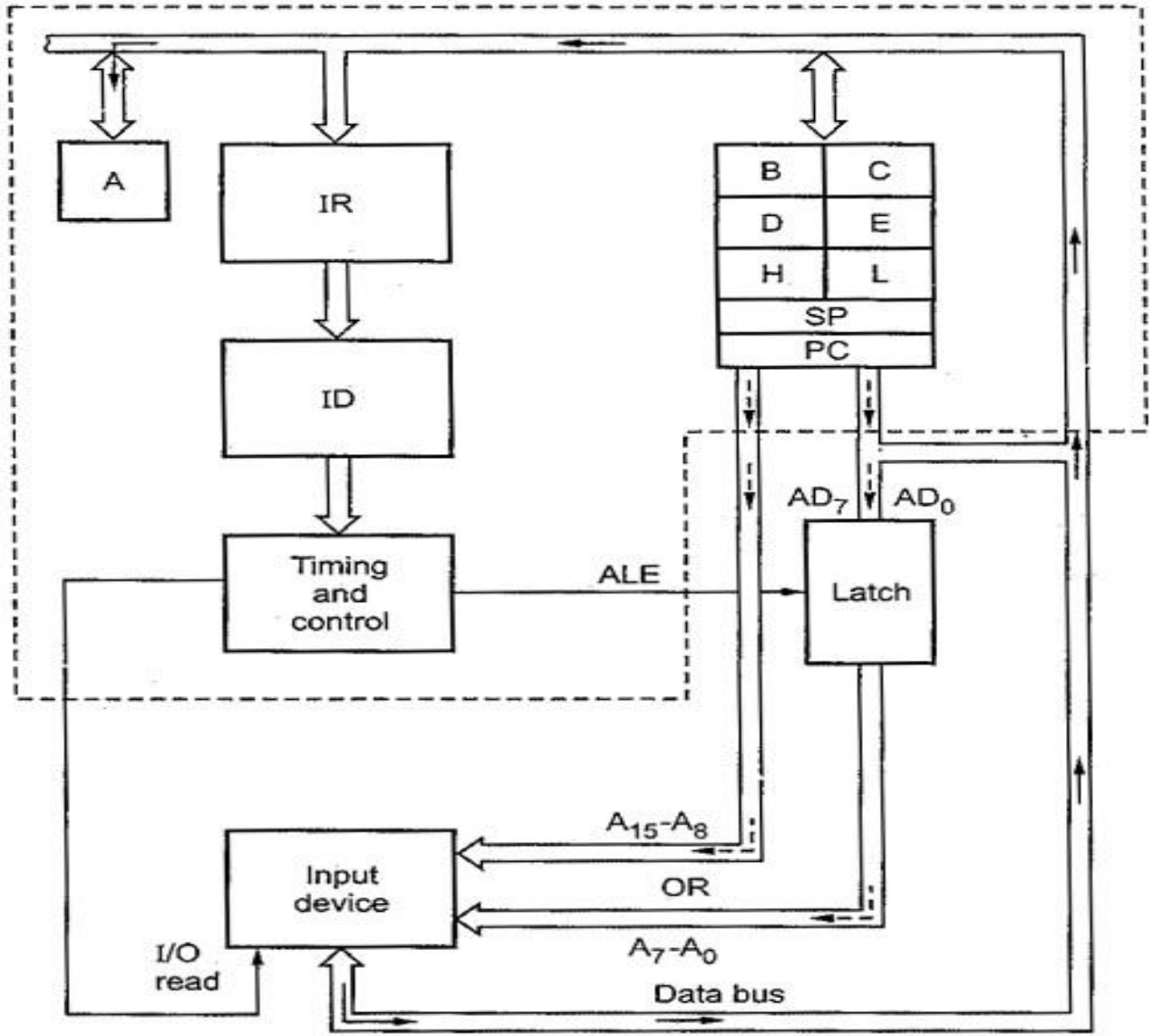
Fig: Timing Diagram for Memory Write Machine Cycle

Timing diagram for I/O read cycle:

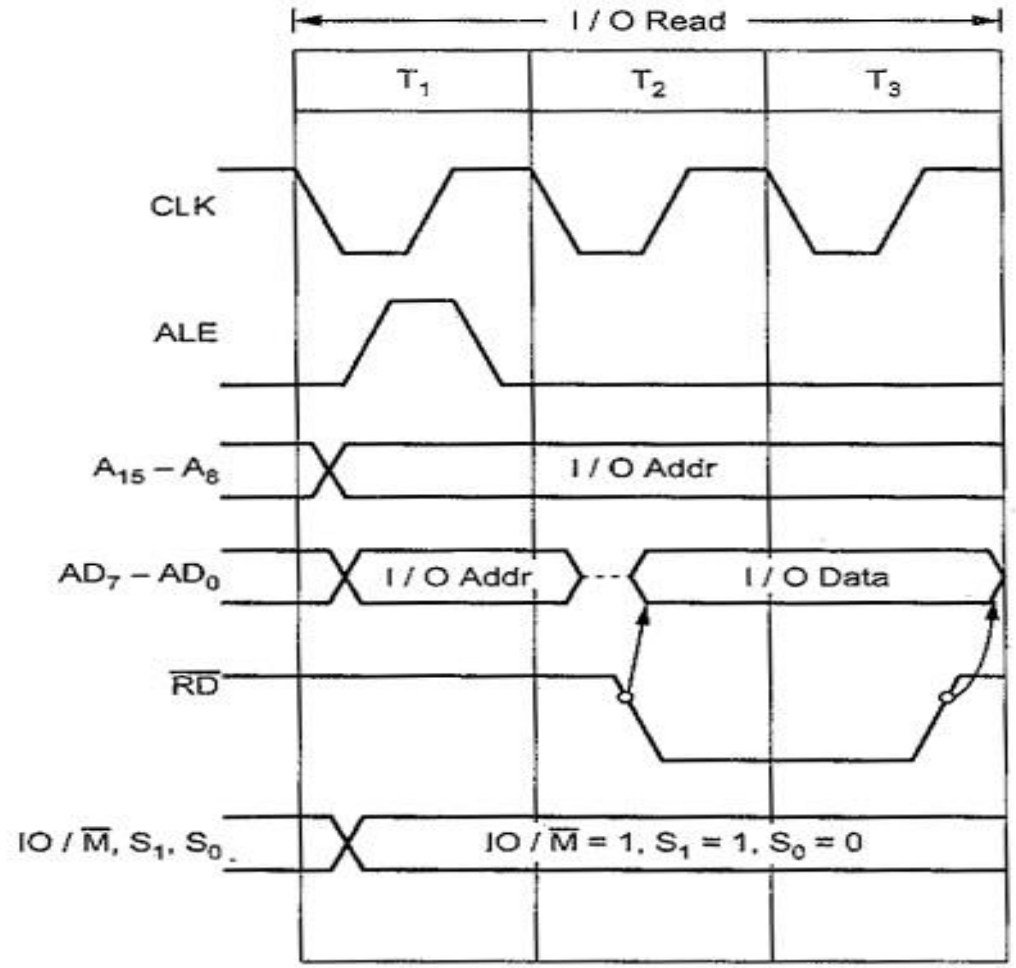
Operation:

It is used to fetch one byte from an IO port. It requires 3 T-States.

1) During T1, The Lower Byte of IO address is duplicated into higher order address bus A8-A15. ALE is high and AD0-AD7 contains address of IO device. IO/M (bar) goes high as it is an IO operation.
2) During T2, ALE goes low, RD (bar) goes low and data appears on AD0-AD7 as input from IO device.
3) During T3 Data remains on AD0-AD7 till RD(bar) is low.



(a) Data flow from input device to microprocessor



(b) I/O read memory cycle

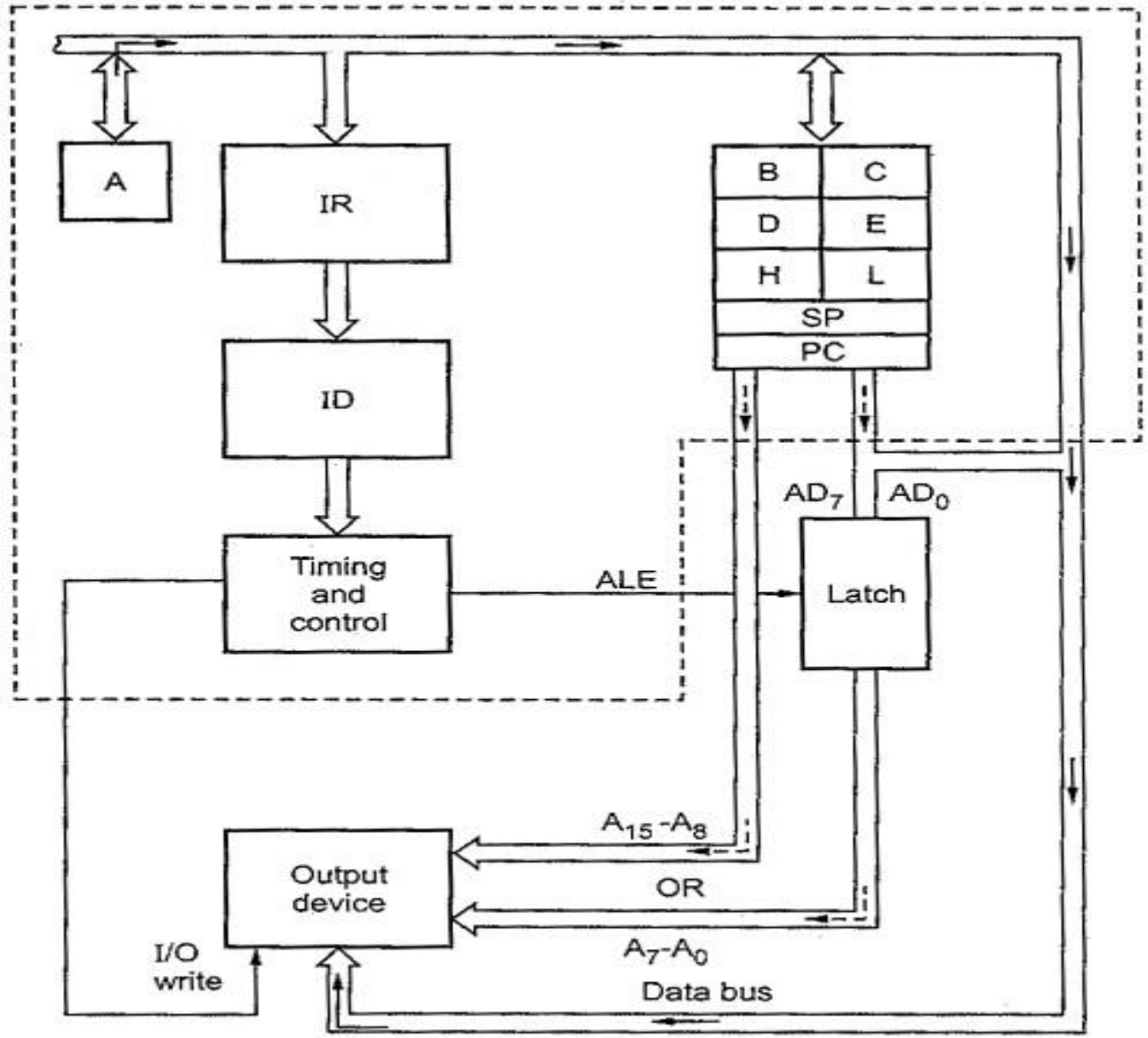
Fig: Timing Diagram for I/O Read Machine Cycle

Timing diagram for I/O write cycle:

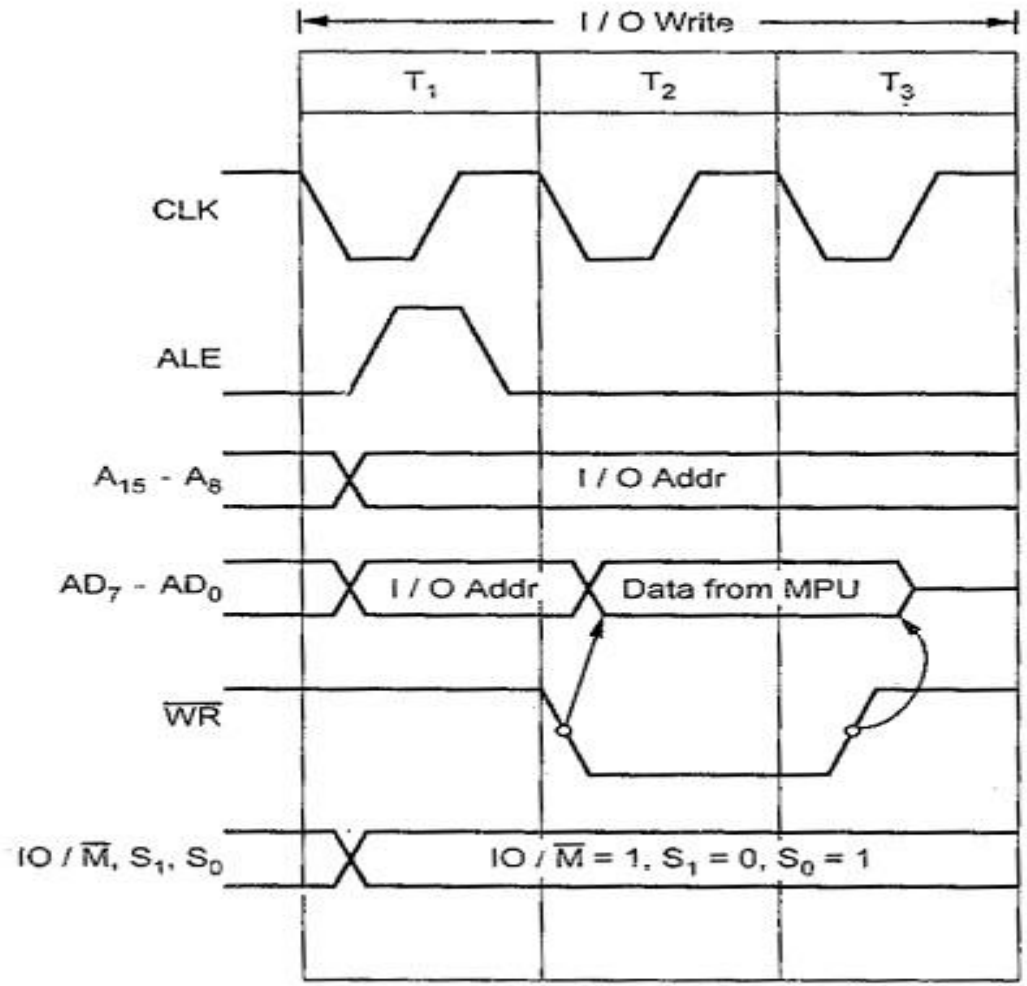
Operation:

It is used to writ one byte into IO device. It requires 3 T-States.

1) During T1, the lower byte of address is duplicated into higher order address bus A8-A15 and ALE is high, the A0-A7 address is selected from AD0-AD7. As it is an IO operation IO/M (bar) goes high.
2) During T2, ALE goes low, WR (bar) goes low and data appears on AD0-AD7 to write data into IO device.
3) During T3, Data remains on AD0-AD7 till WR(bar) is low.



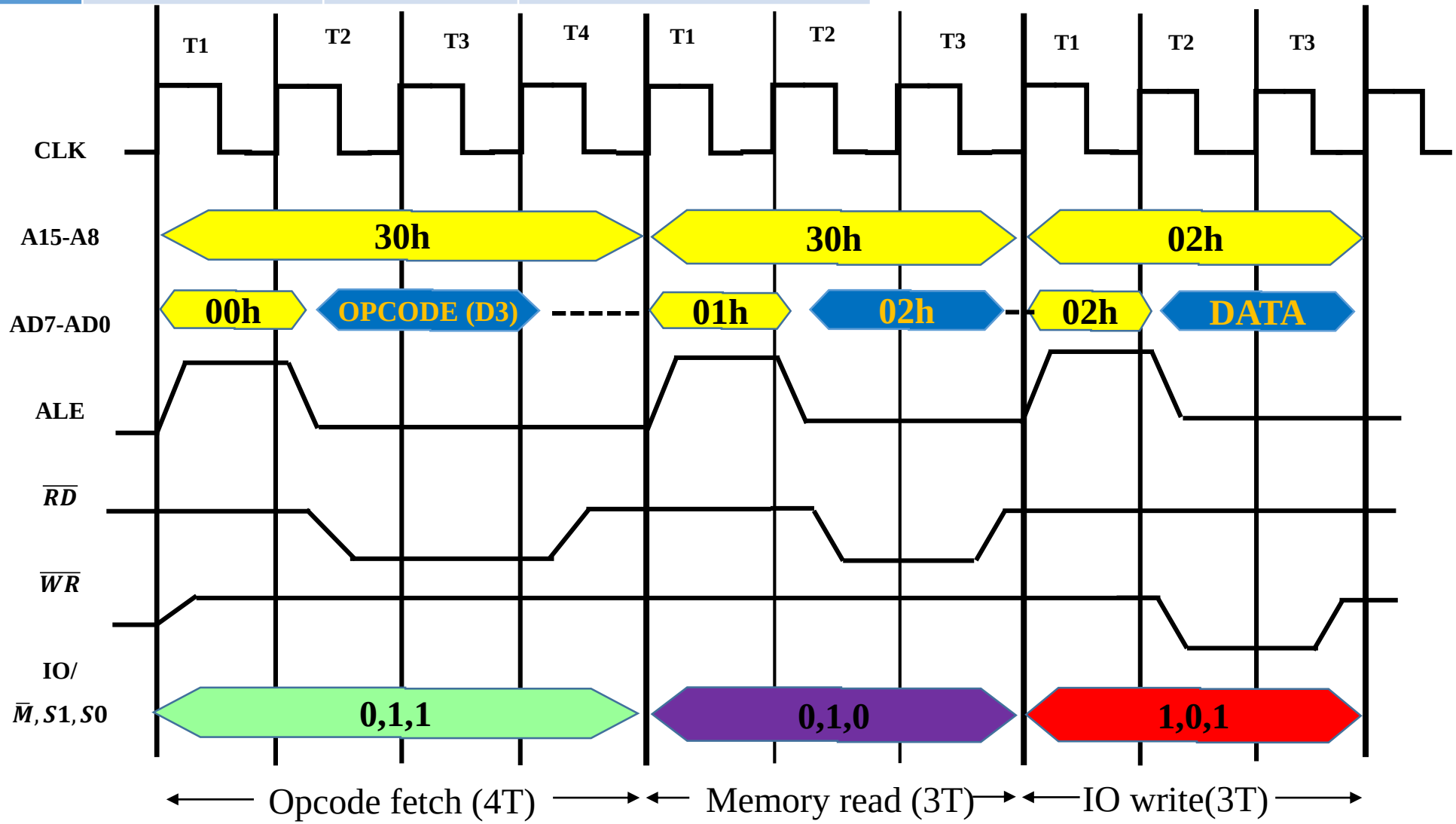
(a) Data flow from microprocessor to output device



(b) I/O write machine cycle

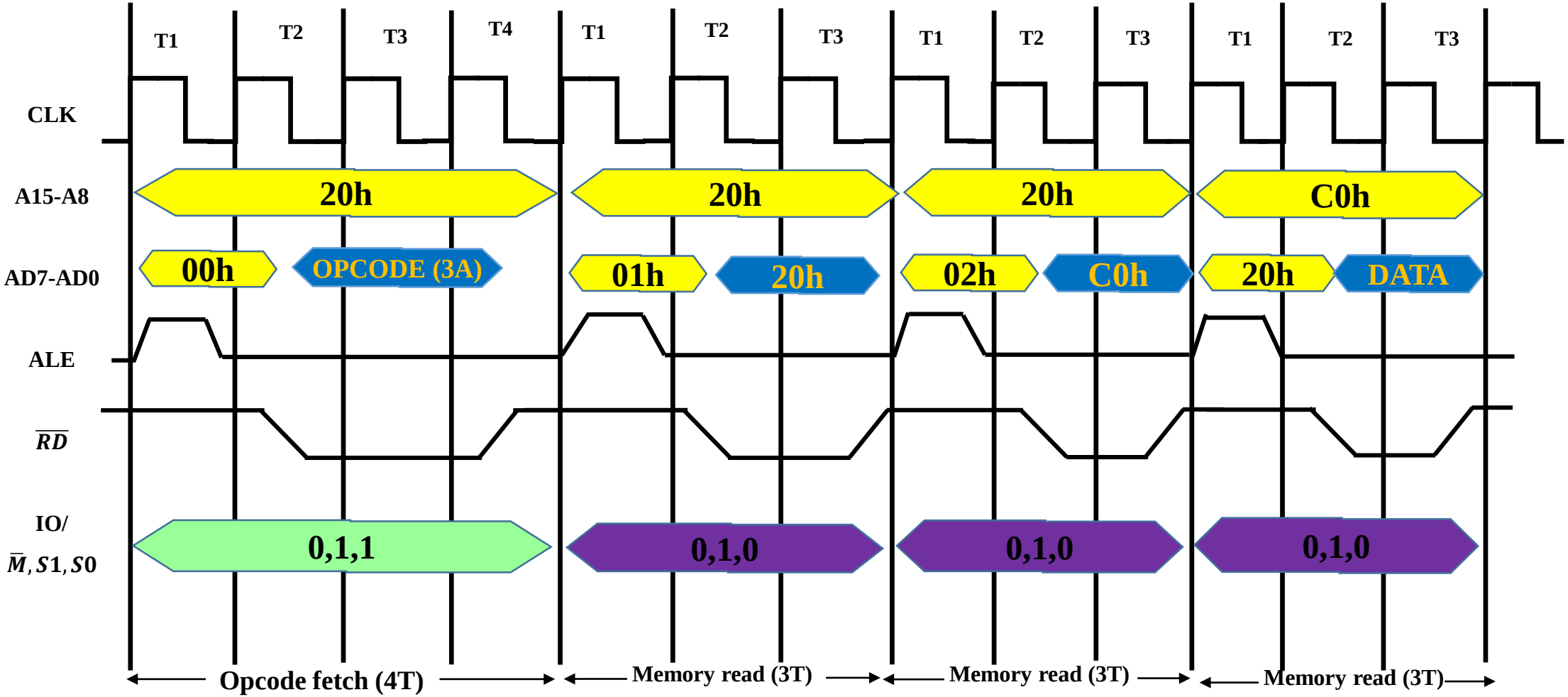
Fig: Timing Diagram for I/O Write Machine Cycle

Base address	Mnemonics	Hex code	
3000h	Out 02h	D3h	Opcode fetch (4T)
3001h		02h	IO read (3T) (write(3T)
			Total t-cycle=10T



BASE ADD.	MNEMONICS	HEX VALUE	T-CYCLE
2000H	LDA C020H	3A	4T
2001H		20	3T
2002H		C0	3T (DATA READ 3T)
		TOTAL=	13T

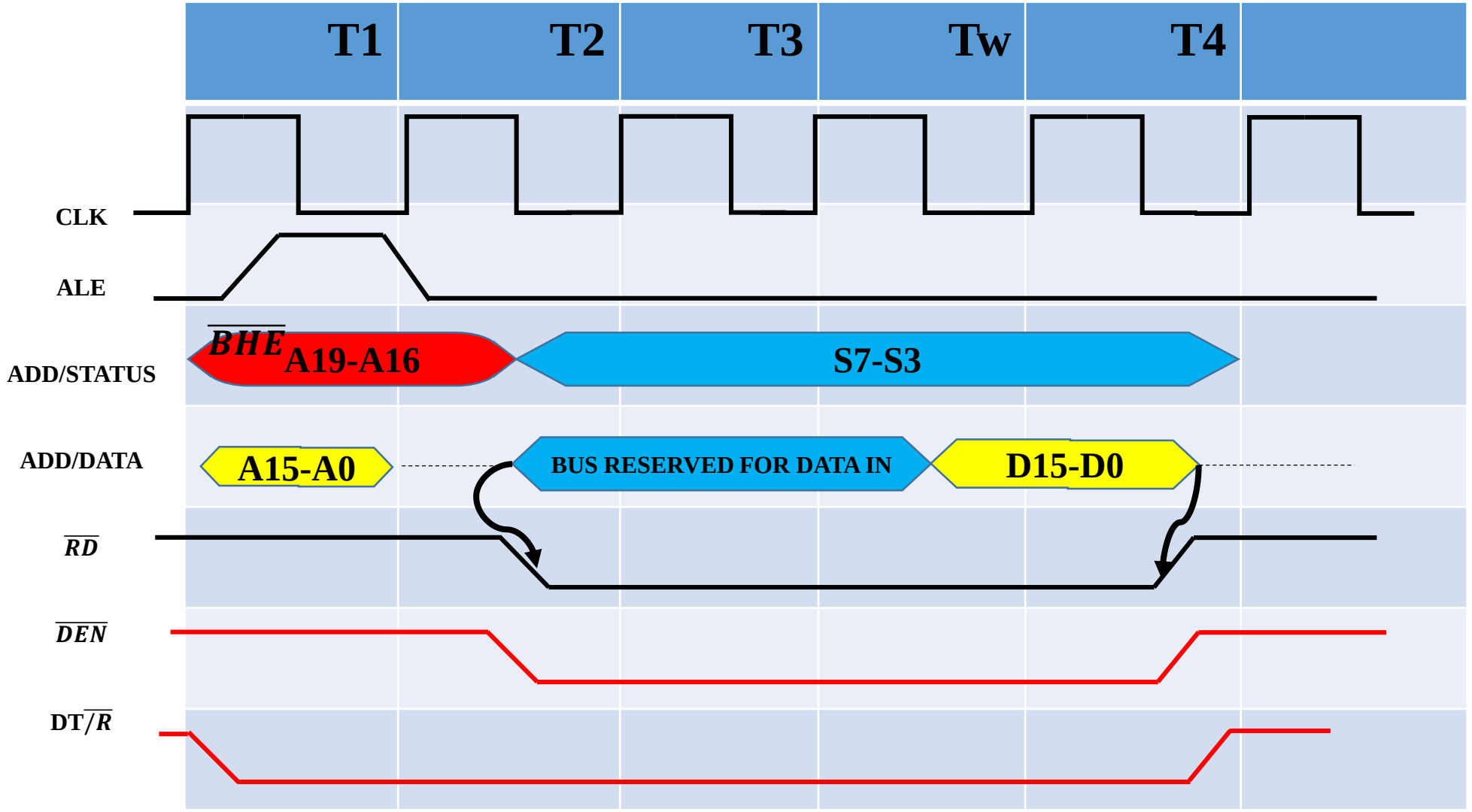
C020H	FAH
C021H	



Read and write bus timing of 8086 microprocessor

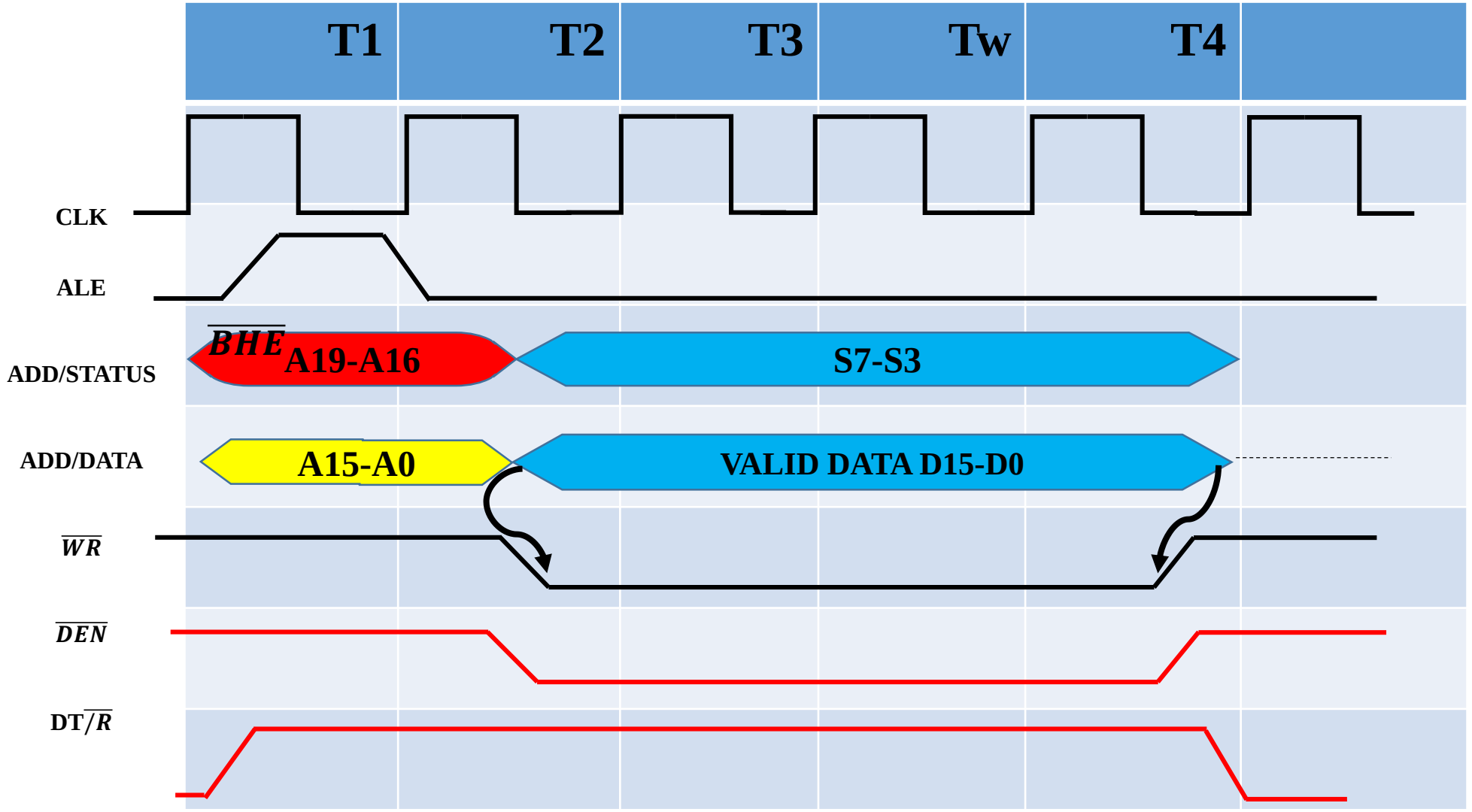
- The working of the minimum mode configuration system can be better described in terms of the timing diagrams rather than qualitatively describing the operations.
- The op-code fetch and read cycles are similar.
- Hence the timing diagram can be categorized in two parts, the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.

Read cycle timing diagram minimum mode 8086

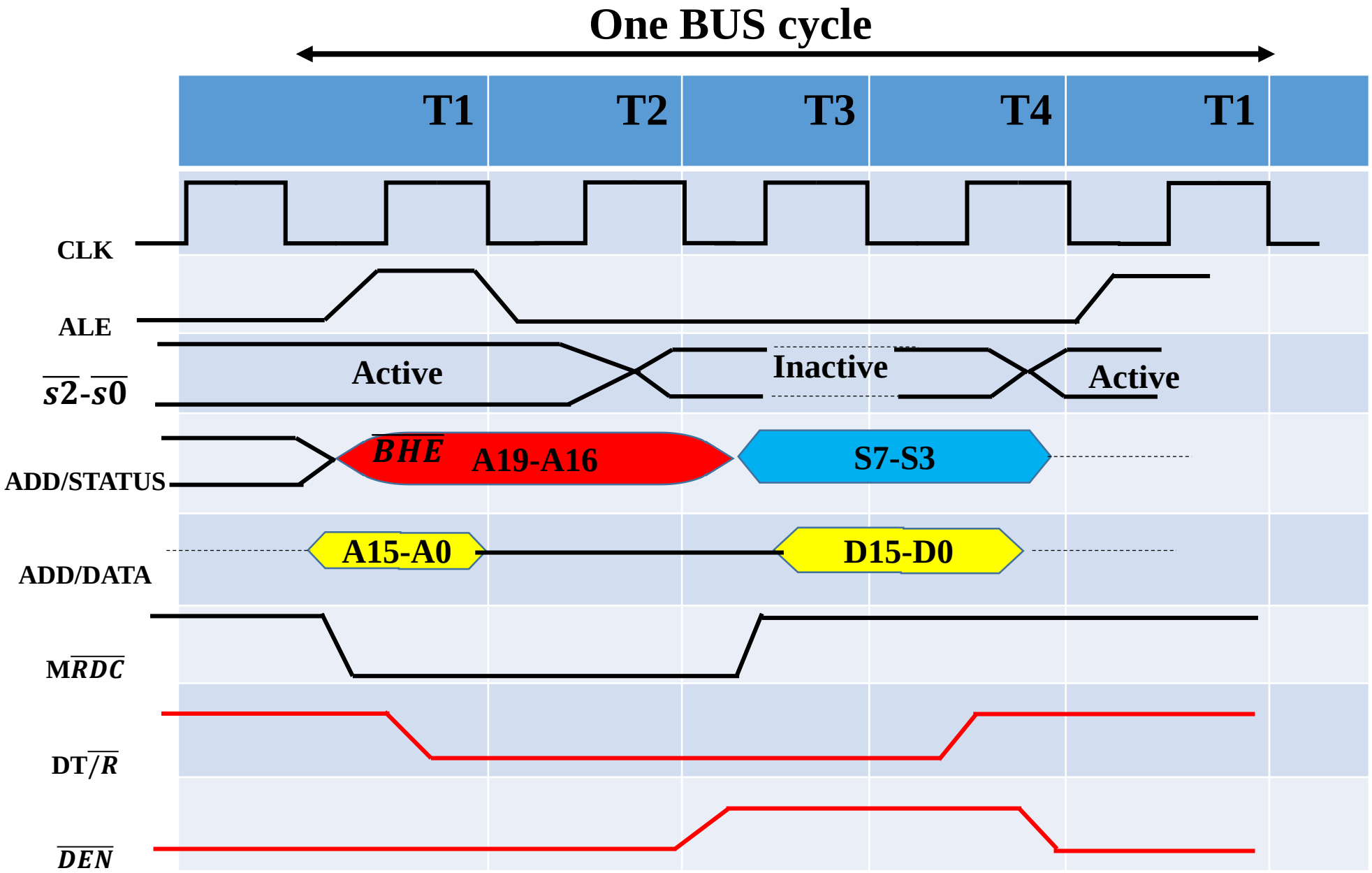


- The read cycle begins in T 1 with the assertion of address latch enable (ALE) signal and also $M/\overline{IO}$ signal.
- During the negative going edge of this signal, the valid address is latched on the local bus.
- The $\overline{BHE}$ and A0 signals address low, high or both bytes.
- From T1 to T4 , the $M/\overline{IO}$ signal indicates a memory or I/O operation.
- At T2, the address is removed from the local bus and is sent to the output. The bus is then tri-stated.
- The read (RD) control signal is also activated in T2.
- The read (RD) signal causes the address device to enable its data bus drivers. After RD goes low, the valid data is available on the data bus.
- The addressed device will drive the READY line high. When the processor returns the read signal to high level, the addressed device will again tristate its bus drivers.

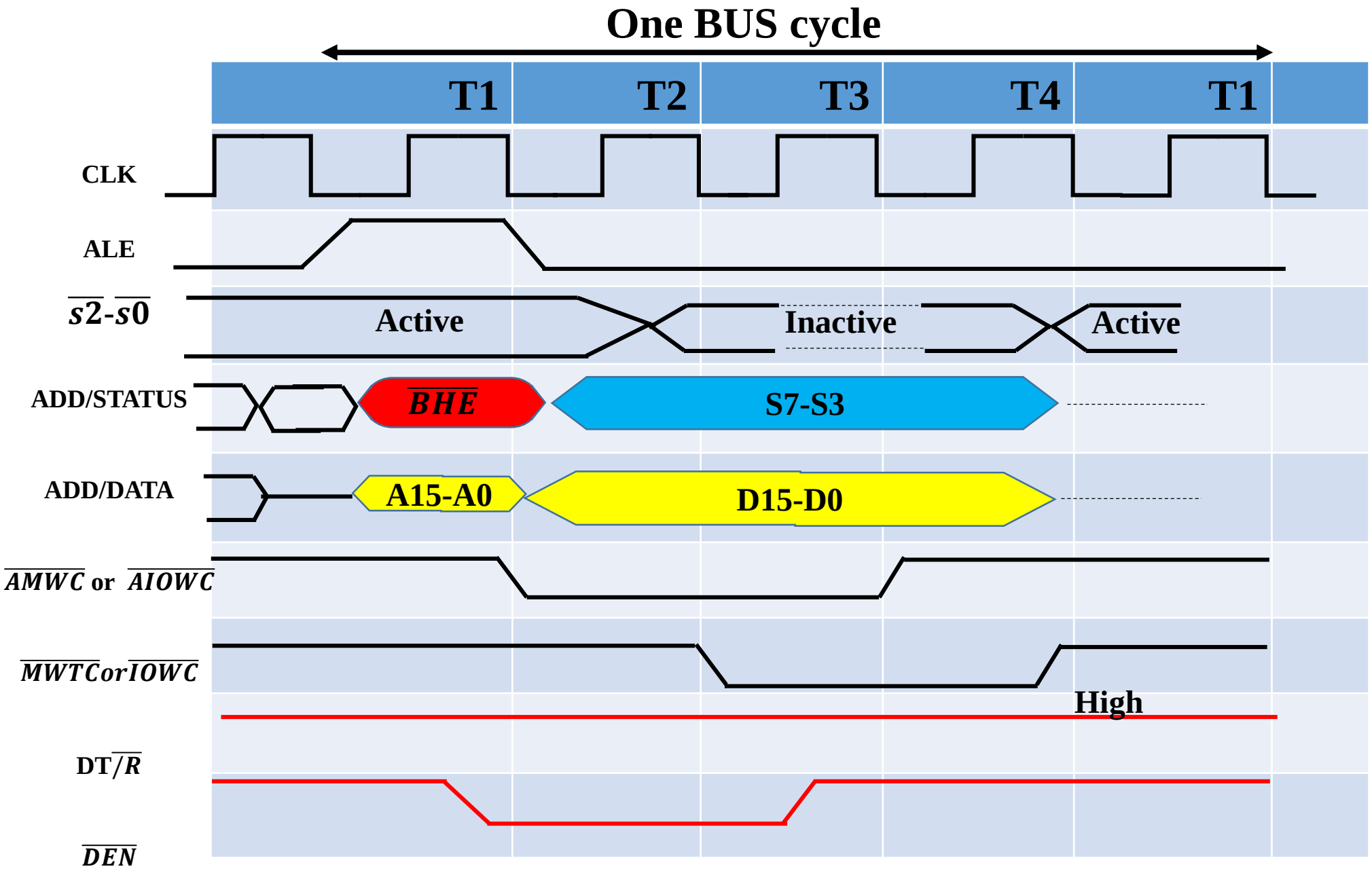
Write cycle timing diagram minimum mode 8086



Read cycle timing diagram maximum mode 8086



Write cycle timing diagram maximum mode 8086



MEMORY DEVICES

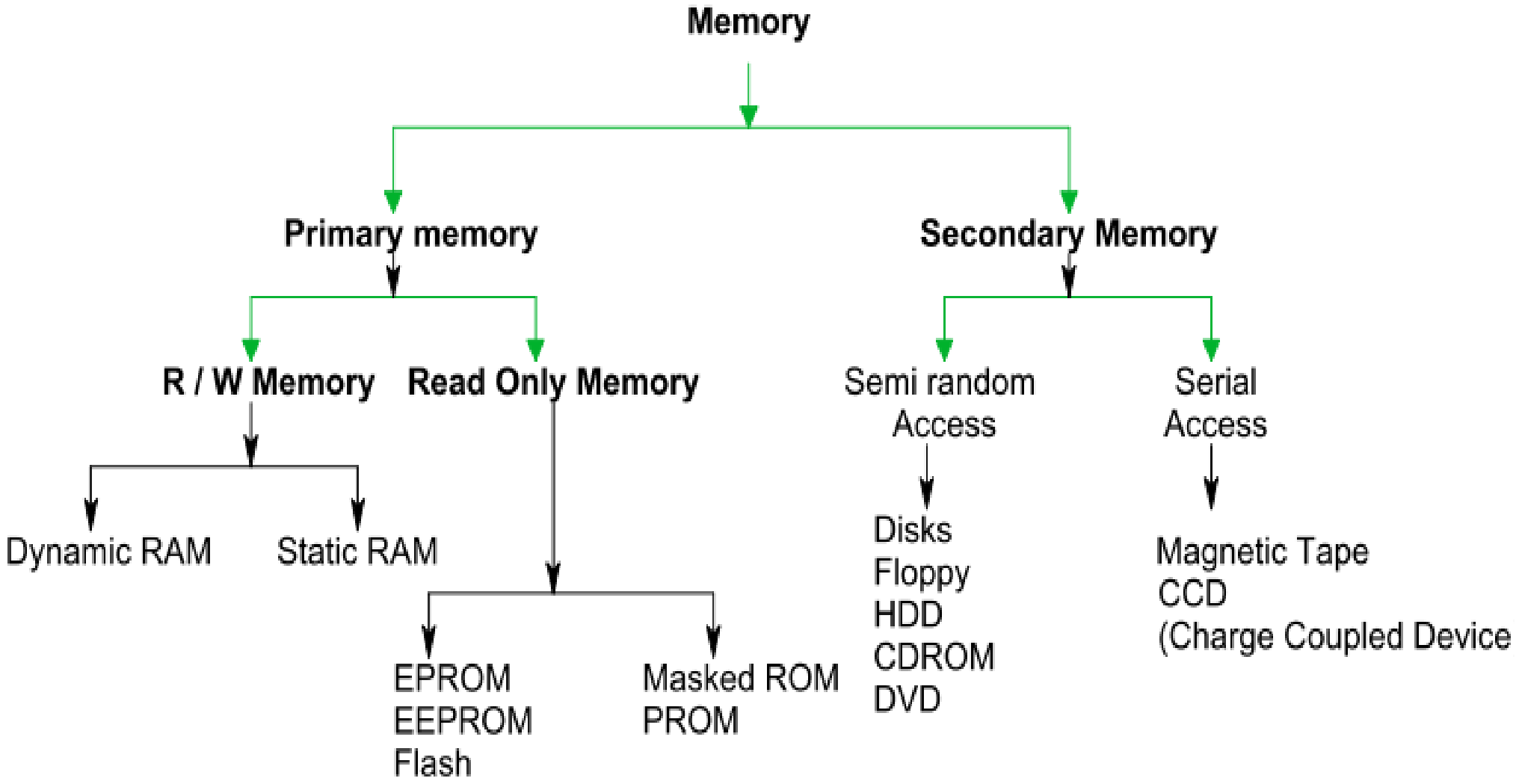


Fig: Classification of memory devices

The Memory Hierarchy

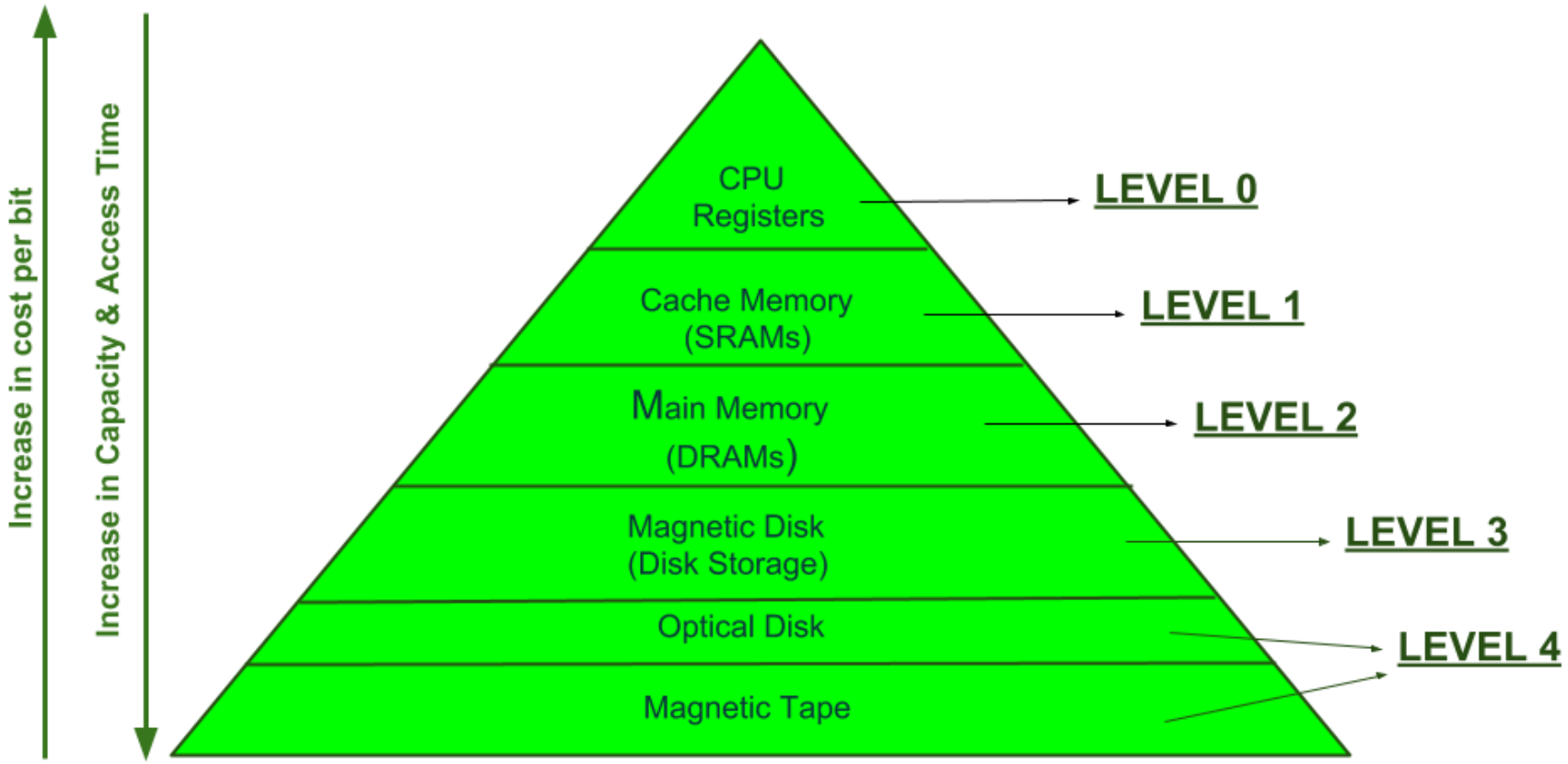


Fig: **MEMORY HIERARCHY DESIGN**

Address decoding:

- Microprocessor is connected with memory and I/O devices via common address and data bus.
- Only one device can send data at a time and other devices can only receive that data.
- In order to avoid data grabbling, the proper device must be addressed at proper time, the technique called ***address decoding***.

- In address decoding method, all devices like memory blocks, I/O units etc. are assigned with a specific address.
- The address of the device is determined from the way in which the address lines are used to derive a special device selection signal called ***chip select (CS).***
- If the microprocessor has to write or to read from a device, the CS signal to that block should be enabled and the address decoding circuit must ensure that CS signal to other devices are not activated.

Address decoding (cont.):

- Depending upon the no. of address lines used to generate chip select signal for the device, the address decoding is classified as:
  1. **I/O mapped I/O**
  2. **Memory mapped I/O**

1. I/O mapped I/O:

- Devices are given a separate addressing region from the memory known as ‘ports’.
- 8-bit address lines for creating this special address space for the I/O devices in 8085, i.e. 2^8=256 bytes of address space (00h-ffh).
- Dedicated address region for ***I/O***s and have dedicated ***I/O*** instructions.

- ***I/O mapped I/Os*** can send/receive data from the processor using ***IN*** and ***OUT*** commands only.
- None of the ***ALU*** operations can be directly applied to the data of the ***I/O mapped I/***O devices.
- Usually I/O mapped I/O is used to map devices like 8255A, 8251A etc.

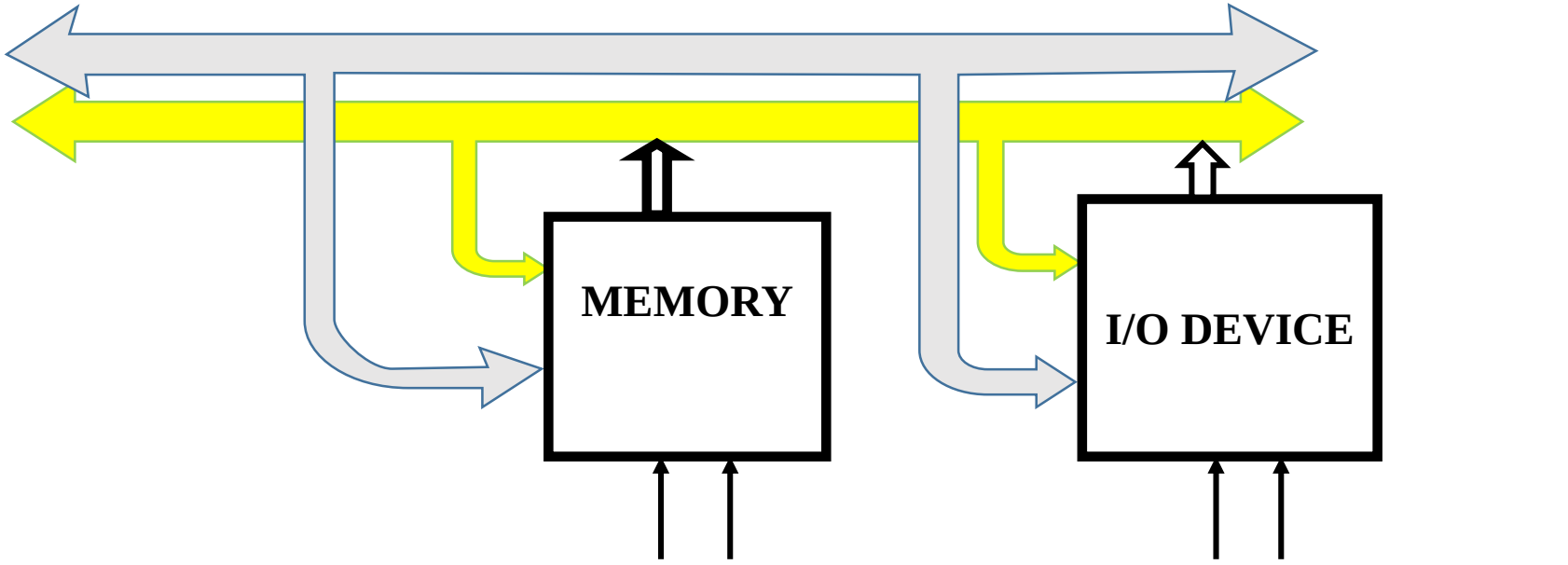
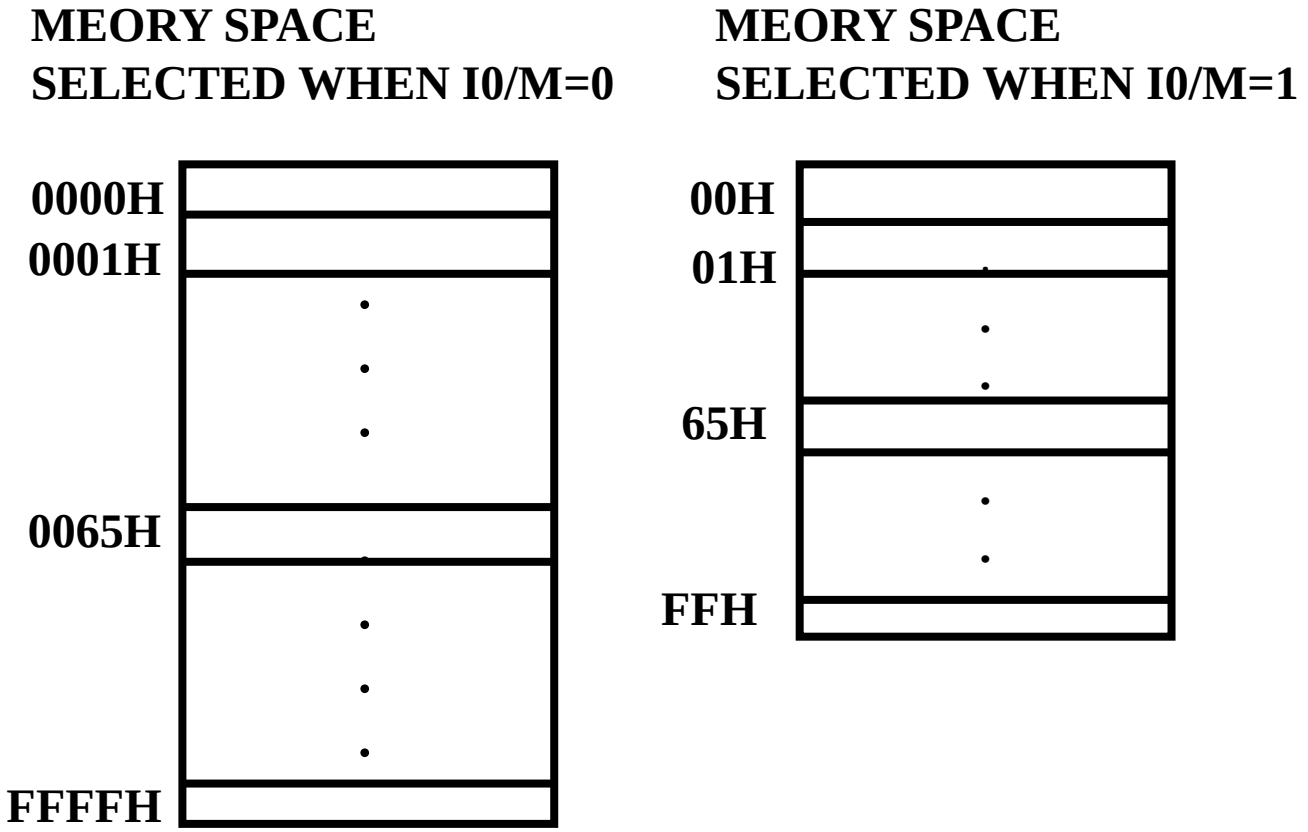


FIG: IO mapped IO (isolated I/O interfacing)



- We get two separate address spaces when we use IO mapped IO method to interface I/O devices.
- The I/O devices get their own special memory space.
- We can choose which address space to communicate with using the IO/M pin.

2. Memory Mapped I/O

- The processor treats the I/O devices like any other memory location.
- The ***I/O*** devices are efficiently mapped into the system memory along with the RAM and ROM memory.
- These devices are assigned with a 16-bit address value within the entire address range of the intel 8085 microprocessor.
- Exchange of data takes place with the help of memory instructions.
- The ***I/O*** device information can also be sent to the ***ALU.***
- The ***LOAD*** and ***STORE*** instructions are executed to read from and write to the I/O devices, just like they are utilized for the memory.

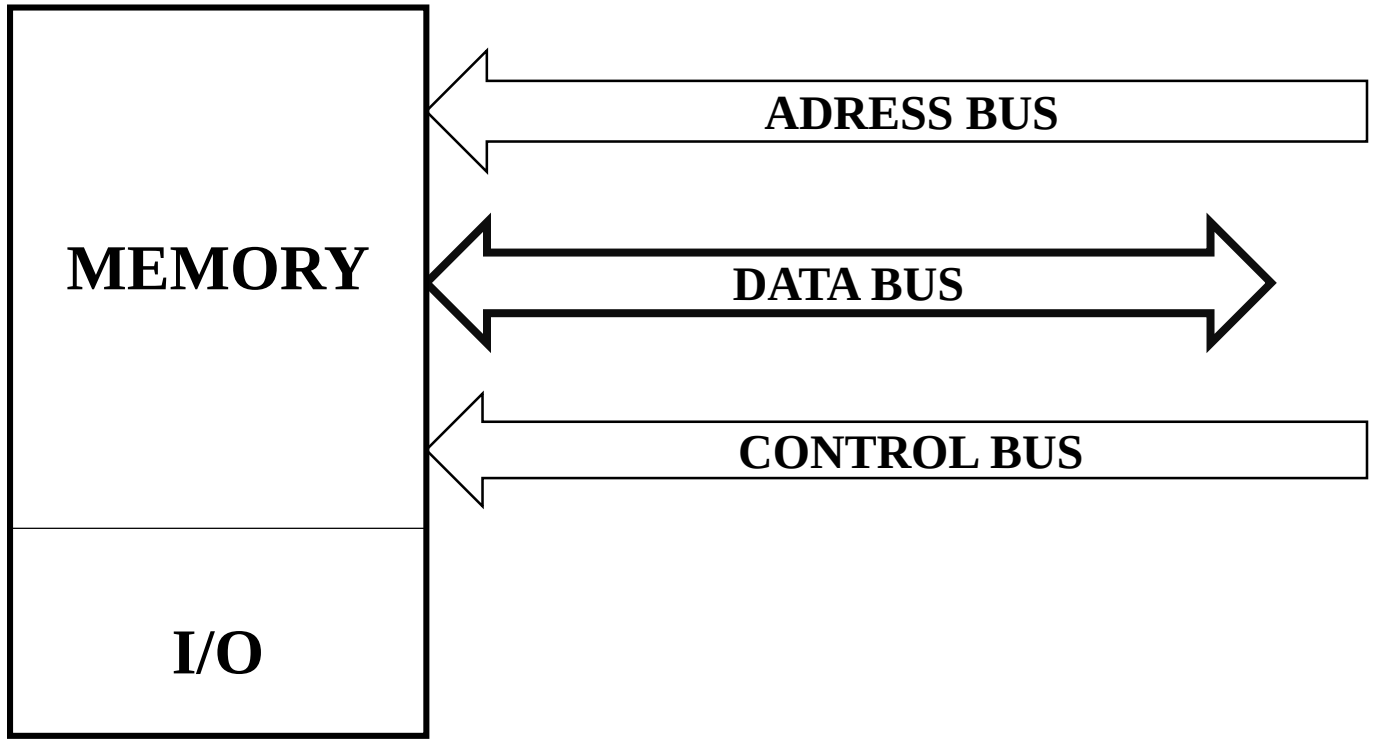
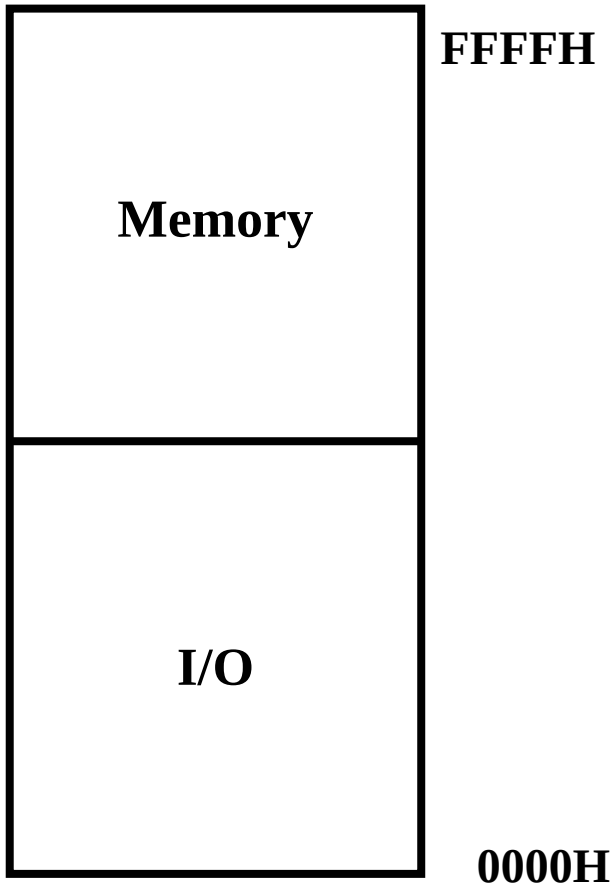


Fig: Memory-Mapped I/O Interfacing



Unified address space for both, memory and I/O

- Depending on the ***address*** that are ***allocated*** to the device the address decoding are categorized in the following two groups.
  1. **Unique Address Decoding**
  2. **Non Unique Address decoding**

1. Unique Address Decoding:

- all the address lines on the mapping mode are used for address decoding.
- **It means all 8-lines in I/O mapped I/O and** all 16 lines in memory mapped I/O are used to derive signal.
- It is expensive and complicated but fault proof in all cases.

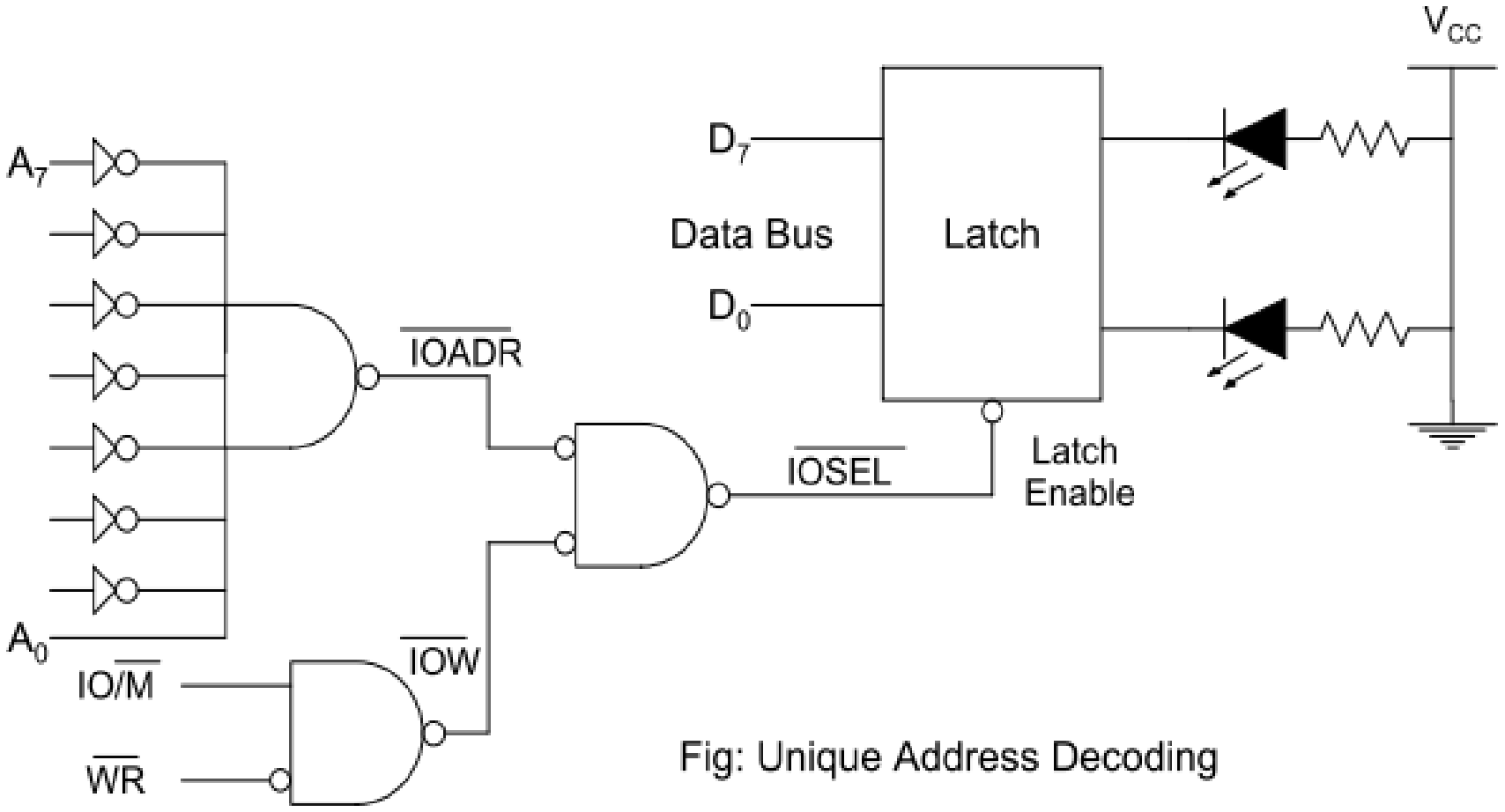


Fig: Unique Address Decoding

- If A0 is high and A7-A1 are low and if $\overline{IOW}$ becomes low, the latch gets enabled.
- The data to the LED can be transferred in only one case and hence the device has unique address of 01H.

Ex: Eight I/P switch interfacing at 53H (01010011).

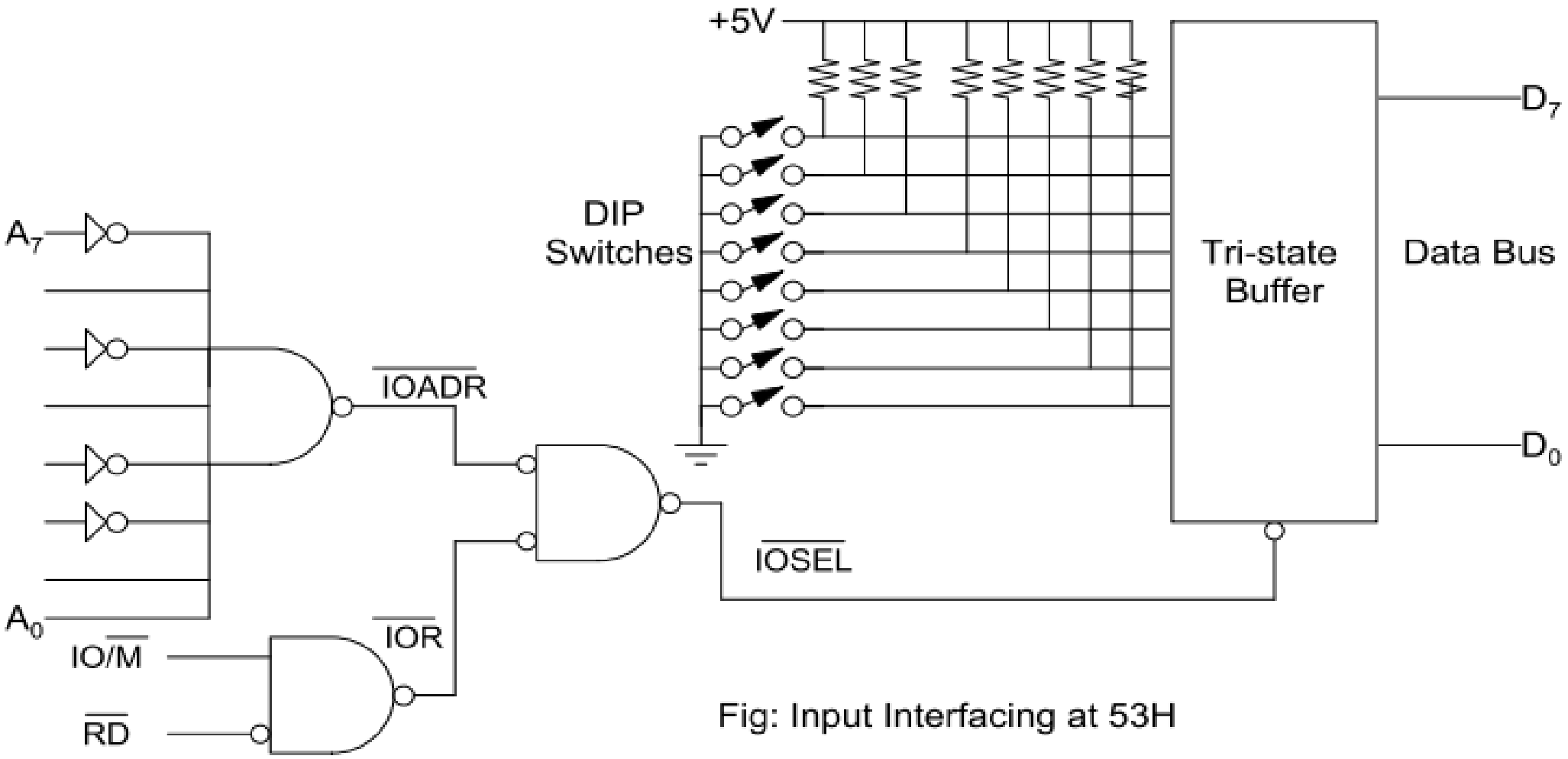


Fig: Input Interfacing at 53H

2. Non Unique Address decoding

- All the address lines available on that mode are not used.
- Though it is cheaper there may be a chance of address conflict.
- Here, if A0 and $\overline{IOW}$ is low, then latch gets enabled.
- A1-A7 are neglected, i.e. any even address can enable the latch.

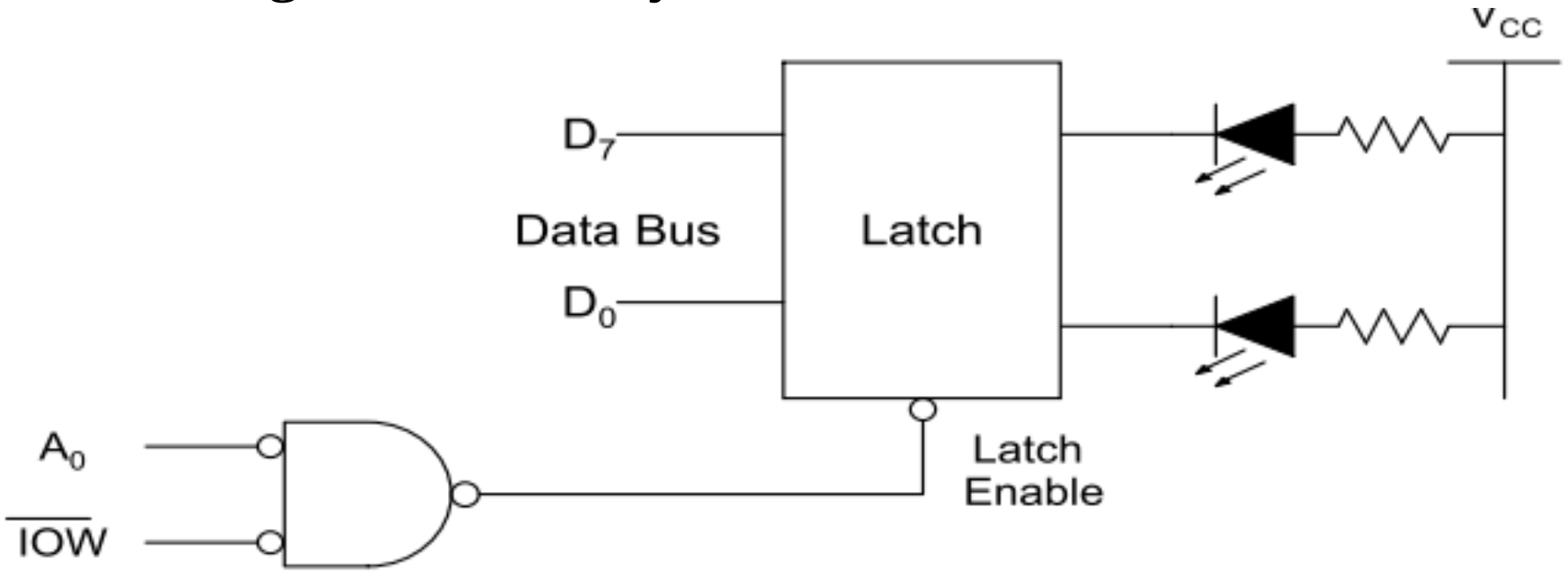


Fig: Non unique Address Decoding