

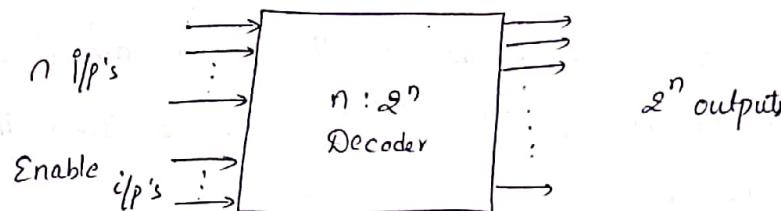
UNIT-5

Combinational Circuits - II

①

Design of Decoder:

A decoder is a multiple-input; multiple-output logic circuit which converts coded inputs into coded outputs, where the input and output codes are different.



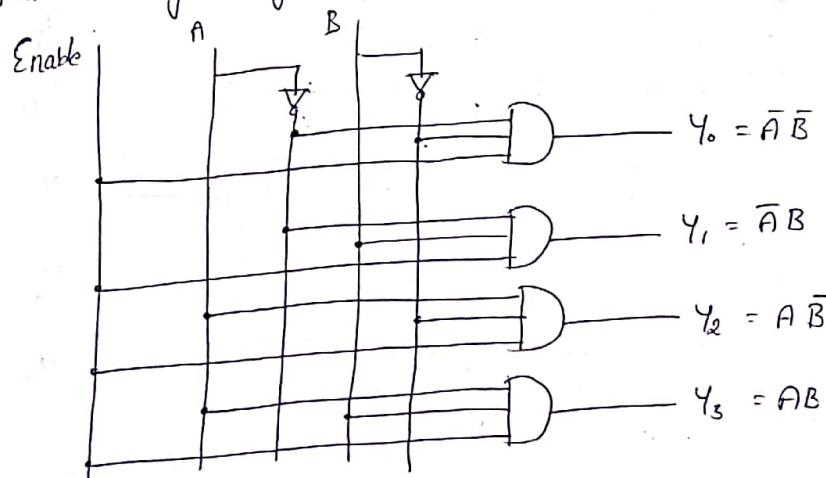
The encoded information is presented as n inputs producing 2^n outputs. A decoder is provided with enable inputs to activate decoded output based on data inputs. When any one enable input is unasserted, all outputs of decoder are disabled.

Binary Decoder:

A decoder which has an n -bit binary input code and a one activated output out-of- -2^n output code is called binary decoder.

2 to 4 Decoder:

Here, 2 inputs are decoded into four outputs, each output representing one of the minterms of the 2 i/p variables. The two inverters provide complement of the i/p's & each one of four AND gates generates one of the minterms.

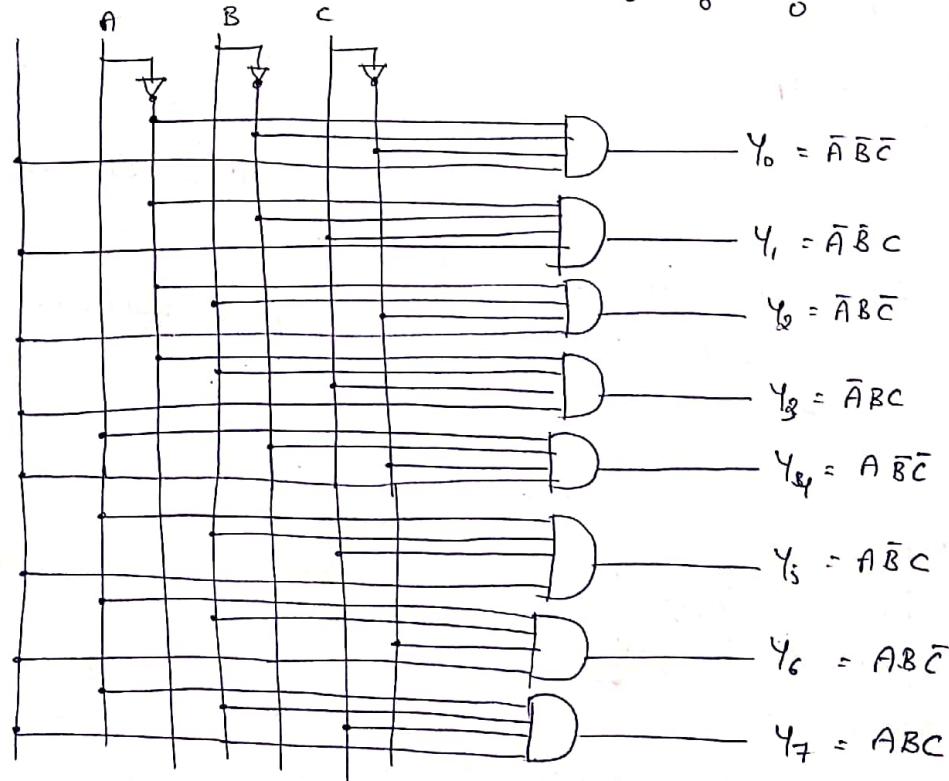


Inputs			Outputs			
En	A	B	Y_3	Y_2	Y_1	Y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

If enable = 0 then all the outputs are 0. If enable = 1 then the outputs Y_0 to Y_3 is active for a given input.

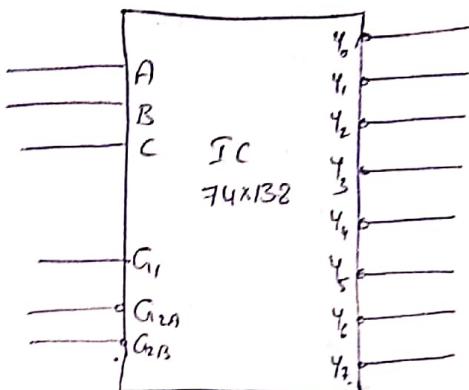
3 to 8 Decoder :

Inputs			Outputs								
En	A	B	C	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	1	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	1	0	0	0	0	0	0



IC 74x138 (3 to 8 Decoder)

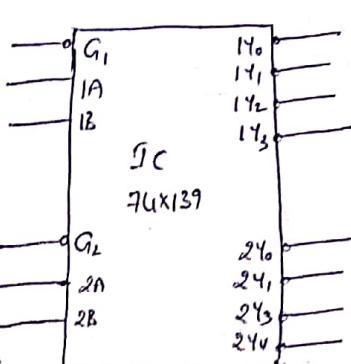
The IC 74x138 is a commercially available 3 to 8 decoder. It accepts three binary inputs (A, B, C) and when enabled, provides eight individual active low outputs ($\bar{Y}_0 - \bar{Y}_7$). The device has three enable inputs : two active low ($\bar{G}_{2A}, \bar{G}_{2B}$) and one active high (G_1).



Inputs			Outputs										
G_{2B}	G_{2A}	G_1	C	B	A	\bar{Y}_7	\bar{Y}_6	\bar{Y}_5	\bar{Y}_4	\bar{Y}_3	\bar{Y}_2	\bar{Y}_1	\bar{Y}_0
1	x	x	x	x	x	1	1	1	1	1	1	1	1
0	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	0	x	x	x	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	0
0	0	1	0	0	1	1	1	1	1	1	1	0	1
0	0	1	0	1	0	1	1	1	1	1	0	1	1
0	0	1	0	1	1	1	1	1	1	0	1	1	1
0	0	1	1	0	0	1	1	1	0	1	1	1	1
0	0	1	1	0	1	1	1	0	1	1	1	1	1
0	0	1	1	1	0	1	0	1	1	1	1	1	1
0	0	1	1	1	1	0	1	1	1	1	1	1	1

The IC 74x139 Dual 2 to 4 Decoder :

The 74x139 consists of two independent and identical 2 to 4 decoders. The o/p's are active low.



Inputs			Outputs			
\bar{G}	B	A	\bar{Y}_3	\bar{Y}_2	\bar{Y}_1	\bar{Y}_0
1	x	x	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

Cascading Binary Decoders :

Binary decoder circuits can be connected together to form a larger decoder circuit.

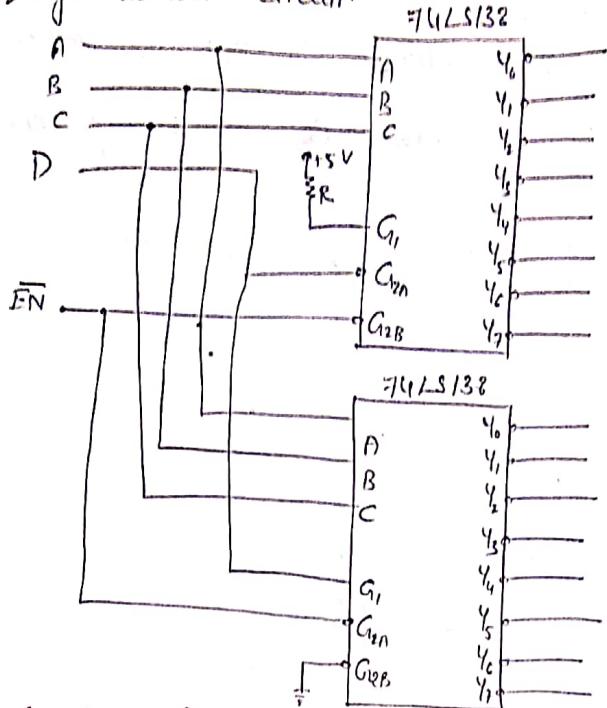
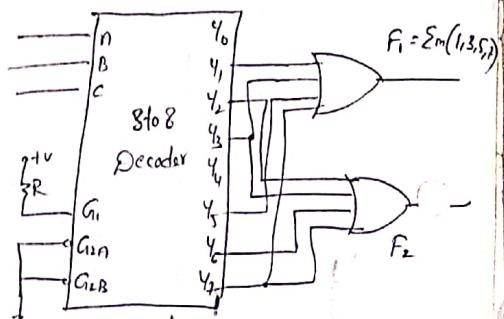
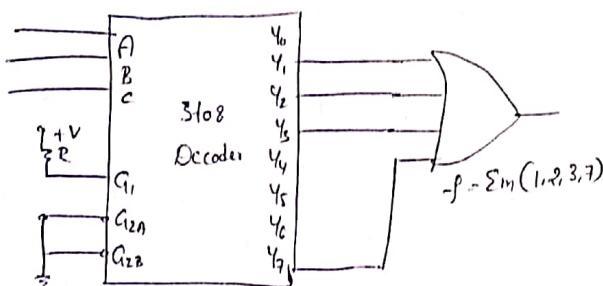


Fig : 4x16 Decoder

Realization of multiple output function using Decoders :

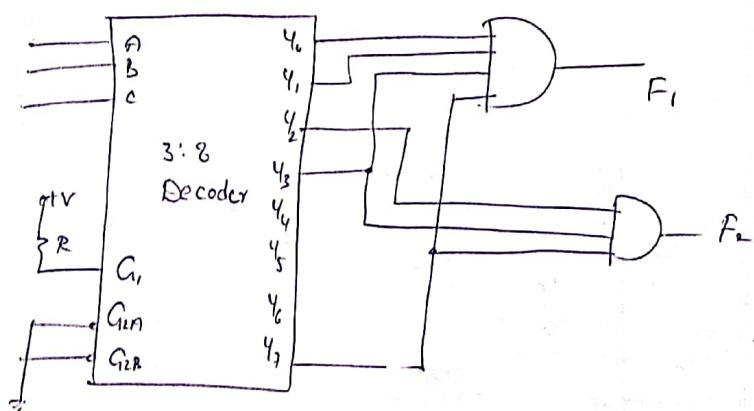
$$\rightarrow f = \Sigma m(1, 2, 3, 7)$$

$$\begin{aligned} \rightarrow F_1(A, BC) &= \Sigma m(1, 3, 5, 7) \\ F_2(A, BC) &= \Sigma m(2, 3, 6, 7) \end{aligned}$$

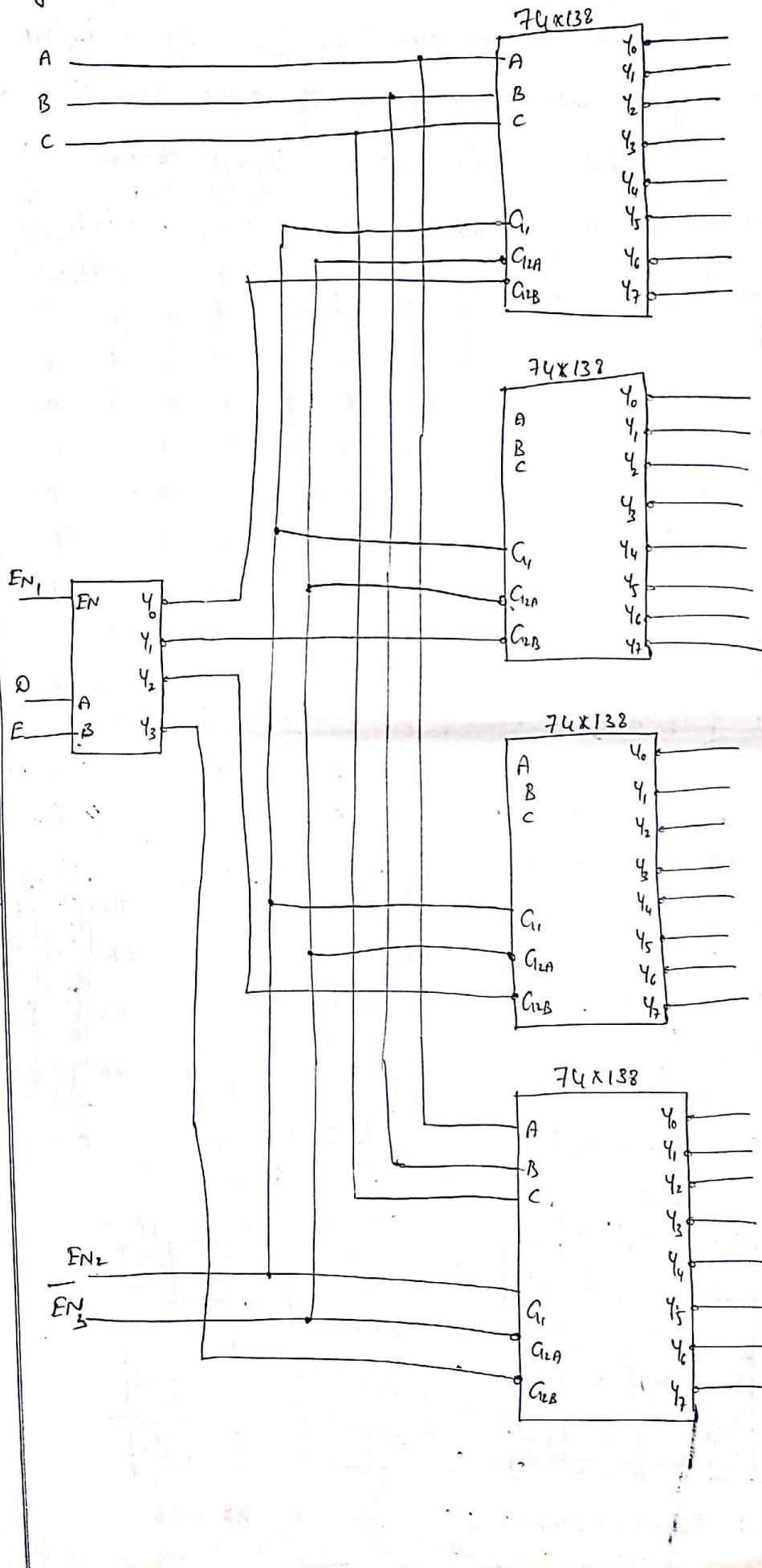


$$\rightarrow F_1 = \Sigma m(0, 1, 3, 7)$$

$$F_2 = \Sigma m(2, 3, 6)$$



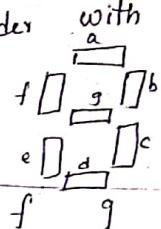
To *Tom*
Design 5 to 32 decoder using 2 to 4 & 3 to 8 decoder



BCD to 7-Segment Display Decoder :

In most practical applications, seven segment displays are used to give a visual indication of the output states of the digital 3.

The truth-tables for BCD to 7-Segment decoder with common anode is given below.



Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	0	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

for a

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	1	1
$\bar{A}B$	0	1	1	1
$A\bar{B}$	x	x	x	x
AB	1	1	x	1

$$a = A + C + BD + \bar{B}\bar{D}$$

for b

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	1	0	1	0
AB	x	x	x	x
$A\bar{B}$	1	1	x	x

$$b = \bar{B} + \bar{C}\bar{D} + CD$$

for c

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	1	1	1	1
AB	x	x	x	x
$A\bar{B}$	1	1	x	x

$$c = B + \bar{C} + D$$

for d

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1		1	1
$\bar{A}B$		1		
AB	x	x	x	x
$A\bar{B}$	1	1	x	x

$$d = \bar{B}\bar{D} + C\bar{D} + B\bar{C}D + \bar{B}C + A$$

for e

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1			1
$\bar{A}B$				1
AB				x
$A\bar{B}$	1			x

$$e = \bar{B}\bar{D} + C\bar{D}$$

for f

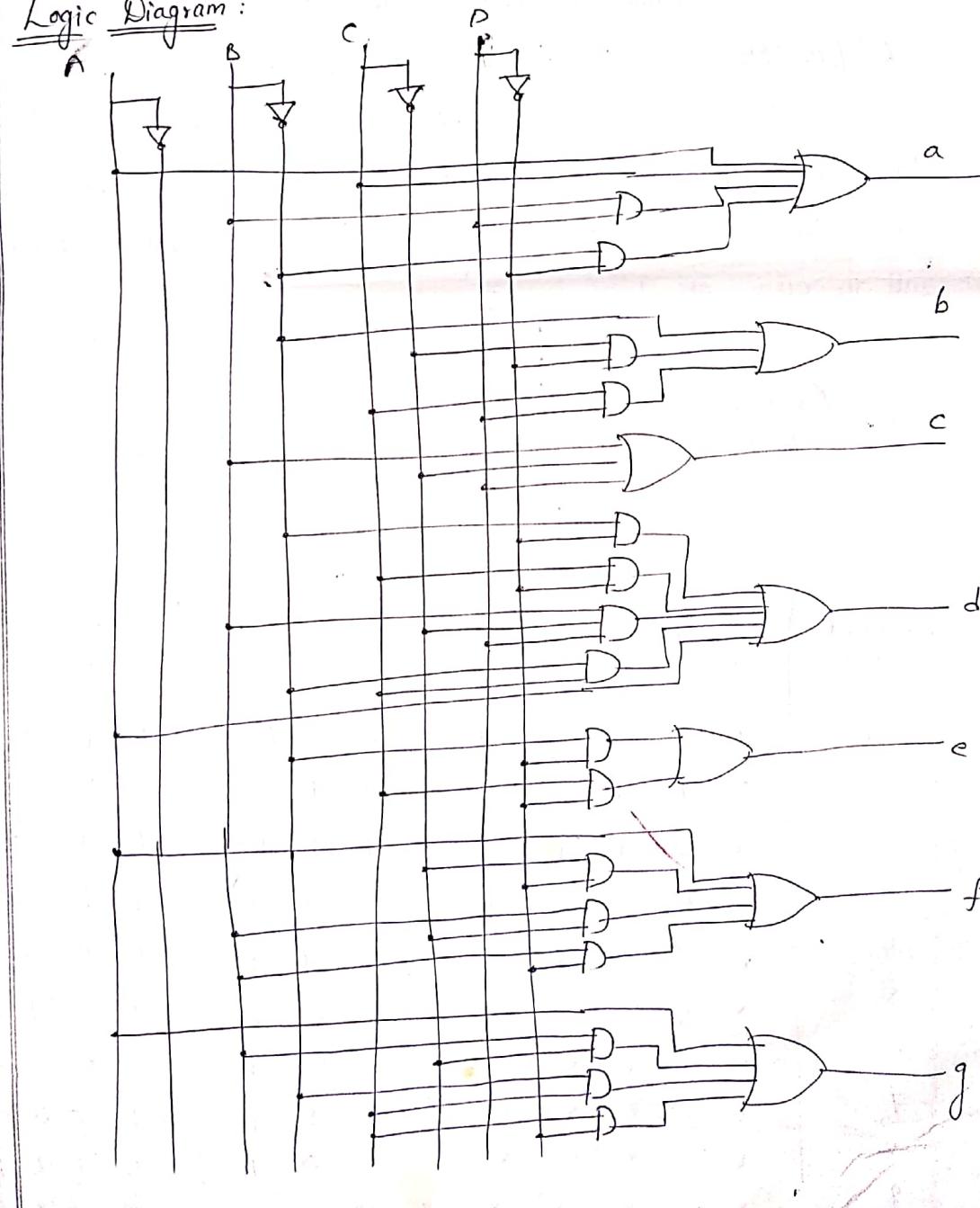
$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1		
$\bar{A}B$	1	1	
$A\bar{B}$	X	X	X
AB		X	X
$A\bar{B}$	1	1	X
$\bar{A}B$		X	X

$$f = A + \bar{C}\bar{D} + B\bar{C} + B\bar{D}$$

for g

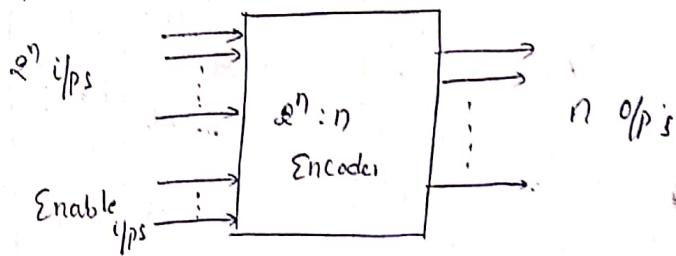
$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$			1
$\bar{A}B$	1	1	
AB	X	X	X
$A\bar{B}$	1	1	X
$\bar{A}B$		X	X

$$g = A + B\bar{C} + \bar{B}C + C\bar{D}$$

Logic Diagram:

Encoder :

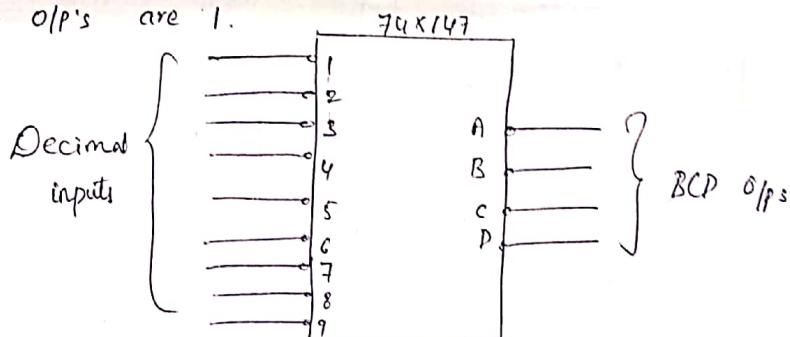
An encoder is a digital circuit that performs the inversion operation of decoder. An encoder has 2^n input lines and 'n' output lines.



Decimal to BCD Encoder :

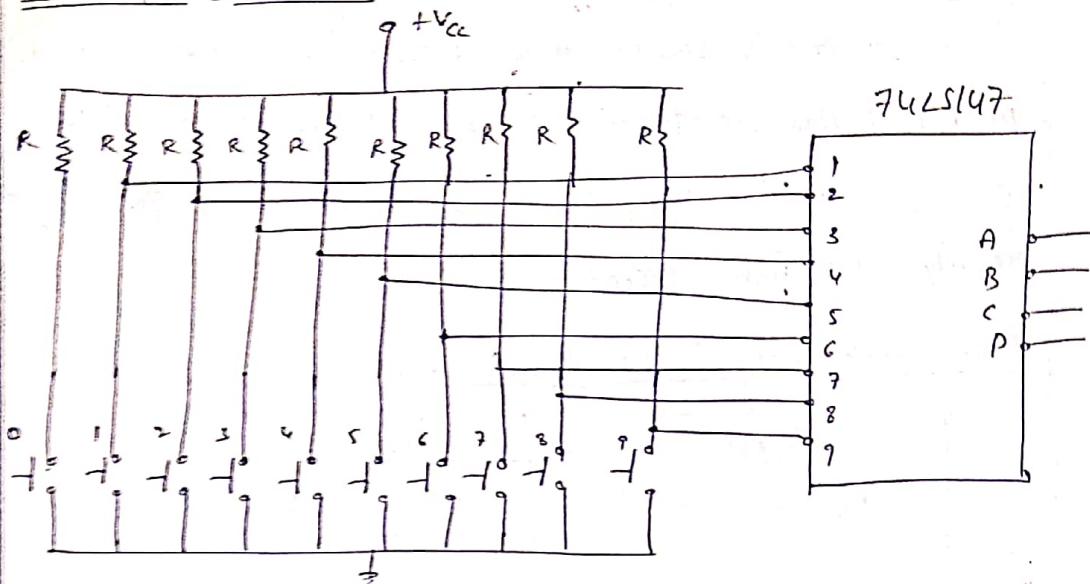
The decimal to BCD encoder, usually has ten inputs & four o/p's.

The IC 74x147 has nine input lines & four o/p lines. Both i/p & o/p lines are asserted active low. It is important to note that there is no i/p line for zero. When this condition occurs all the o/p's are 1.



Decimal Value	Inputs									Output			
	1	2	3	4	5	6	7	8	9	D	C	B	A
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0
2	x	0	1	1	1	1	1	1	1	1	1	0	1
3	x	x	0	1	1	1	1	1	1	1	1	0	0
4	x	x	x	0	1	1	1	1	1	1	0	1	1
5	x	x	x	x	0	1	1	1	1	1	0	1	0
6	x	x	x	x	x	0	1	1	1	1	0	0	1
7	x	x	x	x	x	x	0	1	1	1	0	0	0
8	x	x	x	x	x	x	x	0	1	1	1	1	1
9	x	x	x	x	x	x	x	x	0	0	1	1	0

Ten Keypad Interface :

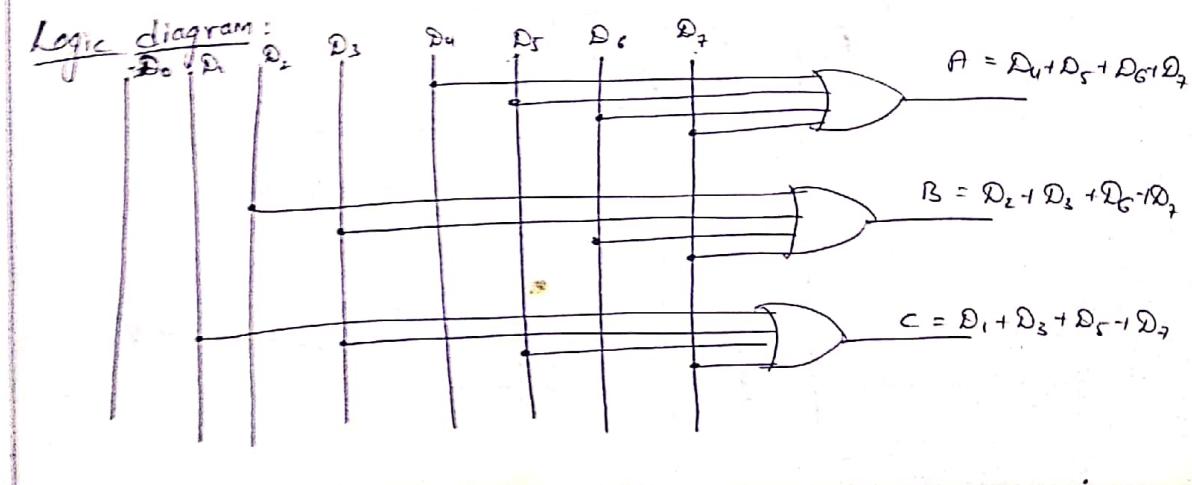


Octal to Binary Encoder :

It has 8 inputs and 3 outputs that generate the corresponding binary code.

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Logic diagram :



Priority Encoder :

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if two or more inputs are equal to 1 at the same time, the inputs having the highest priority will take precedence.

Truth Table for 4-bit Priority encoder :

Inputs				Outputs		
D_0	D_1	D_2	D_3	Y_1	Y_0	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

For Y_1

	$\bar{D}_2 \bar{D}_3$	$\bar{D}_2 D_3$	$D_2 \bar{D}_3$	$D_2 D_3$
$\bar{D}_0 \bar{D}_1$	x	1	1	1
$D_0 \bar{D}_1$		1	1	1
$D_0 D_1$		1	1	1
$\bar{D}_0 D_1$		1	1	1

$$Y_1 = D_2 + D_3$$

For Y_2

	$\bar{D}_2 \bar{D}_3$	$\bar{D}_2 D_3$	$D_2 \bar{D}_3$	$D_2 D_3$
$\bar{D}_0 \bar{D}_1$	x	1	1	1
$D_0 \bar{D}_1$		1	1	1
$D_0 D_1$		1	1	1
$\bar{D}_0 D_1$		1	1	1

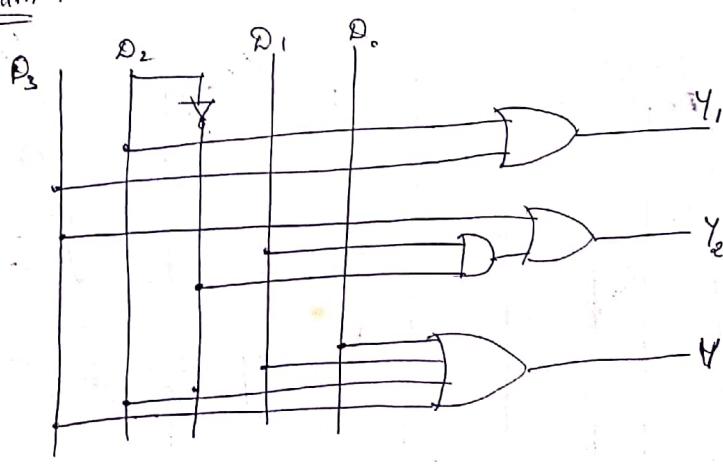
$$Y_2 = D_3 + D_1 \bar{D}_0$$

for V

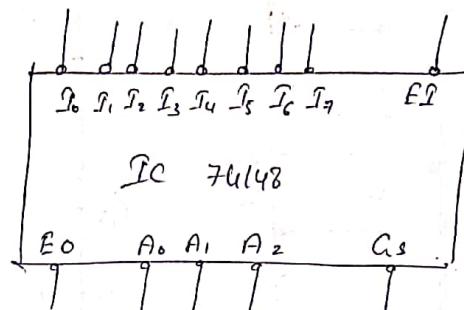
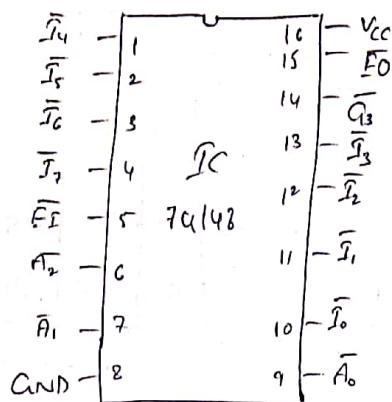
	$\bar{D}_2 \bar{D}_3$	$\bar{D}_2 D_3$	$D_2 \bar{D}_3$	$D_2 D_3$
$\bar{D}_0 \bar{D}_1$	x	1	1	1
$D_0 \bar{D}_1$		1	1	1
$D_0 D_1$		1	1	1
$\bar{D}_0 D_1$		1	1	1

$$V = D_0 + D_1 + D_2 + D_3$$

Logic Diagram :



IC 74xx148 (Priority Encoder):

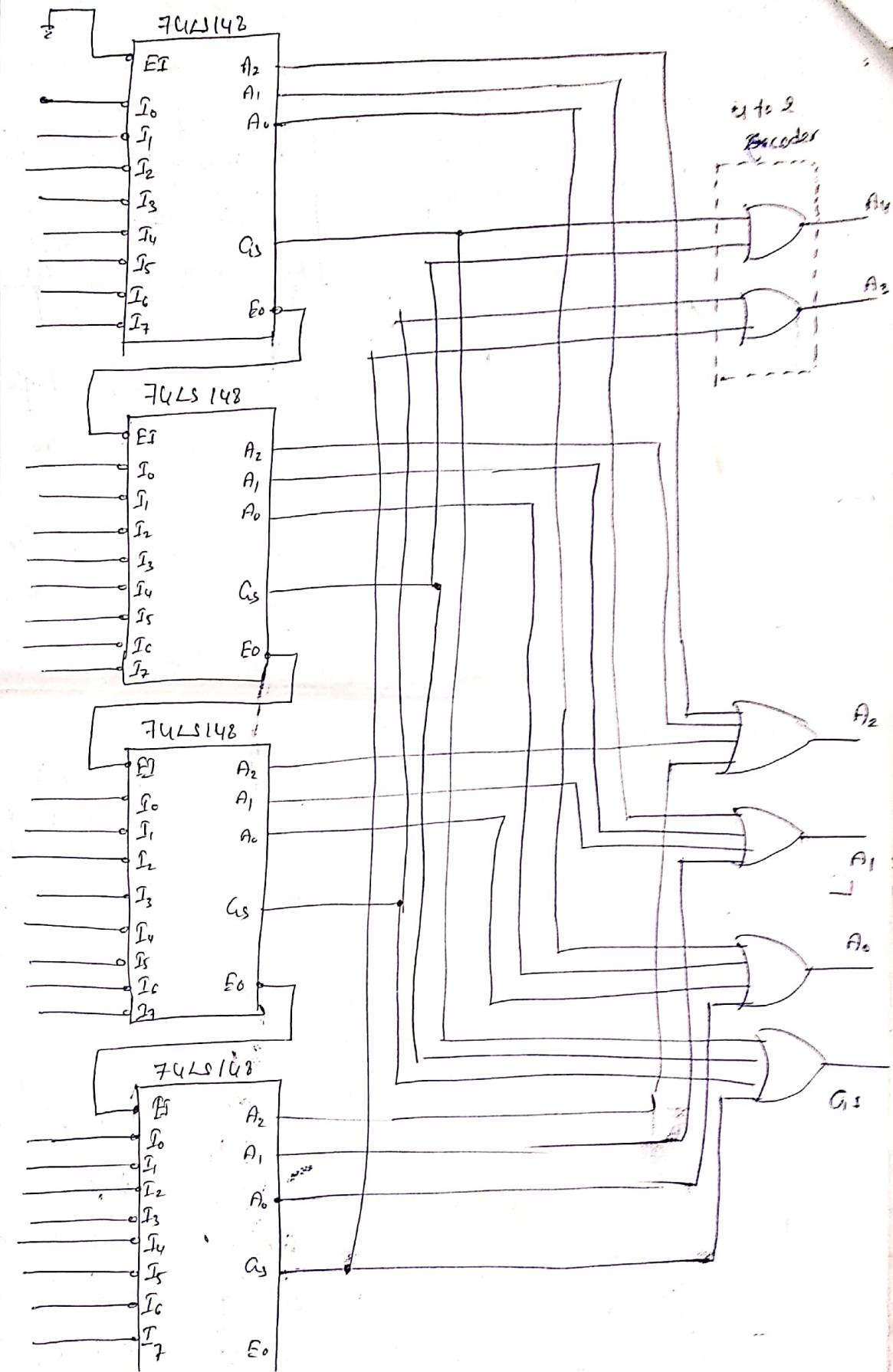


Input I_0 has least priority and I_7 has highest priority. EI is the active low enable input. A high on the EI will force all outputs to the inactive state.

A CS is Group Signal asserted when the device is enabled and one or more of the inputs to the encoder are active. Enable output (EO) is an active low signal that can be used to cascade several priority encoder devices.

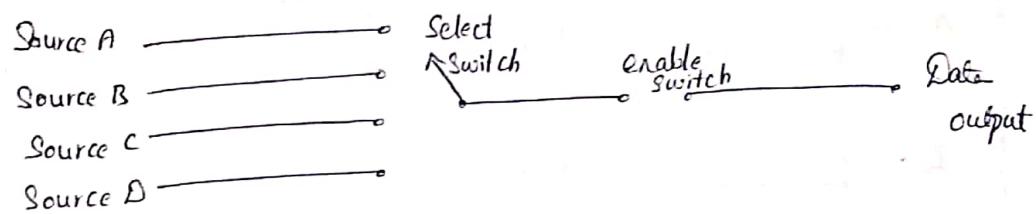
E.I	Inputs								outputs			
	0	1	2	3	4	5	6	7	A ₂	A ₁ , A ₀	CS	EO
1	x	x	x	x	x	x	x	x	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	1	0	1
0	x	0	1	1	1	1	1	1	1	0	0	1
0	x	0	1	1	1	1	1	1	1	0	1	0
0	x	x	0	1	1	1	1	1	1	0	0	0
0	x	x	x	0	1	1	1	1	0	1	1	0
0	x	x	x	x	0	1	1	1	0	1	0	1
0	x	x	x	x	x	0	1	1	0	0	1	0
0	x	x	x	x	x	x	0	1	0	0	0	1

Implement 82 input to 5 output priority encoder using 74LS148



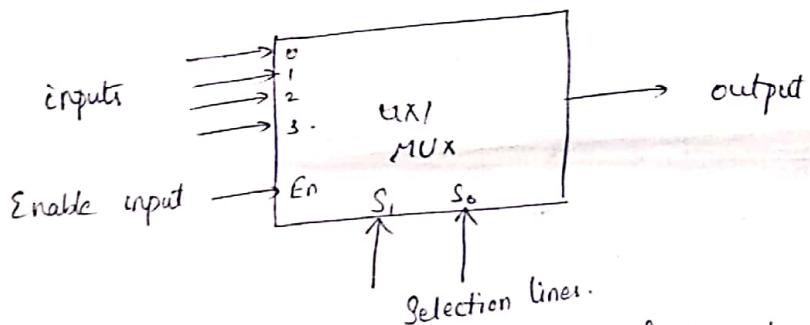
Multiplexer :

Multiplexer is a digital switch. It allows digital information from several sources to be routed onto a single O/p line. The basic multiplexer has several data i/p lines & a single O/p line. Normally, there are 2^n input lines and 'n' selection lines. Therefore, multiplexer is "Many into one".



4x1 Multiplexer :

It is having '4' input lines and one output line.

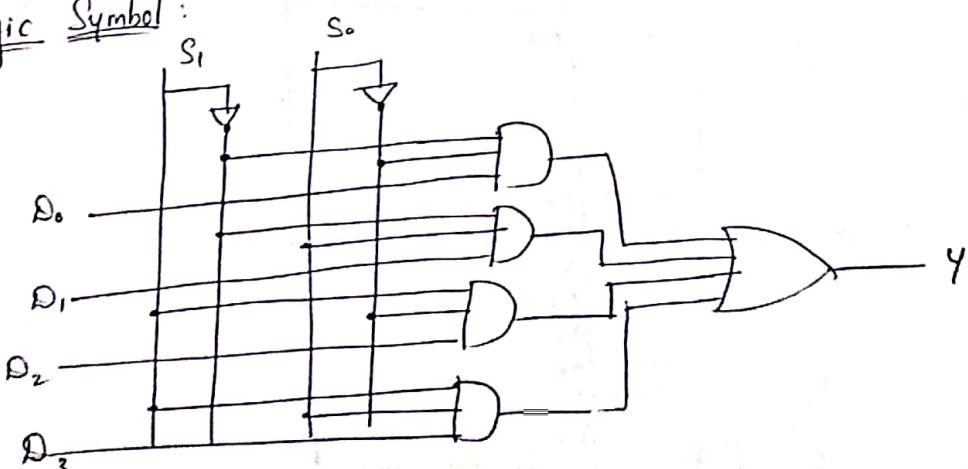


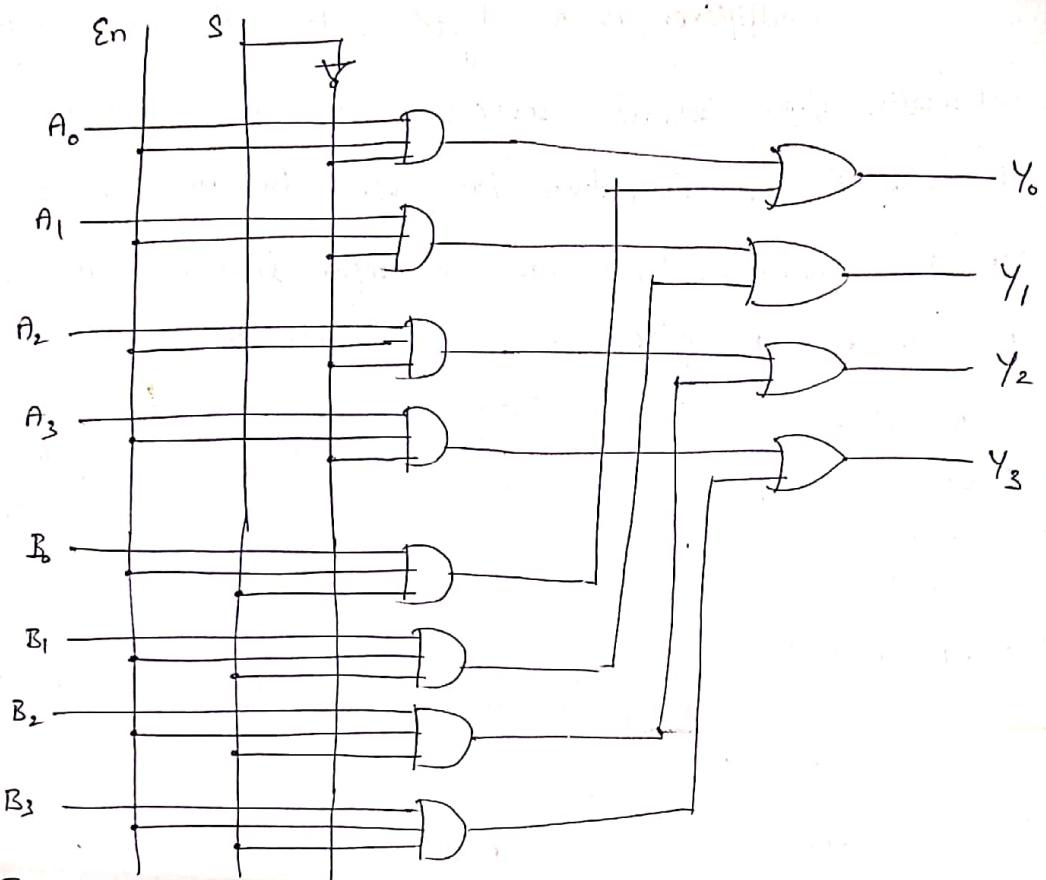
Function table :

S ₁	S ₀	Y
0	0	D ₀
0	1	D ₁
1	0	D ₂
1	1	D ₃

Here, for example, when S₁, S₀ = 01, the AND gate associated with data input D₁, has two of its inputs equal to '1' and third connected to D₁. Therefore the O/p of multiplexer is only D₁.

Logic Symbol :

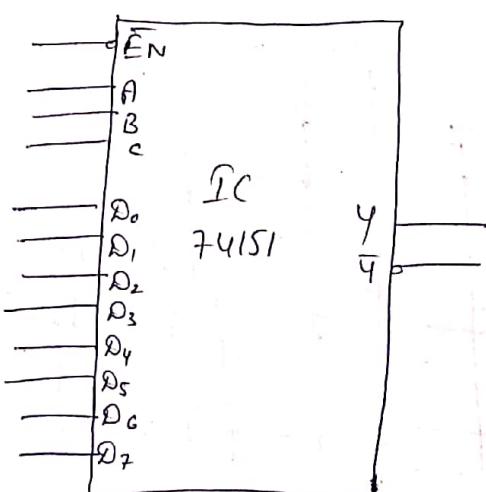


Quadruple 2 to 1 line multiplexer:Function table:

E	S	Output Y
1	x	All 0's
0	0	Select A
0	1	Select B

The IC 74xx151 (8 to 1 MUX):

It has 8 inputs. It provides two outputs, one is active high & other is active low. There are 3 select lines.

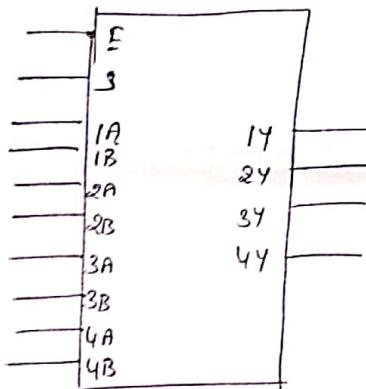


Function table :

EN	A	B	C	Y	\bar{Y}
1	x	x	x	0	1
0	0	0	0	D ₀	\bar{D}_0
0	0	0	1	D ₁	\bar{D}_1
0	0	1	0	D ₂	\bar{D}_2
0	0	1	1	D ₃	\bar{D}_3
0	1	0	0	D ₄	\bar{D}_4
0	1	0	1	D ₅	\bar{D}_5
0	1	1	0	D ₆	\bar{D}_6
0	1	1	1	D ₇	\bar{D}_7

The IC 74xx157 Quad - 2 input Multiplexer :

The IC 74xx157 is a quad 2-input multiplexer which selects 4 bits of data from two sources.



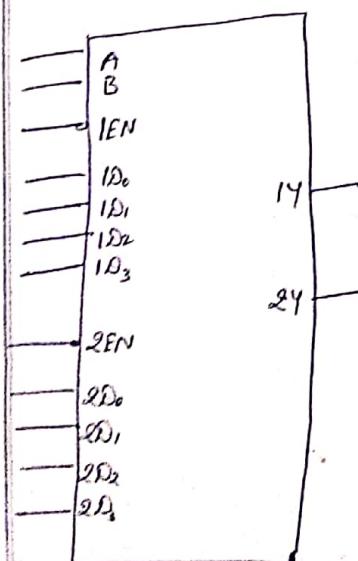
Truth Table

E	S	1A	2A	3A	4A	1B	2B	3B	4B
1	x	0	0	0	0	1	1	1	1
0	0	1A	2A	3A	4A	0	0	0	0
0	1	1B	2B	3B	4B	1	1	1	1

The IC 74xx153 Dual 4 to 1 Multiplexer :

It contains two identical & independent 4 to 1 multiplexers. Each multiplexer has separate inputs.

74xx153



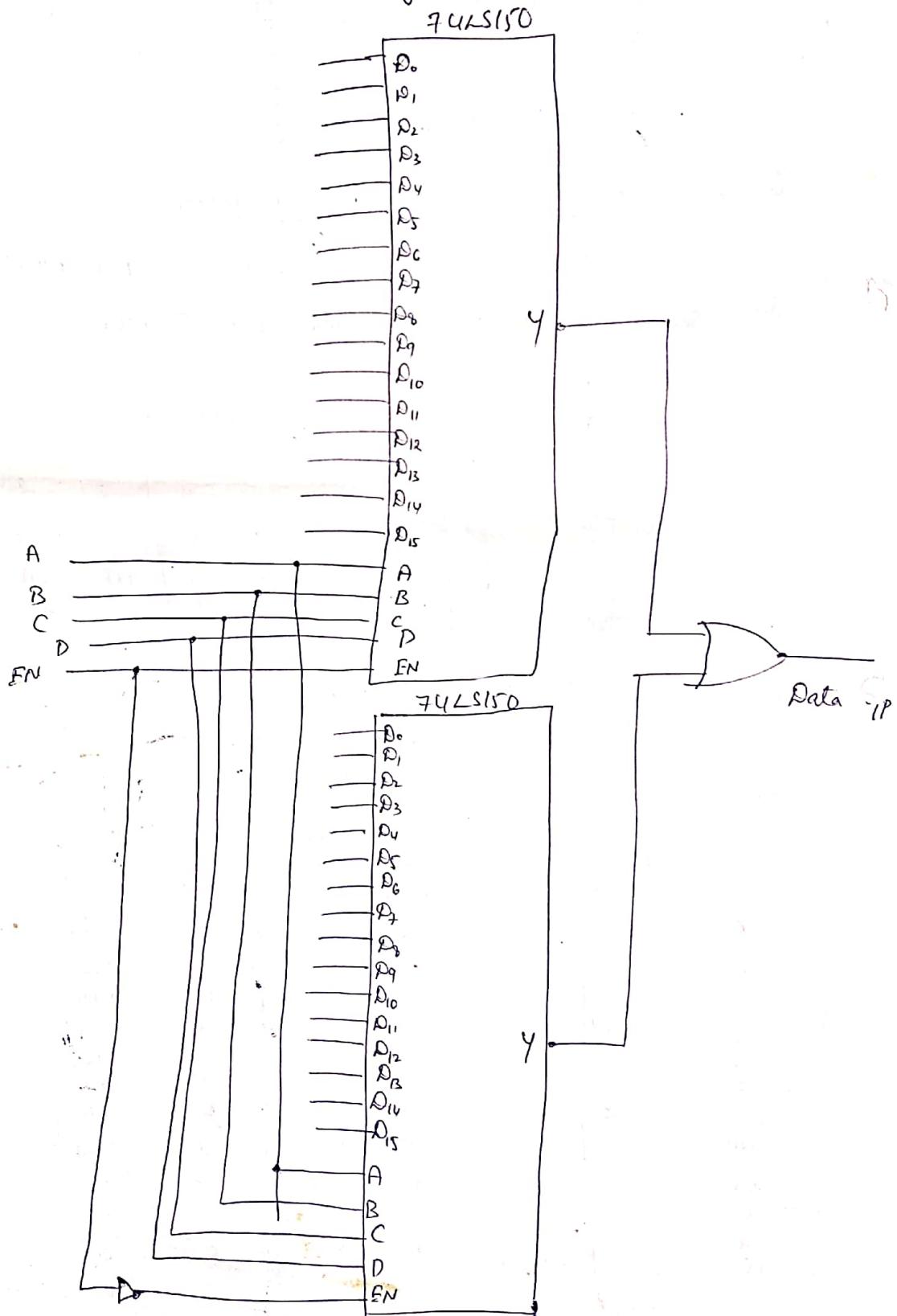
Truth Table

IEN	2EN	B	A	1A	1B	2A	2B	1D ₀	2D ₀
0	0	0	0	1	0	1	0	1D ₀	2D ₀
0	0	0	1	0	1	0	1	1D ₁	2D ₁
0	0	1	0	0	1	0	1	1D ₂	2D ₂
0	0	1	1	0	1	1	0	1D ₃	2D ₃
0	1	0	0	1	0	0	1	1D ₀	0
0	1	0	1	0	1	1	0	1D ₁	0
0	1	1	0	0	1	0	1	1D ₂	0
0	1	1	1	0	1	1	0	1D ₃	0
1	0	0	0	1	0	0	1	0	2D ₀
1	0	0	1	0	1	0	1	0	2D ₁
1	0	1	0	1	0	1	0	0	2D ₂
1	0	1	1	1	0	1	0	0	2D ₃
1	0	1	1	1	1	1	0	0	2D ₃

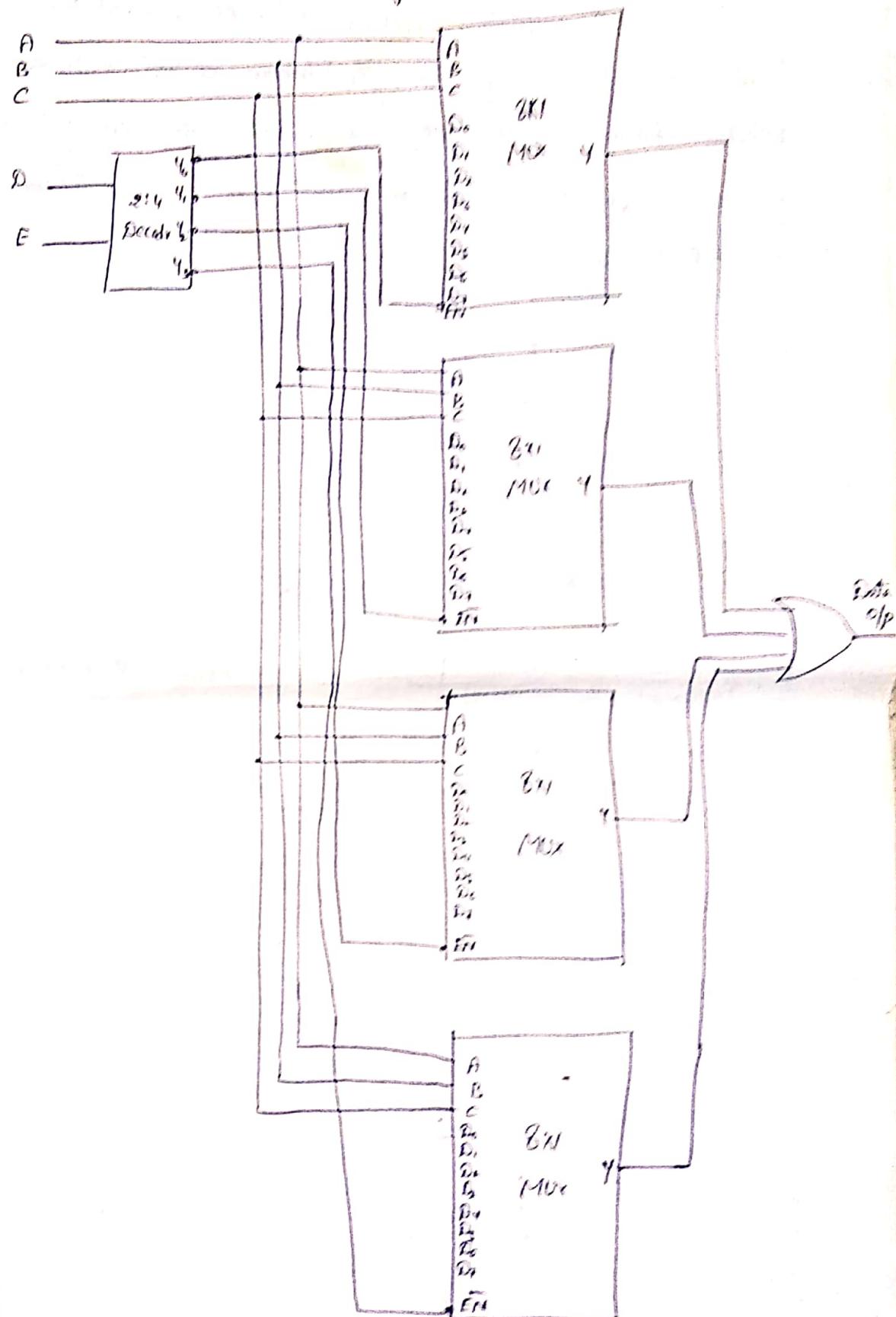
Higher Order Multiplexers

It is possible to expand the range of inputs for multiplexer beyond the available range in the integrated circuits. This can be accomplished by interconnecting several multiplexers.

→ Design 32 to 1 mux using two 16 to 1 MUX.



Design 32 to 1 Mux using 8x1 MUX

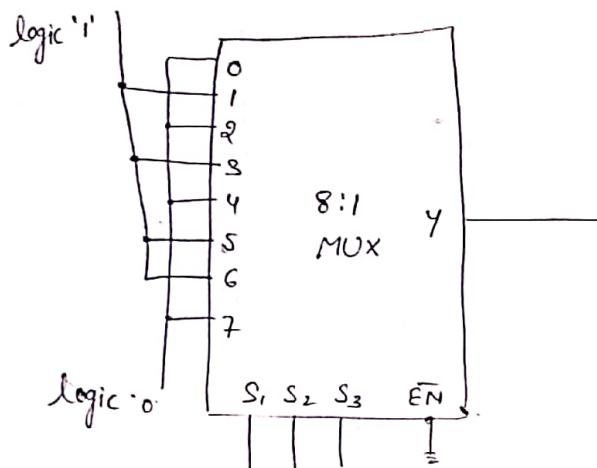


Multiplexers as a function generator :

A multiplexer consists of a set of AND gates whose outputs are connected to single OR gate. Because of this construction any Boolean function in a SOP form can be easily realized using multiplexer.

→ Implement the following Boolean function using 8:1 multiplexer.

$$F(A, B, C) = \sum m(1, 3, 5, 6).$$

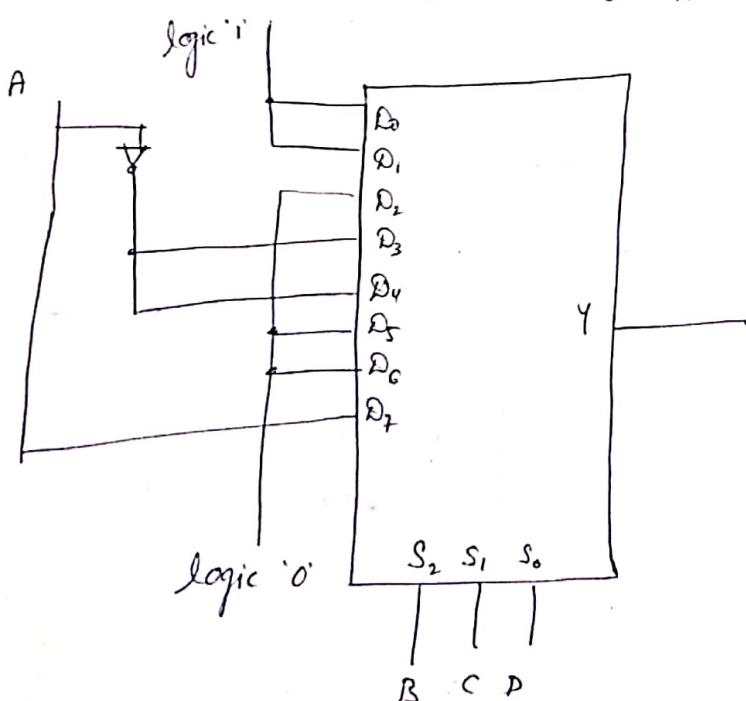


→ Implement the following Boolean function using 8:1 MUX

$$F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15).$$

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
\bar{A}	(0)	1	2	(3)	4	5	6	7
A	(8)	(9)	10	11	12	13	14	(15)

1 1 0 \bar{A} \bar{A} 0 0 A



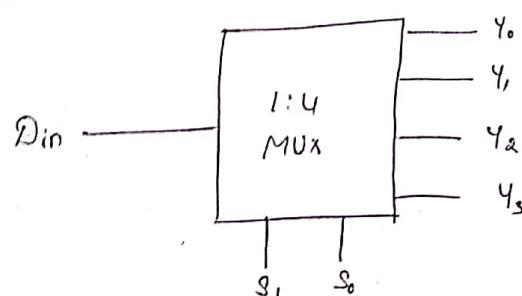
2: Multiplexer

A demultiplexer is a circuit that receives information on a single line and transmits this information on one 2^n possible output lines. The selection of specific output line is controlled by the values of 'n' selection lines.

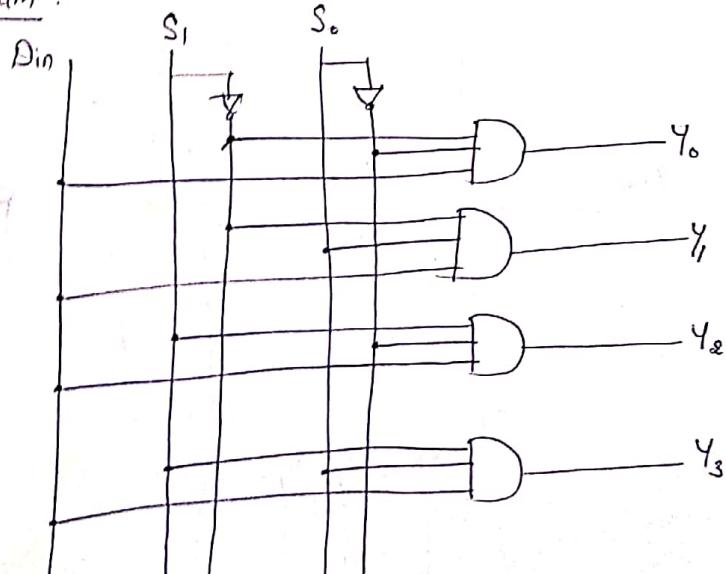
Function table:

Enable	S ₁	S ₀	Din	Y ₀	Y ₁	Y ₂	Y ₃
0	x	x	x	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	1	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1

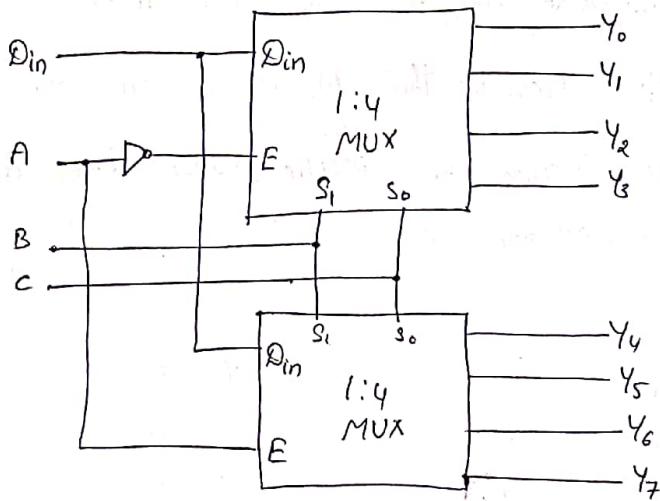
Block Diagram:



Logic Diagram:



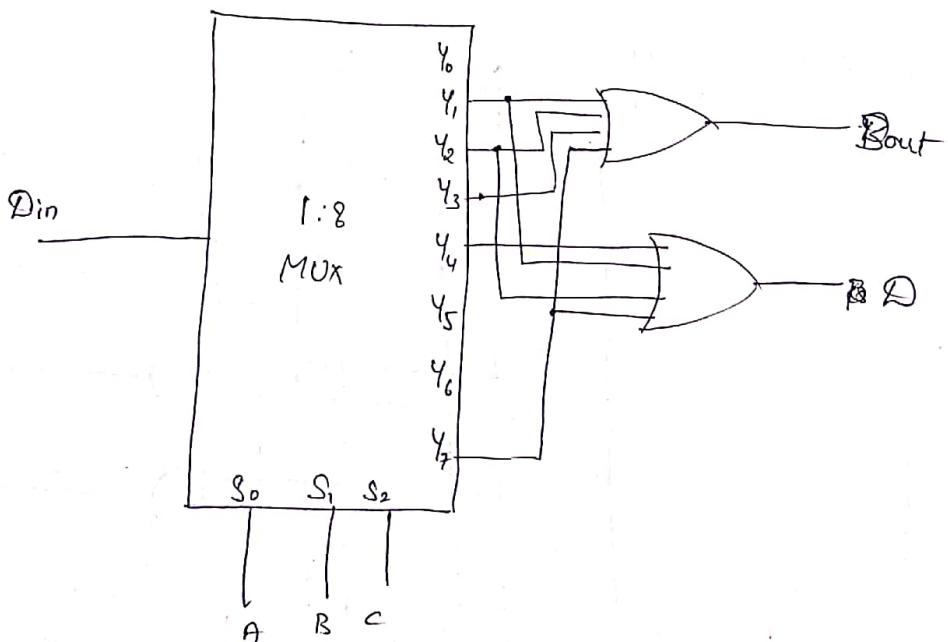
→ Design 1:8 demultiplexer using two 1:4 demultiplexers.



→ Implement full Subtractor using Demultiplexer.

A	B	C	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

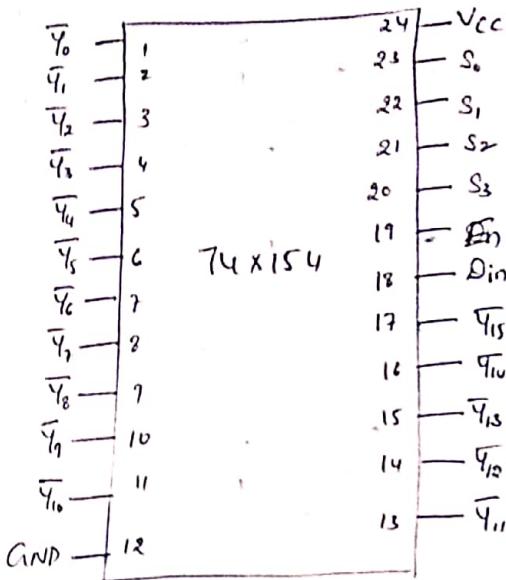
$$D = \sum_m (1, 2, 4, 7) ; \quad B_{out} = \sum_m (1, 2, 3, 7)$$



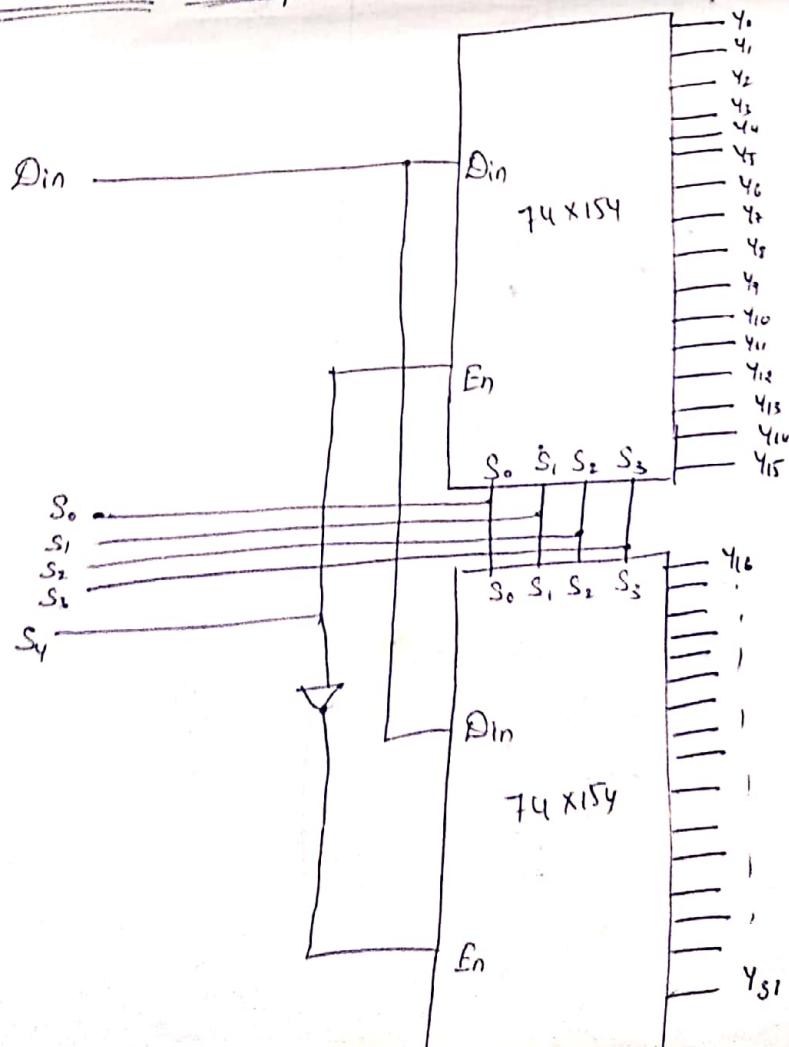
Higher Order Demultiplexing :

1 X 16 Demultiplexer (IC 74x154) :

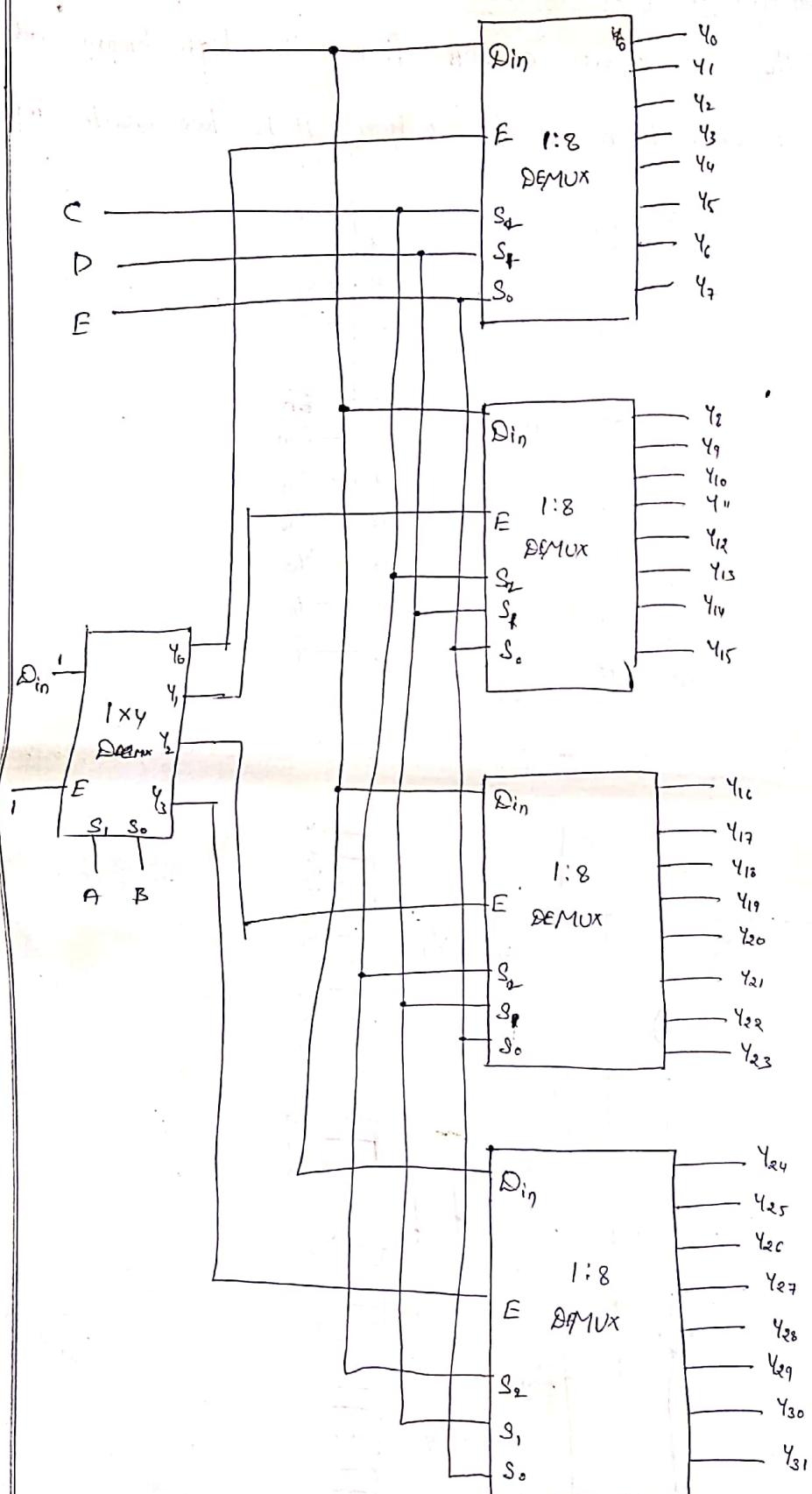
The IC 74x154 accepts four active high binary address inputs and provides 16 active low outputs. It has two enable inputs.



1 X 32 Demultiplexer using 74x154 :



→ 1x32 Demultiplexer using 1x8 Demux & 1x4 Demux.



UNIT-5

- Multiplexer is a digital switch. It allows digital information from several sources to be routed onto a single output line. It is having 2^n inputs & one output line.
- Demultiplexer is a digital circuit which sends data from one line can be sent on to any one of many line.
- Encoders is a logic circuit used to convert one form of data into binary form.
- Decoders converts binary data into other form i.e., decimal, octal, hexa-decimal etc.
- Priority encoder is an encoder circuit that includes the priority function. In priority encoder, if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.
- Code converters are used to convert one form of code into another form.