HA simple code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity HA is
   Port ( a : in  STD_LOGIC;
          b : in  STD_LOGIC;
          s : out  STD_LOGIC;
          c : out  STD_LOGIC);
end HA;

architecture Behavioral of HA is



component XOR22 is
   Port ( x : in  STD_LOGIC;
          y : in  STD_LOGIC;
          z : out  STD_LOGIC);
end component;
component AND22 is
   Port ( P : in  STD_LOGIC;
          q : in  STD_LOGIC;
```

```
        r : out  STD_LOGIC);
end component;
begin
U1:XOR22 port map(a,b,s);
U2:AND22 port map(a,b,c);
end Behavioral;
```

XOR code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity XOR22 is
   Port ( x : in  STD_LOGIC;
          y : in  STD_LOGIC;
          z : out  STD_LOGIC);
end XOR22;

architecture Behavioral of XOR22 is
begin
z<= x xor y;
end Behavioral;
```

AND CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity AND22 is
    Port ( P : in  STD_LOGIC;
           q : in  STD_LOGIC;
           r : out  STD_LOGIC);
end AND22;

architecture Behavioral of AND22 is

begin
r <= p and q;
end Behavioral;
```

HA testbench code:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;
```

```
ENTITY HAtb IS
END HAtb;

ARCHITECTURE behavior OF HAtb IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT HA
   PORT(
        a : IN  std_logic;
        b : IN  std_logic;
        s : OUT  std_logic;
        c : OUT  std_logic
       );
   END COMPONENT;


  --Inputs
  signal a : std_logic := '0';
  signal b : std_logic := '0';

            --Outputs
  signal s : std_logic;
  signal c : std_logic;
  -- No clocks detected in port list. Replace <clock> below with
  -- appropriate port name


BEGIN
```

```
        -- Instantiate the Unit Under Test (UUT)
  uut: HA PORT MAP (
       a => a,
       b => b,
       s => s,
       c => c
      );


  -- Stimulus process
  stim_proc: process
  begin
    a <='0'; b<='1';
            wait for 100 ns;
            assert s<='1'report"error in logic";
            assert c<='0'report"error in logic";
            wait for 10 ns;
            a<='1'; b<='1';
            wait for 100 ns;
            assert s<='0'report"error in logic";
            assert c<='1'report"error in logic";
            wait for 100 ns;
            wait;
  end process;

END;
```