II B. Tech. II Semester Supplementary Examinations – October, 2023

Computer Architecture and Organization

Time: 150 Min (CSE) Max. Marks: 80M

# SECTION – A

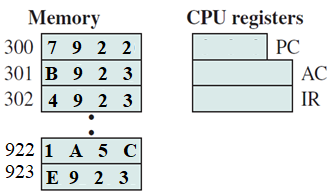
**Answer all Four questions 4×10M=40M**

1. Consider a hypothetical machine having both instructions and data are 16 bits long and have instruction format as below.

Assume the list of opcodes as follows:

|  |  |
| --- | --- |
| 0111 | Load AC from memory |
| 0100 | Store AC to memory |
| 1011 | Subtract to AC from memory |
| 1000 | Load IOBR from memory |
| 0001 | Store IOBR to memory |

Depict an Instruction Cycle with all the necessary steps for the execution of a Subtraction operation of two 16-bit data using above mentioned opcode characteristics, The initial content of Memory and CPU registers are shows below.



1. (a) Contrast the drawbacks of Programmed I/O and Interrupt-Driven I/O Techniques. Illustrate the solution to overcome the drawbacks.

(b) Show mechanism for the DMA controller sharing the CPU’s memory bus.

3. Develop an algorithm to evaluate the given arithmetic statement using

1. a general register computer with three address instructions
2. a general register computer with two address instructions
3. using an accumulator type computer with one address instruction.
4. using a stack organized computer with zero address instruction.

X = [ B + C \* (D + E) ] / [ F \* (G + H)]

4. (a) Depict a hardware for Priority interrupt for 8 different set of Memories/IO. Use below

set of Memories/Interrupts.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| RAM | USB | Camera | DDR | Keyboard | Printer | ROM | Flash |

(b) Develop an algorithm to illustrate the Two Asynchronous data transfer mechanisms. Justify why Handshaking mechanism is preferable?

**SECTION – B**

**Answer all Two questions 2×20M=40M**

5. a) Develop an algorithm to convert the Decimal numbers to its equivalent Sign-Magnitude and Two’s complement representation using Flow chart. Verify the developed algorithm by taking Two decimal numbers in the range of -32 < N < +32 and convert to its Sign magnitude and Two’s complement.

(b) Design an algorithm for the Multiplication of Two Signed numbers. Verify the developed algorithm by taking Two Signed numbers taken earlier in part (a).

6. (a) Illustrate Direct mapping Cache organization for a memory system. Also, articulate Hit ratio, Cache size, Block size, Tag size and Address length with respect to Direct mapped Cache organization.

(b) Design an example of a Direct Mapped cache with block size of 8 words.

(c) Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Conclude the values of (i) Number of bits in tag, (ii) Tag directory size.