Y. Sai Lakshmi
19131A04K9
ECE - 4

VLSI Testing & Testability

Assignment - 2

1. Explain the basic concept of Self checking checkers?

(A) * It may be possible to determine from the outputs of a circuit C whether a certain fault f exists within the circuit without knowing the value of expected response. This type of testing which can be performed "on-time" is based on checking some invariant properties of Response.

* It is necessary to test explicitly for f, and the circuit is said to be self-checking for f. Another circuit, called a "checker" can be designed to generate an Error signal whenever the outputs of C indicate the presence of faults within C.

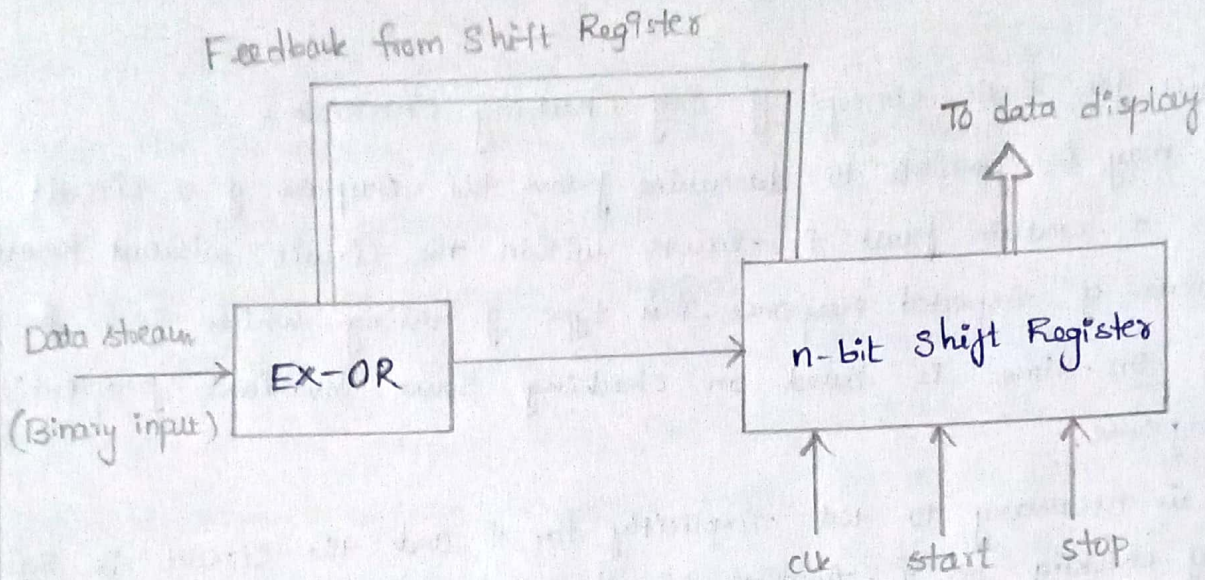
* For an arbitrary combinational circuit with p inputs and q outputs all 2^p input combinations can occur as can all 2^q possible output combinations. If all possible output combinations can occur, it is impossible to determine whether a fault is present by just observing the outputs of the circuit.

* If only $k < 2^q$ output configurations can occur during normal operation, the occurance of any of $2^q - k$ other configuration, indicates a malfunction. Thus, faults that result in such an illegal output can be detected by hardware checker.

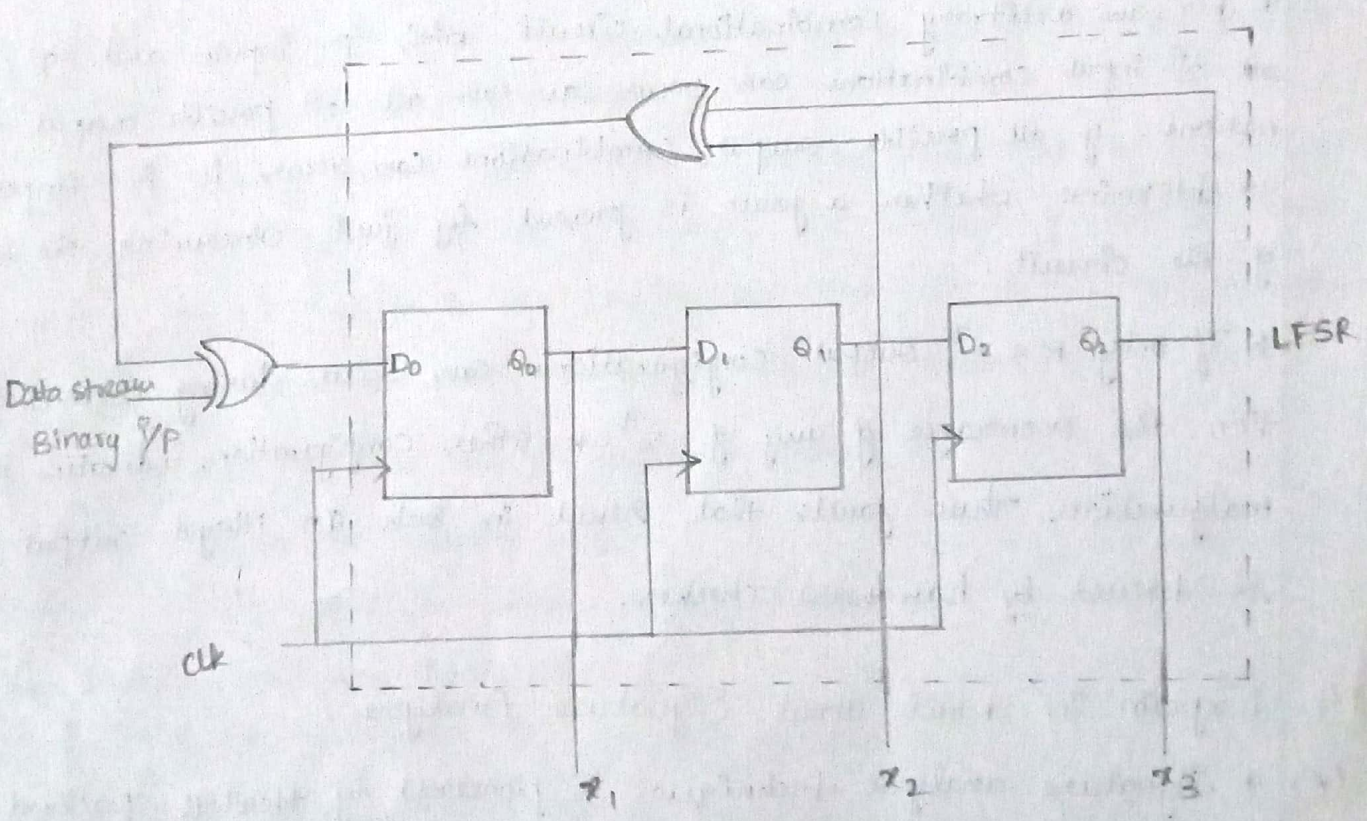
4. Explain in detail about Signature Analysis?

(A) * Signature analysis technique is pioneered by Hewlett-Packard Ltd. It detects Errors in data streams caused by hardware faults. It uses a data compaction technique to reduce long data streams into a unique code called Signature.

* Signatures can be created from the data streams by feeding that data into an n-bit. It is formed by adding an extra XOR gate at the input of LFSR.



(a) Signature analyzer circuit.



* A signature can also be obtained by feeding a subset of the output sequence in parallel when a multiple input signature register (MISR) is used.

3a) Explain about various RAM fault Models?

(A) * The memory array consists of individual memory cells arranged in array of rows and columns. In this, there are 2^n rows and 2^m columns, Each row is called word line and Each column a bit line.

Faults in the address decoder can result in following

1. No memory location is accessed
2. An undesired location is accessed
3. More than one location are accessed simultaneously.

* A defect in the memory array can manifest itself as a single fault (Stuck at/stuck-open fault, transition fault), or as a fault that corrupts a memory cell that corrupts another cell. The latter type of fault is known as a coupling fault.

* A memory cell is said to be stuck-at-0 (or 1) if the value of the cell cannot be changed from its current logical value. A memory cell is stuck open if it cannot be accessed.

* A pair of memory cells P and q may be coupled such that a transition from 0 to 1 (1 to 0) in cell p changes the content of cell q from 1 to 0 (0 to 1); cell P is the coupling cell and cell q is coupled cell. the coupling between two cells results in coupling fault.

* A coupling fault can be one of following types:

1. Inversion coupling fault
2. Idempotent or State coupling fault.

* An inversion coupling fault results if a 0 to 1 or a 1 to 0 write operation into cell p inverts the contents of cell q.

* An idempotent coupling fault occurs if a write operation into cell P forces the content of cell q to be 0 or 1, cell q is said to be static coupled to cell P.

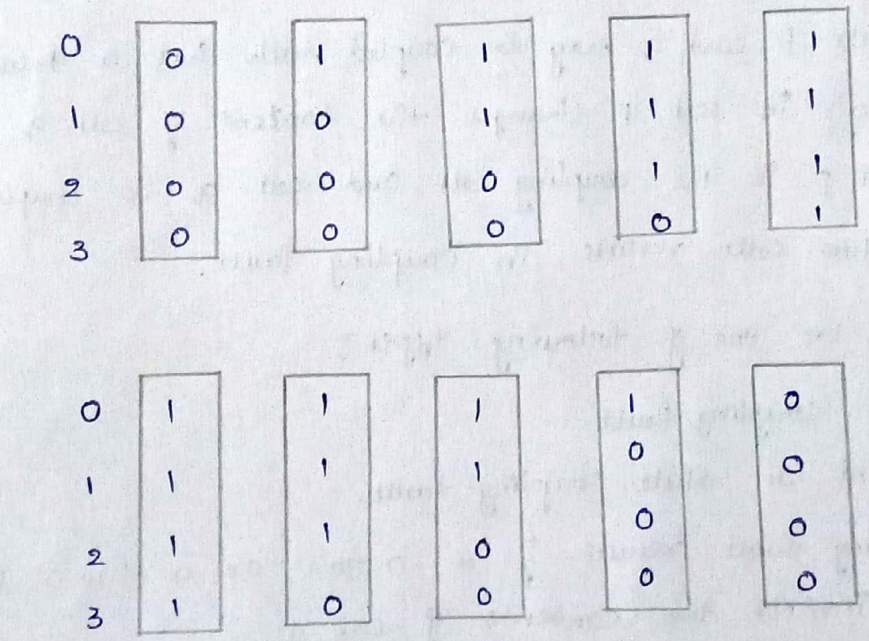
* A memory cell is said to exhibit pattern sensitivity if its content changes by a pattern of 0s and is a transition from a 0 to a 1 - or vice-versa in its adjacent memory cells. Pattern sensitivity can be represented by a static or a dynamic fault model.

3b) Explain about the March Test ?

(A) * The March test technique proposed by Nair and later implemented by Suk and Reddy, initializes the memory locations with 0s. then, Each memory location is read in ascending order to check if it contains a 0; a 1 is then written into it.

* Once, the read/write process is complete, Each location is accessed in descending order to check that it contains a 1 and then a 0 is written into it.

* the Execution time of the algorithm is of order N.



March pattern

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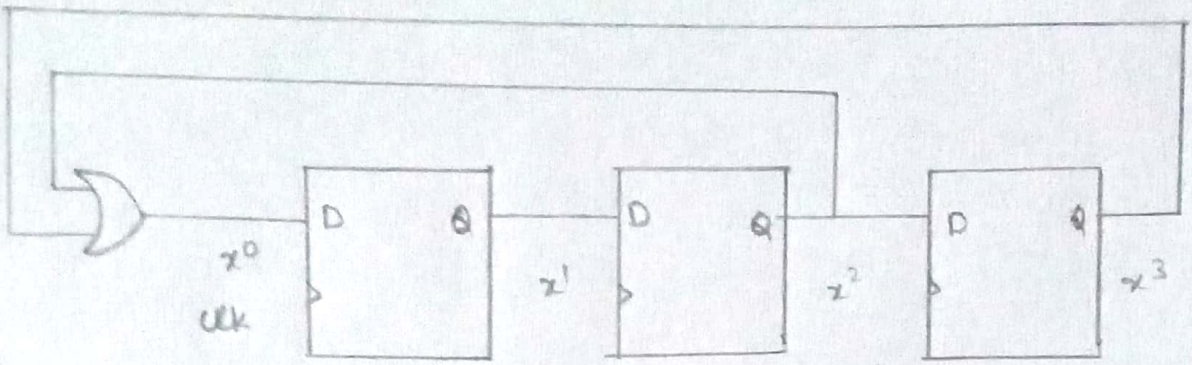
(2) Design a LFSR for the following polynomial $1+x^2+x^3$.

(A)



for $1+x^2+x^3$

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