

## **KIRAN KOTHOU**

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### **CAREER OBJECTIVE:**

Looking for a challenging role to utilize my technical, logical and management skills effectively and efficiently for the growth of the organization as well as to enhance my knowledge in the new and trending practices of the Industry.

### **PROFESSIONAL TRAINING:**

Role : Physical Design Engineer trainee SUMEDHA IT, HYDERABAD. Duration : From July-23 to till date

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### **Core Knowledge:**

- Hands-on experience in complete RTL to GDS-II flow.
- Hands-on experience in complete placement and routing flow.
- Experience with Process nodes i.e 28nm
- Good Knowledge in Floor plan, Power plan, Clock Tree Synthesis, Routing, and STA.
- Hands-on experience in complete back end flow – Logical Synthesis, Floor Planning, Placement, CTS and Routing.
- Hands-on experience in TCL scripting

### **Technical Skills:**

Programming Languages	: TCL (scripting language).
Technical Knowledge	: Synthesis & PNR
Operating System	: Linux, Windows
Tools/Packages	: DC-SHELL, ICC-II
MS Office	: Word, PowerPoint and Excel

### **Projects Experience:**

#### **BLOCK 1**

- \* Tools – DC\_SHELL, ICC2
- \* Description : Block Level Implementation
- \* Duration : 2 months
- \* Technology Node : 28nm TSMC
- \* Instance Count : 68k
- \* Frequency : 400MHz
- \* Macros : 6
- \* Number of Clocks : 1
- \* Metal Layers : 9

### **Challenges:**

1. Rectangular floor plan with lots of congestion and utilization of around 75%
2. Sufficient channel spacing provided around macro to avoid congestion and routing issues.
3. Resolving floating wires
4. Fixing timing violation after placement and routing stages.

## **BLOCK 2**

- \* Tools –DC\_SHELL
- \* Description : Block Level Implementation
- \* Duration : 1 Month
- \* Technology Node : 28nm TSMC
- \* Instance Count : 442
- \* Frequency : 100MHz
- \* Number of Clocks : 3

### **Challenges:**

1. Design constraints like clocks, input delay, output delay, clock uncertainty for design under analysis.
2. Sanity checks performed after synthesis.
3. Optimizing the design with respect to performance.
4. Understanding the reasons for violations.

### **Work Experience:**

Company : Eight Audio International Pvt.Ltd  
Role : Technical Assistant  
Experience : From 09 june, 2019 to 10 may, 2023

### **EDUCATION:**

- ☞ Bachelor of Technology in Electronics and Communication Engineering with Aggregate marks /CGPA – 55% in 2022
- ☞ ACE Engineering College
- ☞ 08/2015 - 05/2018, Ghatkesar
- ☞ Diploma in ECE with 58%,EDUCATION
- ☞ TKR Engineering College
- ☞ 08/2011 - 04/2014, R.N. Reddy
- ☞ 10th Class with Aggregate marks /CGPA - 68
- ☞ Divya Jyothi High School
- ☞ 05/2010 - 03/2011, Ramanthapur

### **DECLARATION:**

I hereby declare that the above stated information is true to the best of my knowledge and belief.

Kiran kothoju

Place :  
Date :