# Organizacija računalnikov

## 1. Neobvezna Domača Naloga - MiMo model CPE

December, 2020

Avtor: Kiril Tofiloski, 63190385

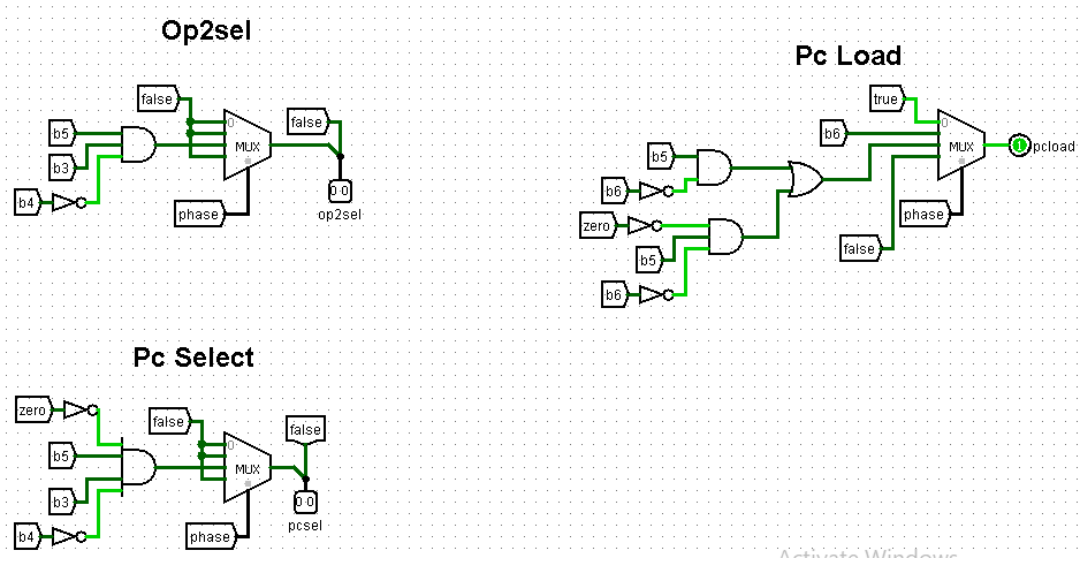
Za neobvezno domačo nalogo sem se odločil za trdo žično različico našega  MiMo modela procesorja.

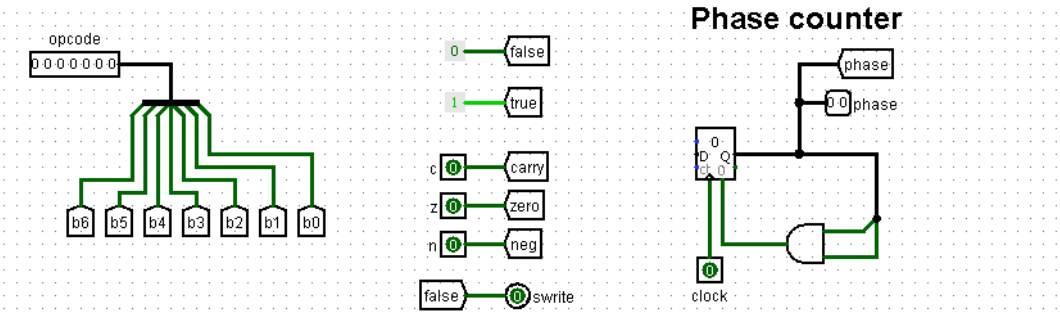
Dizajn sem zasnoval na primeru trdo žičnega procesorja, podanem na https://minnie.tuhs.org/CompArch/Tutes/week03.html

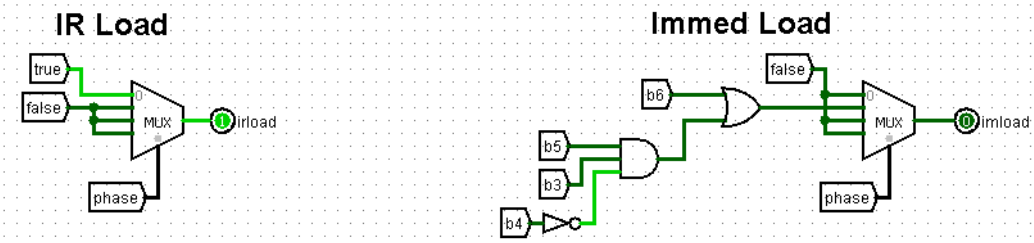
Odločil sem se, da ustvarim logiko na podlagi že implementiranega zbirnika, saj nisem imel dovolj časa za pisanje novega prevajalnika.

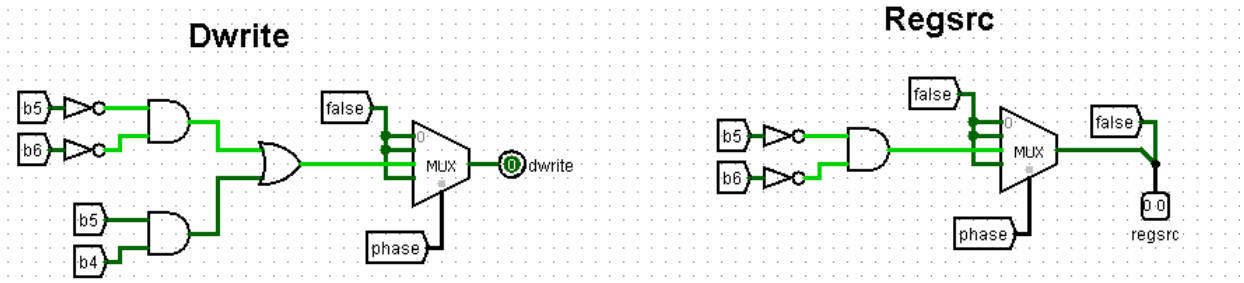
Ustvaril sem logiko, tako da lahko naslednji ukazi delujejo:

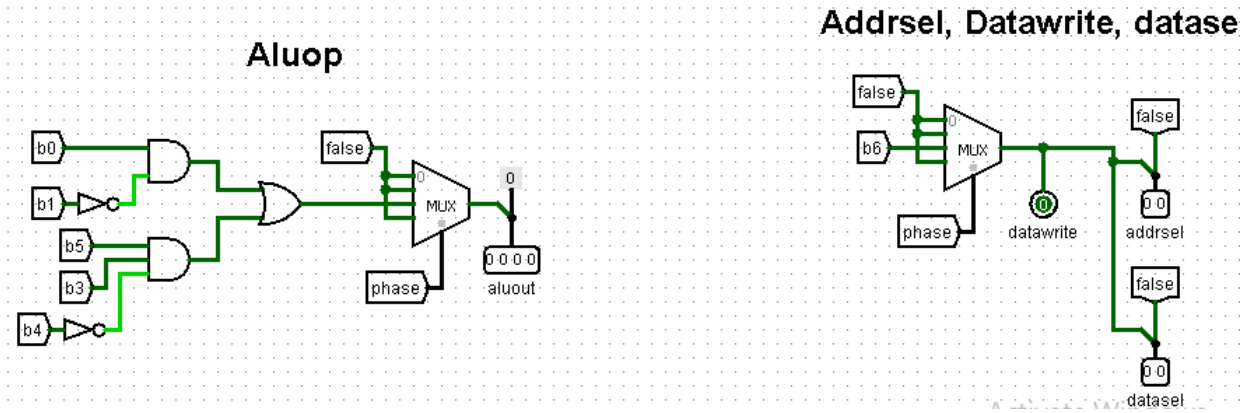
```
# add Rd,Rs,Rt
0:      aluop=add  op2sel=treg  dwrite=1  regsrc=aluout, goto fetch
# sub Rd,Rs,Rt
1:      aluop=sub  op2sel=treg  dwrite=1  regsrc=aluout, goto fetch
# JNEZ Rs,Immed  ; If Rs != 0, PC <- immed else  PC <- PC + 2
40:     addrsel=pc  imload=1
        aluop=sub  op2sel=const0, if z then pcincr else jump
# li Rd,Immed    ; Load immediate Rd, immed
63:     addrsel=pc  dwrite=1  regsrc=databus, goto pcincr
# sw Rd,Immed    ; Store Rd into M[immed] Rd->M[immed];
65:     addrsel=pc  imload=1
        addrsel=immed  datawrite=1  datasel=dreg, goto pcincr
```




opcode
0 0 0 0 0 0 0
b6
b5
b4
b3
b2
b1
b0
0
false
1
true
c
carry
z
zero
n
neg
false
swrite
Phase counter
phase
0 0
phase
D
Q
clock


IR Load
true
false
MUX
irload
phase
Immed Load
b6
b5
b3
b4
false
MUX
imload
phase


Dwrite
b5
b6
b5
b4
false
MUX
dwrite
phase
Regsrc
b5
b6
false
MUX
false
phase
0 0
regsrc


Aluop
b0
b1
b5
b3
b4
false
MUX
0
phase
0 0 0 0
aluout
Addrsel, Datawrite, datase
false
b6
MUX
phase
datawrite
false
0 0
addrsel
false
0 0
datasel

Procesor sem preizkusil z naslednjim programom, ki pravilno oddaja.

trdozicen_programa.s

```
main:   li r1, 5            #comment
        li r2, 5
        add r1, r1, r2
        li r3, 3
        sub r1, r1, r3
        sw r1, 20
        jnez r4, 01
        jnez r1, 30
```