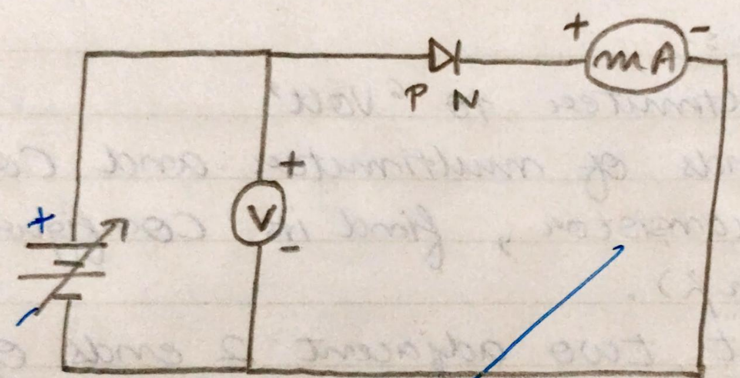
Experiment No. ⇒ 1(b)

Aim :- Plot and analyze the forward & reverse characterstic of PN junction Si & Ge & determine the knee and breakdown Voltage.

Apparatus :- A PN junction diode kit, power supply, Connecting leads.




Forward Biasing.

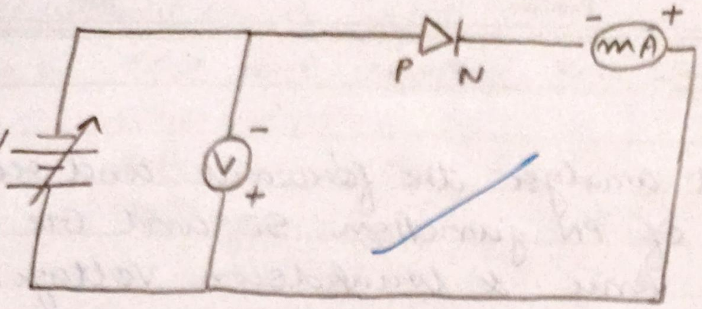
Experiment No :-

Aim :- Plot and analyse the forward and reverse characterstics of PN junction Si and Ge & determine the knee & breakdown voltage.

Apparatus :- A PN junction diode kit, power supply, Connecting ~~loads~~ leads.

Theory :- A diode is a two terminal device with P & N sides, ~~respectively~~ representing the positive & negative terminals which conducts in one direction and stops the conduction in other.

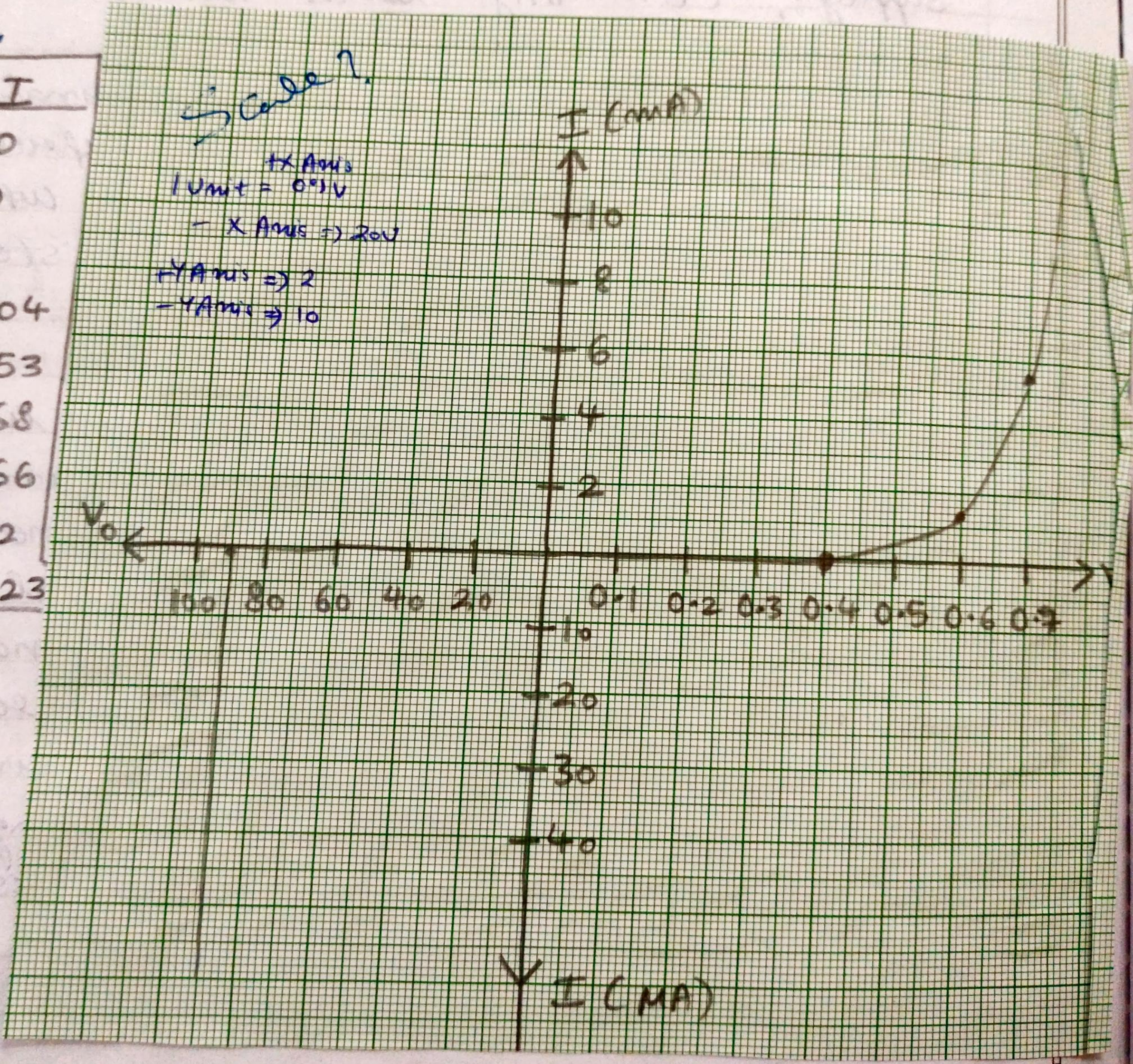
- Forward Bias :- A diode is said to be in forward biased when positive terminal of external voltage source is connected to anode (P) and negative terminal of source to N side which results in the narrowing of depletion region due to a reduction in the positive charge at the junction. The narrow depletion region along with a very small potential barrier results in a very low resistive path and diode behaviour like a conductor in direction




Reverse
Forward
Biasing

| V | I |
|---|---|
| 0·1 | 0 |
| 0·2 | 0 |
| 0·3 | 0 |
| 0·4 | 0·04 |
| 0·5 | 0·53 |
| 0·6 | 1·68 |
| 0·7 | 5·66 |
| 0·8 | 13·2 |
| 0·9 | 19·23 |

Forward



of diode. The net diode current is given by :-

$$I_d = I_s \left(e^{kV_d/T_k} - 1\right)$$

where $I_s$ = reverse saturation current

- **Reverse Bias :-** A diode is said to be reverse biased when negative terminal of the battery is connected to anode and positive terminal is connected to cathode. The reverse biasing causes majority electrons in N-side and majority holes on P-side to move away from junction. The width of the depletion region greatly increases and barrier voltage rises. It represents a high impedance path and diode behaves like an insulator.

# Procedure :-

(1.) Connect the digital PN junction diode trainer kit to the power.

(2.) Connect the circuit as per the circuit diagram.

?

| V | I |
|---|---|
| 0 | 0 |
| 10 | 0 |
| 20 | 0 |
| 30 | 0 |
| 40 | 0 |
| 50 | 0 |
| 60 | 0 |
| 70 | 0 |
| 80 | 0 |
| 90 | — |

Reverse Biasing

Result :-

(1.) The Knee Voltage for Si is 0.7V

(2.) The Knee Voltage for Ge is 0.3V

• **For forward Bias :-**

(1.) Connect the positive terminal of the voltage source to the anode of the diode and negative terminal to cathode of diode.

(2.) Connect the voltmeter in parallel to diode and ammeter in series to diode.

(3.) Vary the regulated power supply voltage in steps of 0.1 V, upto 1V.

(4.) Record all observations in a table & plot the VI characterstics of forward bias.

• **Reverse Bias :-**

(1.) Connect the negative terminal of voltage source to the anode of diode and positive terminal to cathode of diode.

(2.) Connect the voltmeter in parallel to diode and ammeter in series to diode

(3.) Vary the regulated power supply voltage in steps of 10V upto 90 V.

(4.) Record all observations in table and plot the VI characterstic of reverse bias.

# Result :-

(1.) The Knee Voltage for Si is 0.7V

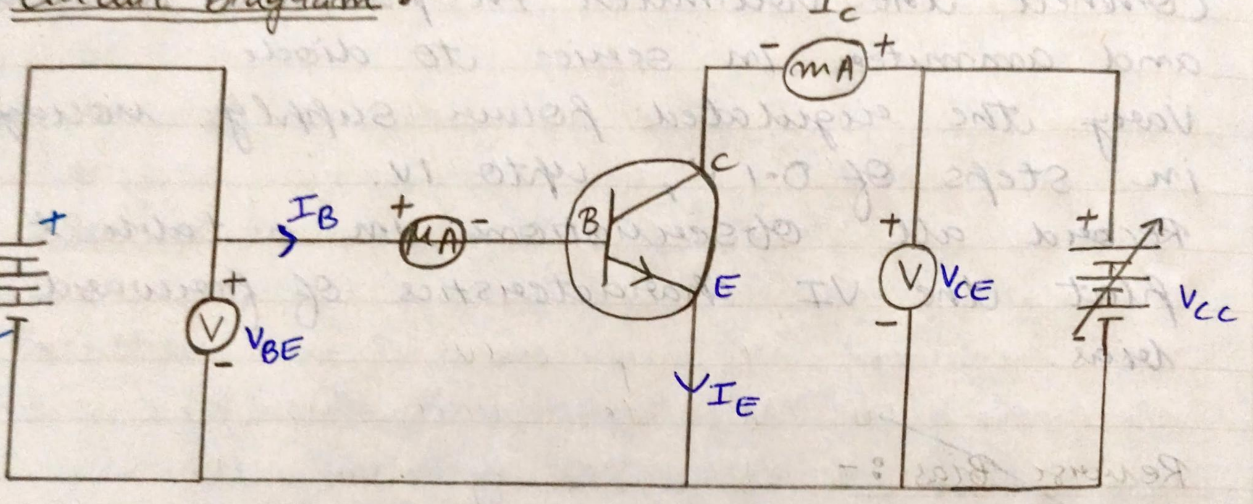
(2.) The Knee Voltage for Ge is 0.3V

Teacher's Signature ____

**Aim** :- To plot input and output characteristics of transistor in CEC configuration.

**Apparatus** :- Regulated ~~Power~~ supply, DC Voltmeter, DC multimeter, DC micrometer and connecting wires

**Circuit Diagram** :-




**Observation Table** :-

**Input Characteristics** :-

$V_{CE} = 2V$

| $V_{CB}$ | $I_B$ (μA) |
|---|---|
| 0.436 | 0.0 |
| 0.5 | 0.4 |
| 0.6 | 10.9 |
| 0.7 | 55.6 |
| 0.8 | 142.6 |
| 0.9 | — |

$V_{CE} = 4V$

| $V_{CB}$ | $I_B$ (μA) |
|---|---|
| 0.46 | 0.1 |
| 0.5 | 0.3 |
| 0.6 | 9.4 |
| 0.7 | 57.1 |
| 0.8 | 136.5 |
| 0.9 | — |

$V_{CE} = 6V$

| $V_{CB}$ | $I_B$ (μ |
|---|---|
| 0.46 | 0.1 |
| 0.5 | 0.3 |
| 0.6 | 9.8 |
| 0.7 | 60.4 |
| 0.8 | 130 |
| 0.9 | — |

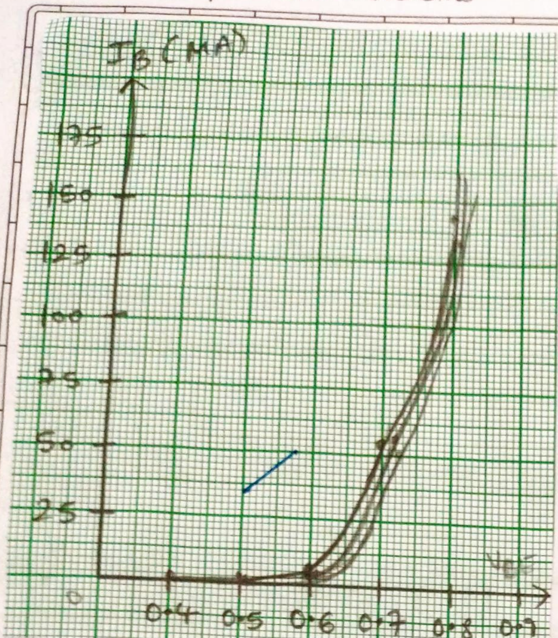
**Aim:-** To plot input & output characteristics of transistor in CEC (common emitter configuration).

**Apparatus:-** Regulated power supply, DC, Voltmeter, DC multimeter, DC micrometer and connecting wires.

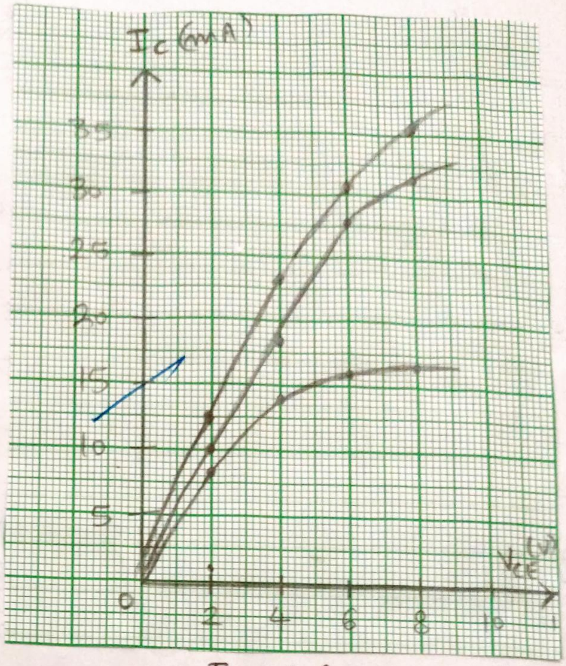
**Theory:-** In CEC configuration, input is connected b/w base and emitter while the ~~input~~ output is taken b/w collector and emitter. The emitter is common to input and output circuit. In this configuration, voltage is applied b/w collector and emitter base-emitter base junction is forward biased then the base is made more positive than the emitter by $V_{BE}$, collector by use $V_{BE}$. The value of $V_{CE}$ is greater than $V_{BE}$. In this circuit $I_A$ flows in input & $I_C$ flows in output circuit. In this arrangement circuit gain between input and output sides is obtained, since input resistance is again less than output resistance.

**Procedure:-** (i) Connect the given circuit as shown.
(2) Note reading in input characteristics by changing regulator.

Input Characteristics




Output Characteristics




Output Characteristics

$I_B = 0.6$

| $V_{CE}$ | $I_C$ (mA) |
|---|---|
| 2 | 1.8 |
| 4 | 1.4 |
| 6 | 1.9 |
| 8 | 2.0 |

$I_B = 0.7$

| $V_{CE}$ | $I_C$ (mA) |
|---|---|
| 2 | 8.7 |
| 4 | 14.7 |
| 6 | 15.6 |
| 8 | 16.7 |

$I_B = 0.8$

| $V_{CE}$ | $I_C$ (mA) |
|---|---|
| 2 | 8.9 |
| 4 | 17.6 |
| 6 | 28 |
| 8 | 31.6 |

# Result :-

(A) Input Characteristics :-

The curve drawn b/w $I_B$ & $V_{CE}$ for given value of collector emitter voltage $V_{CC}$ is known as input characteristics.

(B) Output Characteristics :-

It is for common ~~emm~~ emitter transistor, the curve drawn b/w collector current $I_C$ & $V_{CC}$ given value of $I_B$.

(3) Move switch on $V_{CE}$ and note down the reading by changing regulator.

(4) Now for output characteristic turn on the reading by changing regulator. Switch and

(5) Set 100 μA on connector.

(5) Note down the reading of $I_C$ and $V_{CE}$ by changing regulator.

(6) Now set the ammeter to 150 μA and note down the reading by changing regulator.

(7) Now draw graph with different set of reading.

# Precautions :-

(1) Connection should be tight and as shown.

(2) Switch off Power supply when not in use.

# Result :-

(A) Input Characterstics :-

→ The curve drawn b/w $I_B$ and $V_{CE}$ for given value of collector emitter voltage $V_{CE}$ is known as input characterstics.

(B) Output Characterstics :-

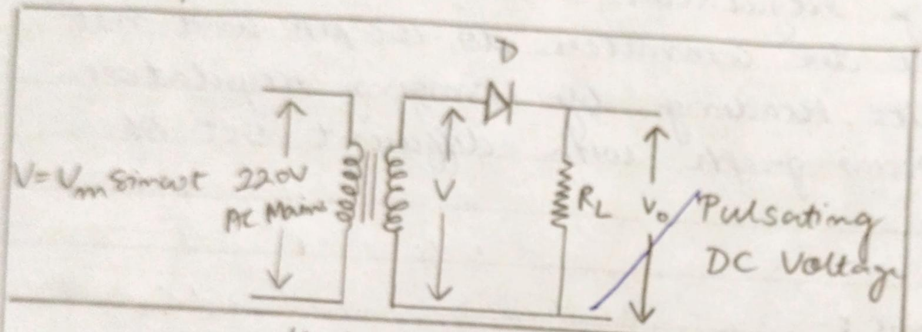
→ It is for common emitter transistor, the curve drawn between collector current $I_C$ and $V_{CE}$ gives value of $I_B$.

Teacher's Signature

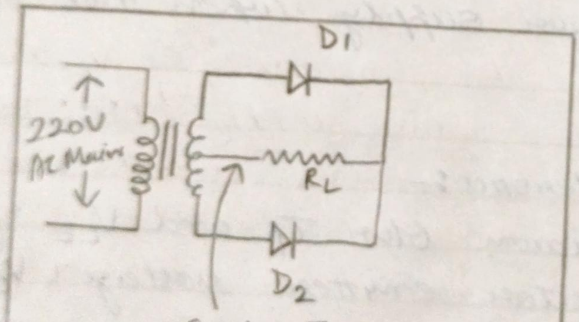
Exp. No. 3

**Aim:-** Study and observe the output waveform of half wave & full wave rectifiers on CRO & Calculate the average and RMS value of output Voltage

**Apparatus:-** Half Wave & full Wave rectifier kit, digital multimeter, Connecting wires, CRO, CRO probes




Half Wave Rectifier




Full Wave Rectifier

# Experiment No 3

**Aim** :- Study and observe the output waveform of half wave and full wave rectifiers on CRO and calculate the average and RMS value of output Voltage.

**Apparatus** :- Half Wave and full wave rectifier kit, digital multimeter, connecting wires, CRO, CRO probes.

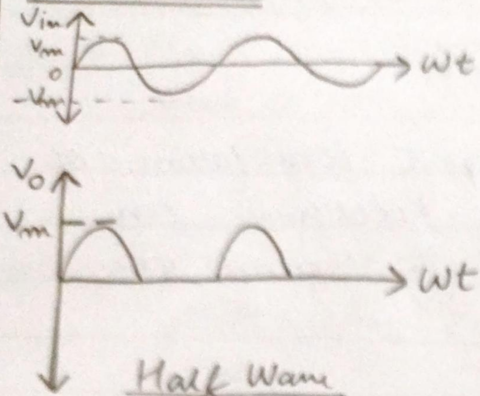
# **Theory** :-

- **Half Wave Rectifier** :-

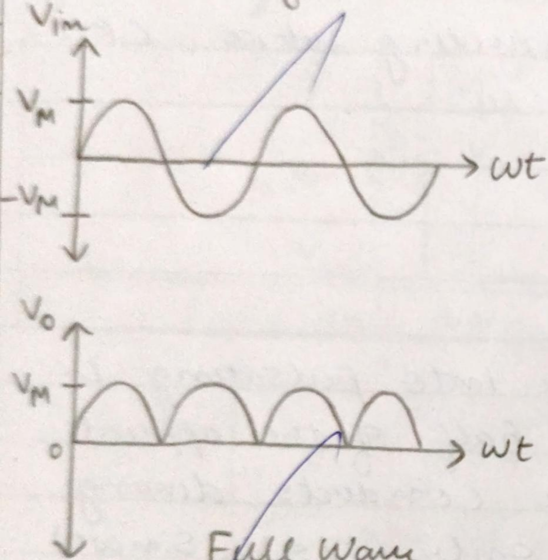
→ It converts AC voltage into pulsating DC voltage using only one half of the applied AC voltage. The rectifier conducts during one half of AC cycle only ($V = V_m \sin \omega t$) During +ve half input anode of the diode is positive w.r.t cathode. Hence, diode conducts in reverse biasing.
So the whole input voltage is across load resistance during -ve half of input, anode of the diode is -ve w.r.t cathode. Hence, diode does not conduct across load resistance, voltage drop is 0.

Teacher's Signature ____________

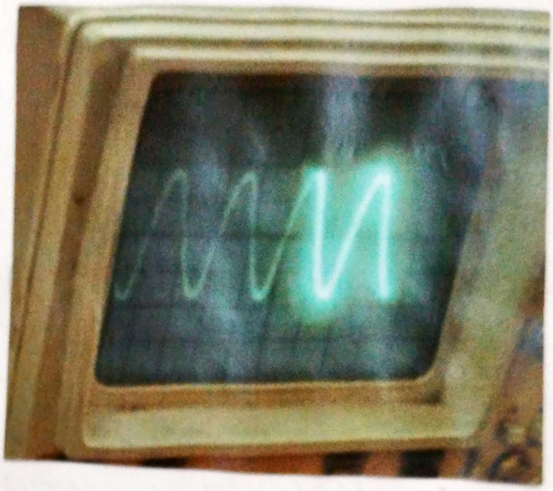
Observation :-

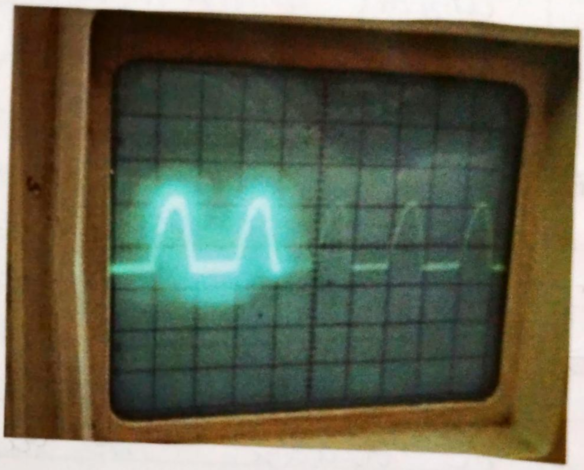


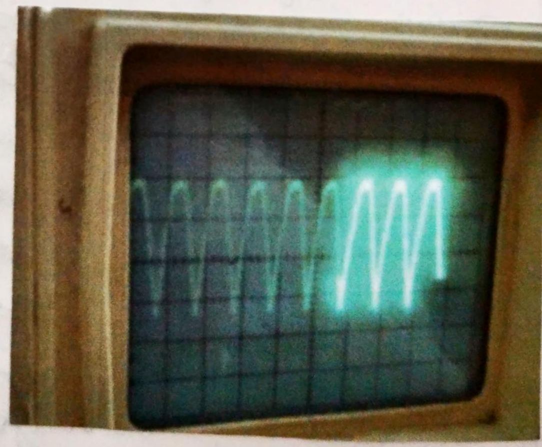

Half Wave Rectifier




Full Wave Rectifier







Result :- Output Waveform of half wave & full wave rectifier has been studied & Observed.

Expt. No. Page No. 13 Date

- Full Wave Rectifier :-

(A.) Centre - tapped :-
It uses 2 diodes of which one conducts during +ve half & other conducts during -ve half of input cycle.

(B.) Bridge Wave Rectifier :-
It uses 4 diodes. $D_1$ & $D_3$ conducts during +ve half and $D_2 - D_4$ conducts during -ve half of input voltage.

- Procedure :-

(1) Make the connections as shown in diagram of half wave and full wave rectifier.
(2) Now connect the CRO before diode to see the input waveform.
(3) Now connect the CRO after diode to see the output waveform (output of rectifier).
(4) Measure the $V_{in}$ (peak) and $V_{out}$ (peak).
(5) Now connect the filter (circuit with rectifier) and connect CRO after it to get output waveform.

- Result :-

Output waveform of half wave and full wave rectifier has been studied & observed.

Teacher's Signature ____

Experiment - 4

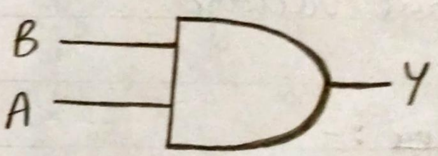
Aim :- Logic gate is a basic building block of a digital circuit. So verify the truth table of all the logic gates on trainer kit using TTL IC's

# Circuit Diagrams & Truth Table

- BASIC LOGIC GATES

(1) AND Gate :-

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



Experiment No:- ~~3~~4

**Aim:-** Analyse the truth table of various logic gates.

**Apparatus:-** logic gate kit, a power source and connecting wires.

**Theory:-**

- **Logic gates:-** In electronics, a logic gate is an idealized or physical device implementing a Boolean function; that is, it performs a logical operation on one or more logical inputs, and produce a single logical output. They are primarily implemented using diode or transistor acting as electronic switches.

There are 7 logic gates - AND, OR, NOT, NAND, X-OR & X-NOR. AND, OR, NOT are basic gates. NAND & NOR are universal gates as they can be converted into basic gates.

(1) **AND:-** The AND gate is a basic digital logic gate that implements logical conjunction - it behaves according to the truth table to the left. The output of AND gate is 'true' only

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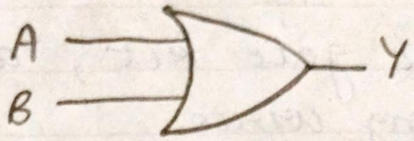
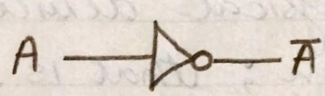
## (2) OR Gate :-

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



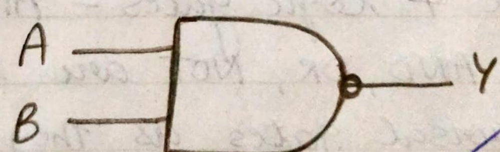

## (3) NOT Gate :-

| A | $\bar{A}$ |
|---|---|
| 0 | 1 |
| 1 | 0 |



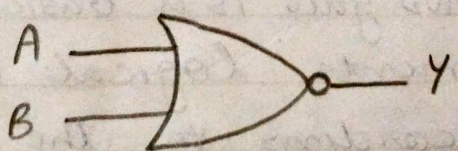

## (4) (A) NAND Gate :- {UNIVERSAL LOGIC GATE}

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |




## (B) NOR Gate :-

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |



when all of the inputs are 'true'. If one or more of an AND gate's inputs are false", then the output of the AND gate is false.

(2) OR Gate :- The OR gate gets its name from the fact that it behaves after the fashion of logical inclusive 'or'. The output is "True". If both inputs are "false", then the output is "false"

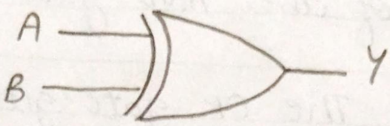
(3) NOT Gate :- A logical inverter, sometimes called NOT gate to differentiate it from other types of electronic inverter devices, has only one input. It reverses the logic state.

(4) NAND gate :- The NAND gate is a combination of OR gate followed by an inverter. Its output is "TRUE" if both inputs are 'false'. Otherwise, the output is "false".

(5) X-OR gate :- The X-OR gate (exclusive - OR) gate acts in the same way as the logical "either/or". The output is "True" if either, but not both, of the inputs are "false", or if both inputs are "TRUE". Another way of looking at this circuit is to observe that the output is 1 if the inputs are different

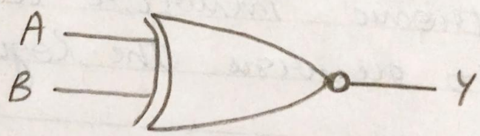
## (6) X-OR gate

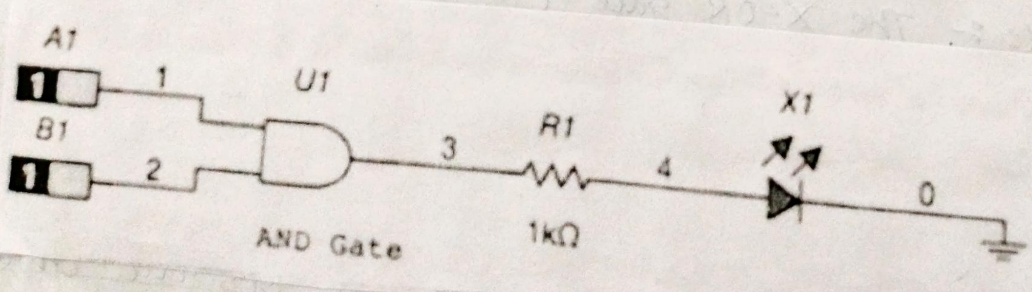
| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |




## (7) X-NOR gate

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |




| A1 | B1 | X1 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

but 0 if the inputs are the same.

(7) X-NOR gate :- Using combination of logic gates, complex operations can be performed. In theory there is no limit to the number of gates that can be arranged together in a single device. The X-NOR gate is a combination of X-OR gate followed by an inverter. Its outputs is 'TRUE' if the inputs are same and false, if the inputs are different.

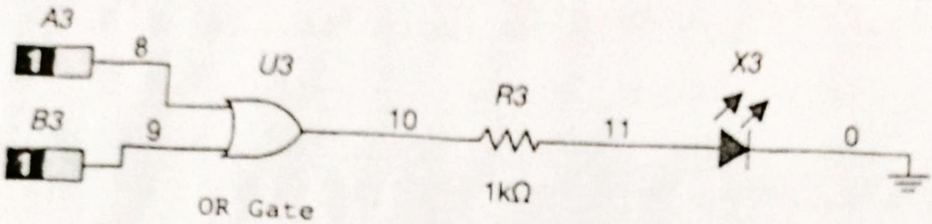
# PROCEDURE :-

(A) AND Gate (IC-7408) :-

(1) Connect one end of each of the two wires to the input slots and the other ends to the respective slots in the AND gate. Then connect a wire to the third (i.e output) slot of the AND gate to the output slot next to the LED of the kit. Now give inputs and note the output.

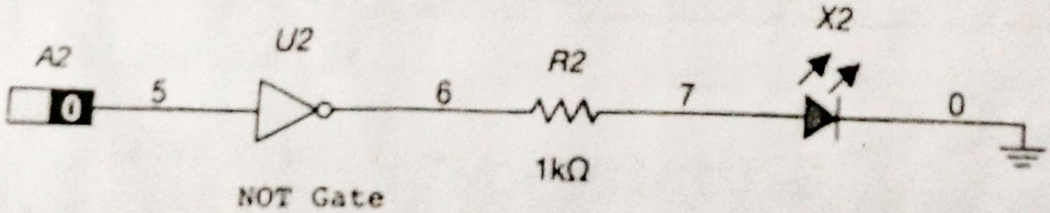
(2) If both inputs are taken 'false' then output is 'false' i.e LED does not light up.

(3) When one input is taken 'false' and the other is 'TRUE', then too the output is 'false'.



OR Gate

| A3 | B3 | X3 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



NOT Gate

| A2 | X2 |
|---|---|
| 0 | 1 |
| 1 | 0 |

(4) When both the inputs are 'True', then output is 'True' i.e LED lights up.

(B) OR Gate (IC-7432) :-

→ Connect one end of each of the two wires to the input slots and the other ends to the ~~resistance~~ respective slots in the OR gate. Then connect a wire to the third (i.e output) slot of the OR gate to the output slot next to the LED of the kit. Now give inputs & note the output.

(2) If both 'inputs' are 'false', then output is 'false' i.e LED does not light up.

(3) When one of the inputs is taken as 'True', then output is also 'True' if the other is taken 'false'.

(4) When both inputs are 'true', then output is 'True' i.e LED lights up.

(C) NOT Gate (IC-7404) :-

(1) Take one connecting wire, connect one of its ends to an input slot on the kit & the other end to the input slot of the NOT gate.

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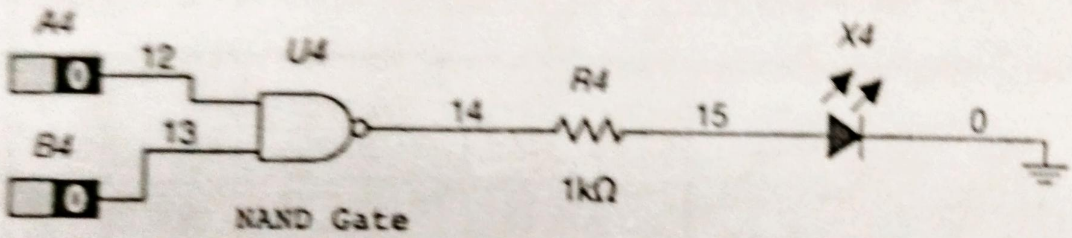



| A4 | B4 | X4 |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(2) Take another wire and connect it to the output slot of the NOT gate & the other end to the output slot next to the LED of the kit. Now, give inputs and note the output.

(3) If A is input & taken as 'false', then output is 'True'. i.e LED lights up.

(4) If A is taken 'True', then output is 'false' i.e LED does not light up.

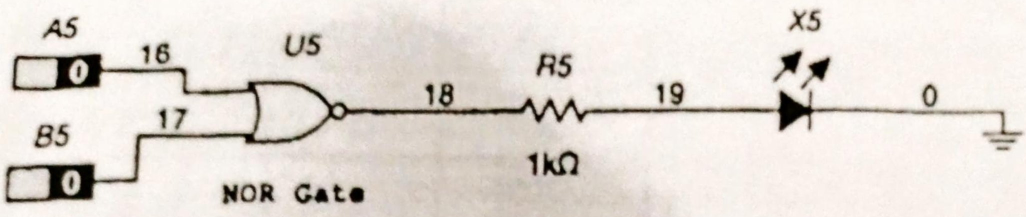
(D) NAND Gate (IC-7400):-

(1.) Connect one end of each of the 2 ~~Variable~~ wires to the input slots and the other end to the respective slots in the NAND gate. Then connect a wire to the third (i.e output) slot of the NAND gate to the output slot next to the LED of the kit. Now, give inputs and note the output.

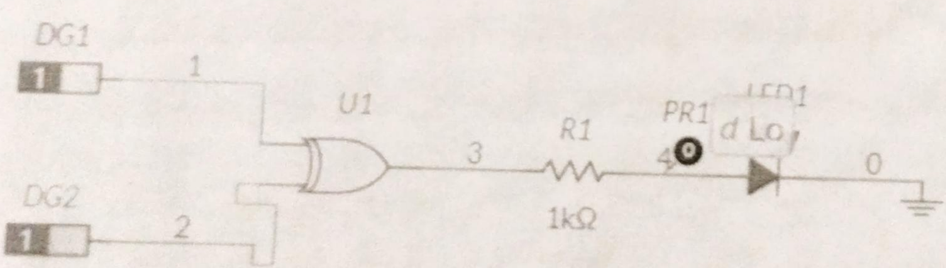
(2.) If both the inputs are taken 'false', then the output is 'True' i.e LED lights up.

(3) If A is taken 'True' & B is taken 'false' or vice-versa i.e A is taken 'false' & A is taken 'True' in both the cases, the output is 'True'.

(4.) If both the inputs are 'true', then output is 'false'




| A5 | B5 | X5 |
| --- | --- | --- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |




| A | B | Y |
| --- | --- | --- |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(E) NOR Gate (IC-7402):-

(1) Connect one end of each of the two wires to the input slots and the other ends to the respective slots in the NOR gate. Then connect a wire to the third (i.e output) slot of the NOR gate to the output slot next to the LED of the kit. Now, give inputs & note the output.

(2) If both the inputs are taken 'false' then the output is 'true' i.e LED lights up.

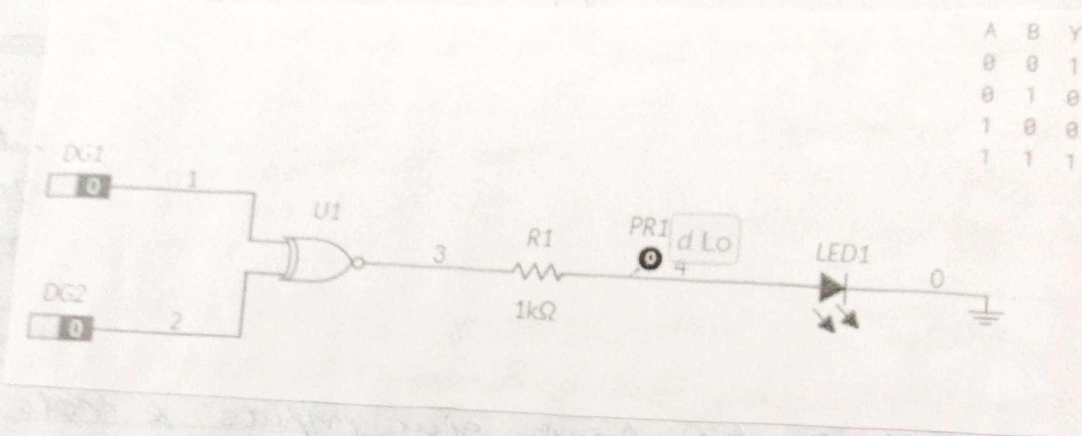
(3) If one of the inputs is taken 'false' & the other is taken 'true', then the output is 'false' i.e LED does not light.

(4) If both the inputs are 'true', then output is 'false'.

(F) X-OR gate (IC-7

(1) Connect one end of each of the two wires to the input slots & the other ends to the respective slots in the X-OR gate of the kit. Then connect a wire to the input slot of the NOT gate.

(2) Now, connect a wire to the output slot of the NOT gate and to the output slot next to the LED of the kit. Give inputs and note the output.




Result :- The truth table of various logic gates have been analyzed.

(3) If both the inputs are taken as "~~True~~ False" and the output is 'True' i.e LED lights up.

(4) If one of the inputs is taken as 'True' and the other is taken as 'false' then output is also 'false' i.e LED does not light up.

(5) If both the inputs are 'True', then output is also 'True'.

**Result:-** The truth tables of various logic gates have been analysed.