Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

Course Title:	**COE**
Course Number:	328
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Instructor:	

Assignment/Lab Number:	Lab 1
Assignment/Lab Title:	

Submission Date:	
Due Date:	

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
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Table of Contents

Introduction

Lab Objectives

- ◊ Introduction to Quartus II software and its tools
- ◊ To design, compile and simulate block diagram schematics and VHDL-based design
- ◊ Introduction to modular design and mixed-design entry

Lab work

Figure for Block Diagram

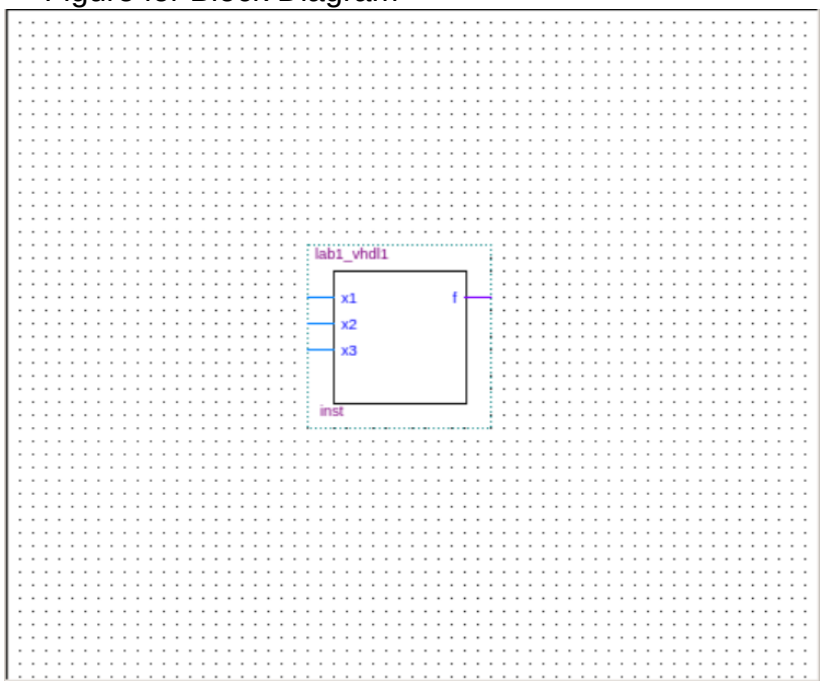
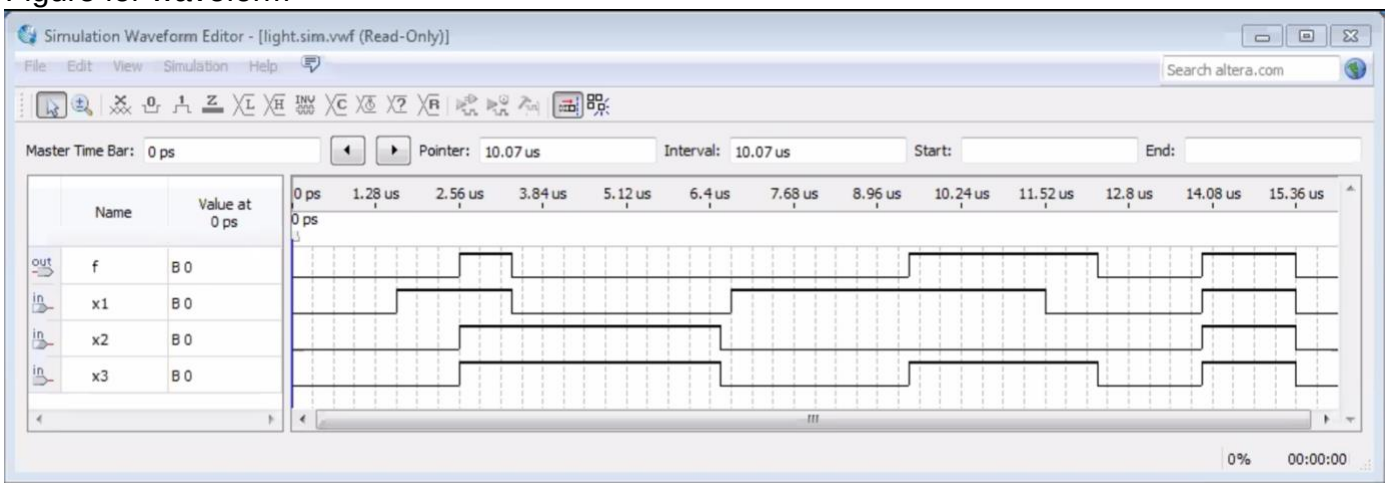


Figure for waveform



Part 2

Figure for VHDL Code

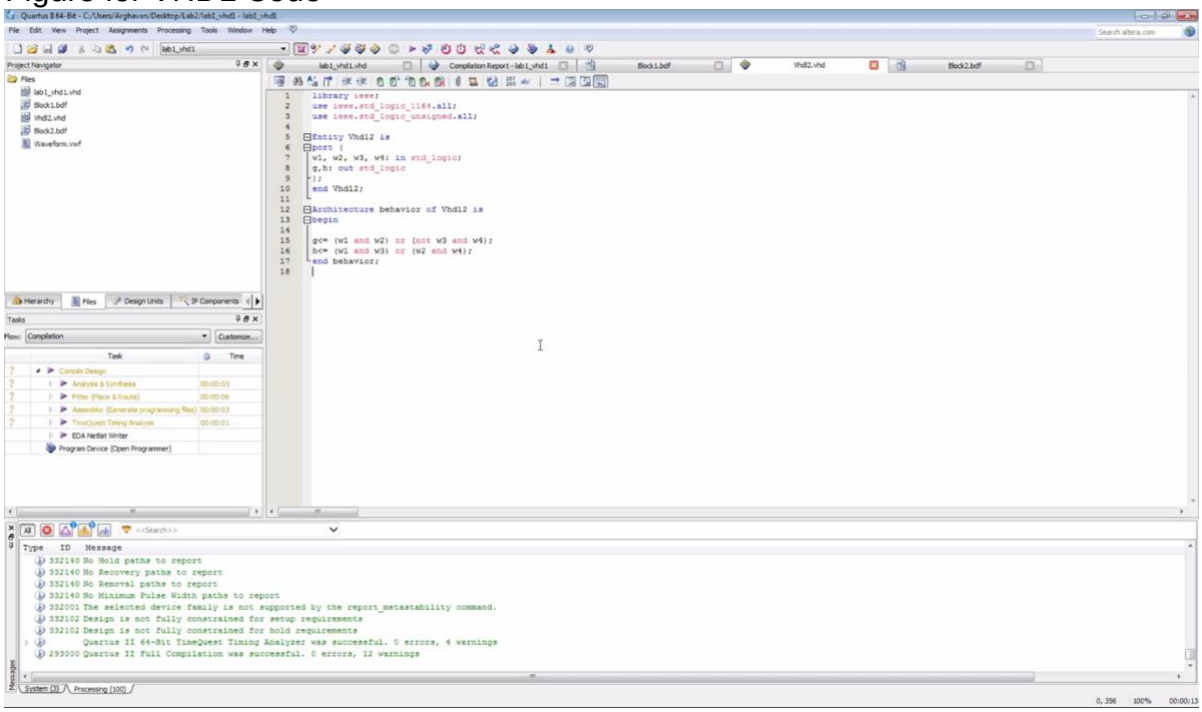
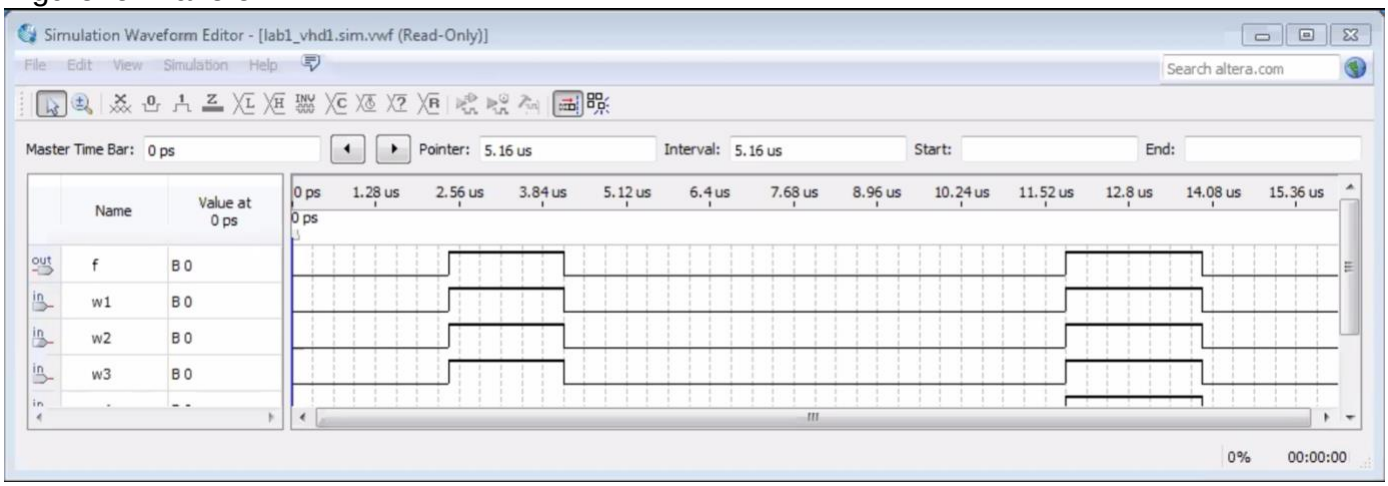


Figure for waveform



Part 3

Figure For 2 VHDL Codes

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;

ENTITY lab1_vhdl1 IS
PORT (
x1,x2,x3 : IN STD_LOGIC ;
f : OUT STD_LOGIC );
end lab1_vhdl1;

ARCHITECTURE Behavior OF lab1_vhdl1 IS
BEGIN
f <= --Insert code here
END Behavior;


```

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;

ENTITY lab1_vhdl2 IS
PORT (
w1,w2,w3,w4 : IN STD_LOGIC ;
g,h : OUT STD_LOGIC );
end lab1_vhdl2;

ARCHITECTURE Behavior OF lab1_vhdl2 IS
BEGIN
--Insert code here
END Behavior;


```

Figure for Combined block Diagram

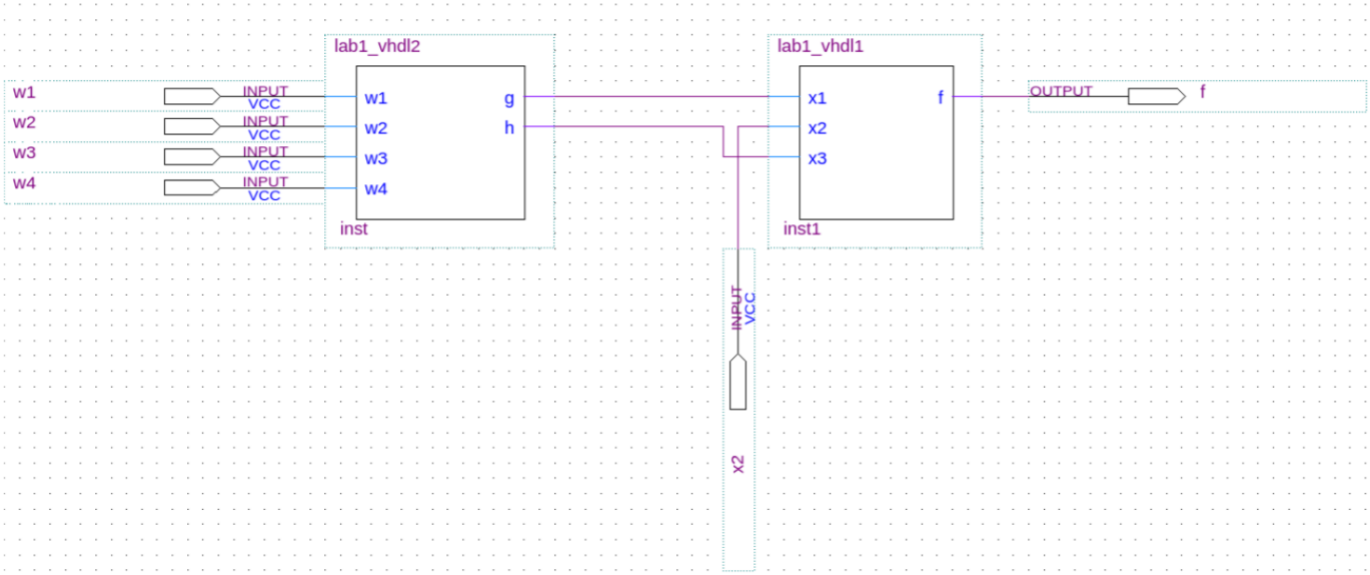
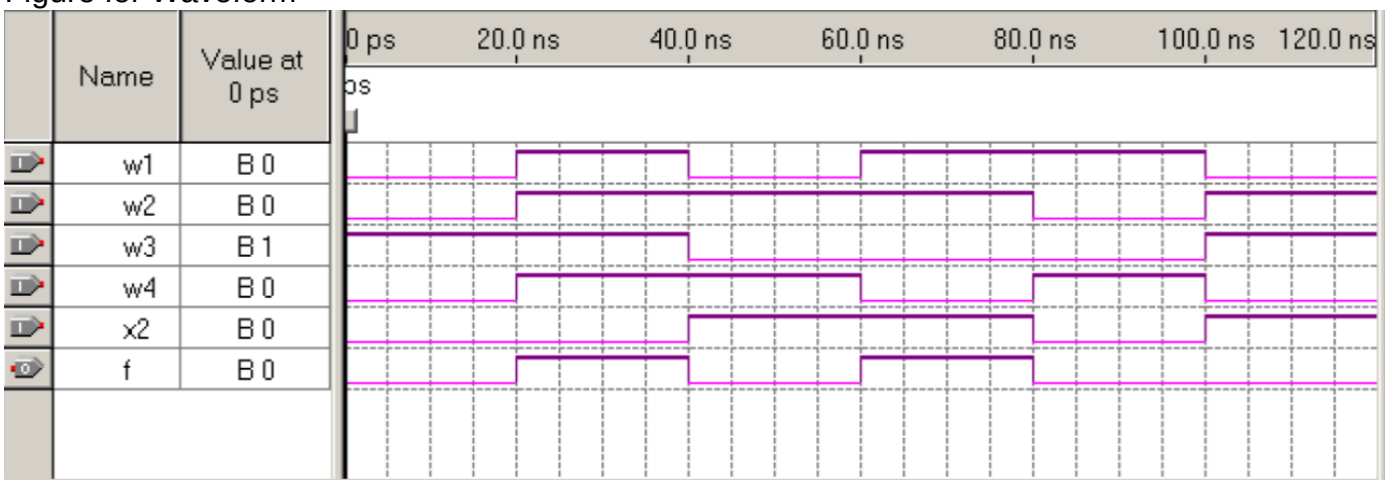


Figure for Waveform



Discussion & Conclusion

The objective of this lab is to familiarize ourselves with the Quartus 2 program and the different methods of simulating and representing a circuit with logic gates.

Result discussion

The results

As expected, the waveform output represented the combination of the VHDL codes shown in the combined block diagram (a sum of product of 3 inputs) and matched the truth table.

Lab Take-Aways

Quartus is a powerful tool for simulating complex circuits that can be broken down into simpler functions in cascade and can conveniently display the output value of the circuit when the input values are manipulated.