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Understanding Low Drop Out (LDO) Regulators

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Understanding Low Drop Out (LDO) Regulators

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ABSTRACT

This paper provides a basic understanding of the dropout performance of a low dropout linear regulator (LDO). It shows how both LDO and system parameters affect an LDO's dropout performance, as well as how operating an LDO in, or near, dropout affects other device parameters. Most importantly, this paper explains how to interpret an LDO's datasheet to determine the dropout voltage under operating conditions not specifically stated in the datasheet.

I. INTRODUCTION

Low dropout regulators (LDOs) are a simple inexpensive way to regulate an output voltage that is powered from a higher voltage input. They are easy to design with and use. For most applications, the parameters in an LDO datasheet are usually very clear and easy to understand. However, other applications require the designer to examine the datasheet more closely to determine whether or not the LDO is suitable for the specific circuit conditions. Unfortunately, datasheets can't provide all parameters under all possible operating conditions. To the designer must interpret and extrapolate the available information to determine the performance under non-specified conditions.

II. LINEAR REGULATORS

There are two types of linear regulators: standard linear regulators and low dropout linear regulators (LDOs). The difference between the two is in the pass element and the amount of headroom, or dropout voltage, required to maintain a regulated output voltage. The dropout voltage is the minimum voltage required across the regulator to maintain regulation. A 3.3 V regulator that has 1 V of dropout requires the input voltage to be at least 4.3 V. The input voltage minus the voltage drop across the pass element equals the output voltage. This brings up the question, "What is the minimum voltage drop across the pass element?" The answer to this question depends upon several factors.

III. UNDERSTANDING LDO

For standard regulators, the pass element is either a Darlington NPN or PNP output stage. Fig. 1 shows that a Darlington transistor has a high collector-to-emitter voltage drop because the gate drive voltage encounters two base-to-emitter drops before reaching the output. Standard linear regulators have voltage drops as high as 2 V which are acceptable for applications with large input-to-output voltage difference such as generating 2.5 V from a 5 V input.

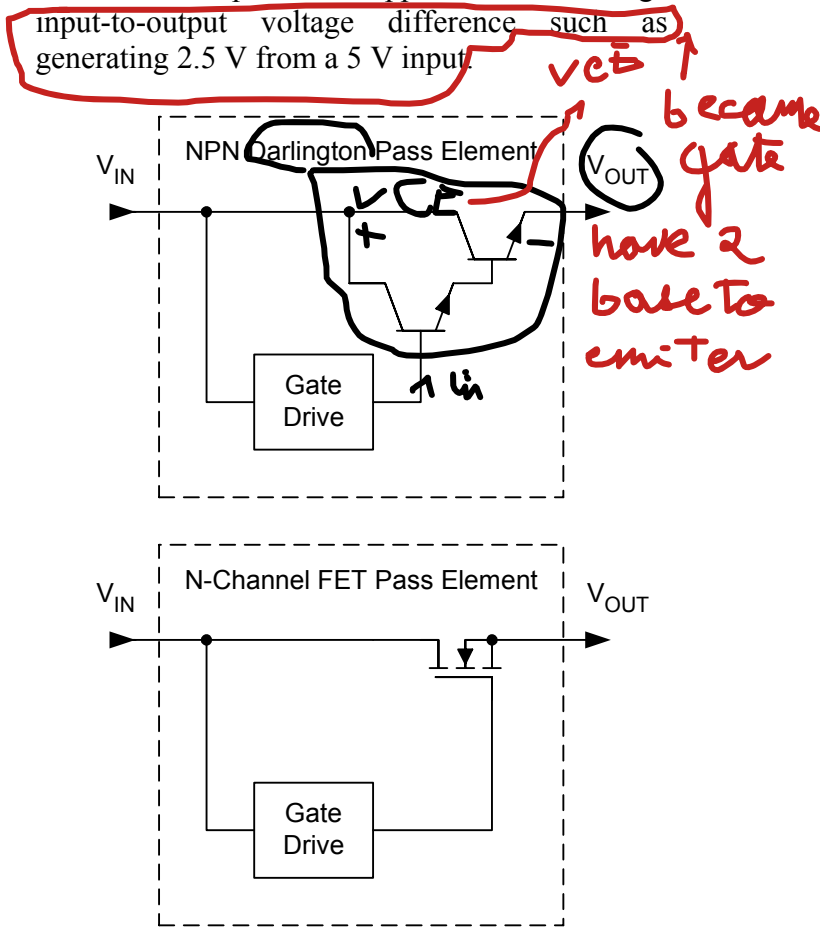

Fig.1. LDO pass elements.

A typical application such as generating 3.3 V from a 3.6 V Li-Ion battery requires a much lower dropout voltage (less than 300 mV). These applications require the use of an LDO to achieve the lower dropout voltage. Most LDOs use an N-channel or P-channel FET pass element and can have dropout voltages less than 100 mV. Fig. 1 shows that the dropout voltage of an N-channel FET LDO is only dependent upon the minimum voltage drop across the FET. This voltage drop is a function of the $R_{DS(on)}$ of the FET.

Fig. 2 shows an LDO block diagram in its most basic form. The input voltage is applied to a pass element, which is typically an N-channel or P-channel FET, but can also be an NPN or PNP transistor. The pass element operates in the linear region to drop the input voltage down to the desired output voltage. The resulting output voltage is sensed by the error amplifier and compared to a reference voltage. The error amplifier drives the pass element's gate to the appropriate operating point to ensure that the output is at the correct voltage. As the operating current or input voltage changes, the error amplifier modulates the pass element to maintain a constant output voltage. Under steady state operating conditions, an LDO behaves like a simple resistor.

For example, with the following operating conditions: V_{IN}=5 V, V_{OUT}=3.3 V, and I_{LOAD}=500 mA, the LDO pass device behaves like a 3.4-Ω resistor. This equivalent resistance is determined by calculating the voltage drop across the LDO and dividing by the load current:

(5 V-3.3 V)/0.5 A = 3.4 Ω. (1)

Under these specific application operating conditions, the LDO can be replaced by a 3.4 Ω.resistor with no change in output voltage or current. In a practical application, however, operating conditions are never static; therefore, feedback is necessary to change the LDO's effective resistance to maintain a regulated output voltage.

Fig. 3 shows the operating region of an LDO's N-channel pass element. The range of operation is limited in the x-axis by the saturation region of the pass element, and limited in the y-axis by either the pass element's saturation region or by the IC's programmed current limit. In order to operate properly and maintain a regulated output voltage, the pass element must operate within the boundaries set by these two lines. In the example, the drain-to-source voltage of 1.7 V and the drain current of 500 mA set the operating point at "A." At this point, the LDO sets the pass element's gate-to-source voltage at 3 V to maintain regulation. A line drawn through the origin and point "A" represents the 3.4 Ω resistance.

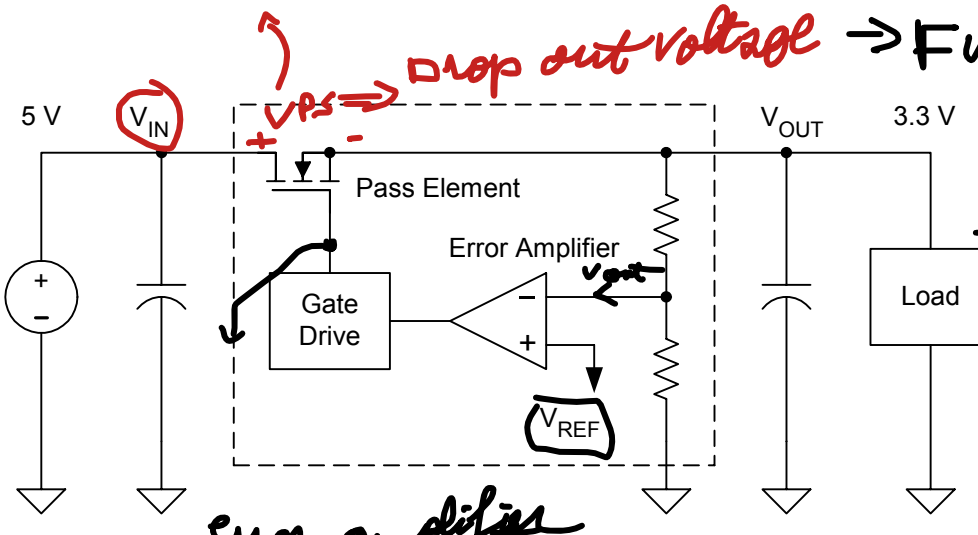

Fig. 2. LDO block diagram.

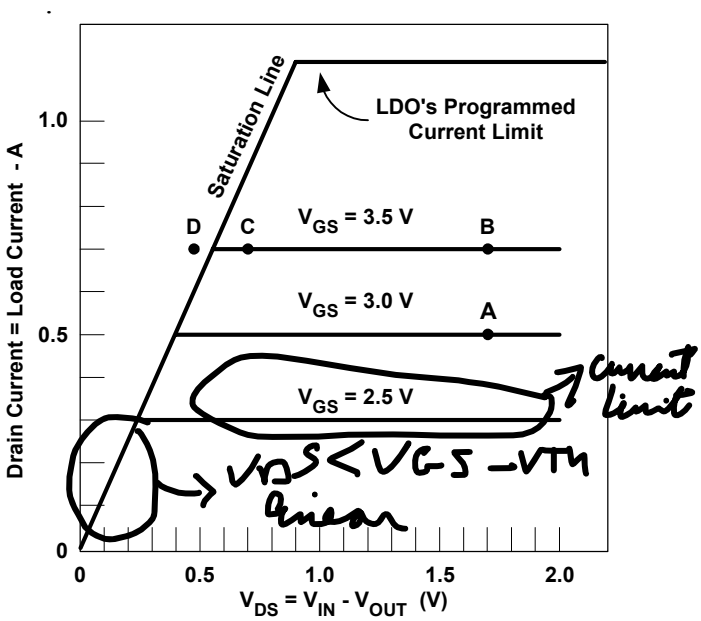

Fig. 3 Operating region of an LDO's N-channel pass element.

Consider a change to the static conditions in the example: if the load resistance decreases (an increase in load current), the LDO must react to maintain regulation. If it doesn't react, the LDO has a higher voltage drop across the pass element which causes the output voltage to fall out of regulation. The LDO must decrease the pass element's resistance by increasing the gate-to-source voltage on the FET. When the gate-to-source voltage increases, the operating point moves upward, assuming a fixed input and output voltage. If I_{OUT}=700 mA, the error amplifier increases the pass element's gate-to-source voltage to 3.5 V to maintain regulation. This corresponds to "B." A line drawn through the origin and point "B" now represents a pass element resistance of 2.4 Ω. Fig. 3 shows that with a drain-to-source voltage of 1.7 V, the LDO's maximum current draw is only limited by the maximum programmed current limit.

When considering a decrease in input voltage, the pass element must reduce its drain-to- source voltage to keep the output in regulation. If V_{IN} is reduced to 4 V, the operating point moves to "C." This point represents a 1-Ω .resistance. Note that the gate-to-source voltage remained unchanged. Any further increase in current or decrease in input voltage forces the operating point onto the saturation line of the pass element. At this point, the LDO is said to be in "dropout." The saturation line is the minimum FET drain-to-source resistance ($R_{DS(on)}$). If the system operating conditions dictate that the LDO operate at point "D", the LDO cannot reduce the drain-to-source voltage any further to stay in regulation. In practice, this results in the output voltage falling out of regulation. The pass element now operates up and down the saturation line to correspond with changes in input voltage, or load resistance. Note that a line drawn from the origin through the saturation line represents the FET's minimum $R_{DS(on)}$. If this were a 1A LDO, it would have a datasheet dropout rating of 800 mV at 1 A. Note that when the LDO is operated at a fraction of its rated output current, its dropout voltage is a fraction of the maximum specified dropout voltage.

LDO datasheets can only specify the IC's dropout voltage under a limited number of operating conditions. Few datasheets provide a graph like that shown in Fig. 3. For all other conditions, the user must interpolate the data to determine the dropout voltage at a specific output current. This task is surprisingly easy. As an example, consider an application that requires V_{OUT} = 3 V at 170 mA with an input voltage that varies between 3.15 V and 3.45 V. The designer has chosen a TPS79330 LDO and needs to know if it can be ensured that the LDO doesn't enter dropout.

Table 1 shows the datasheet's ensured dropout voltage from the parametric table. The datasheet shows that the maximum dropout voltage (ensured over all temperatures) for a 3.0 V output at 200 mA is 200 mV. The minimum input voltage of 3.15 V for this application requires the effective dropout voltage be less than 150 mV at 200 mA. For this regulator, the actual dropout is less than 200 mV since the current is less than 200 mA, but the datasheet does not specify the dropout voltage at 170 mA. When operating in dropout, the LDO pass element is at its minimum $R_{DS(on)}$ which is equivalent to operating on the saturation line like the one shown in Fig. 3. This minimum resistance is calculated by dividing the dropout voltage by the test current. The TPS79330 pass element minimum $R_{DS(on)}$ is shown in Equation (3).

$$R_{DS(on)} = 200\ mV/200\ mA = 1\ \Omega. \quad (3)$$

The dropout voltage at any other current is calculated by multiplying this minimum $R_{DS(on)}$ by the actual load current. Operating at lower currents corresponds to moving down and to the left on the saturation line. Since the $R_{DS(on)}$ is known, the dropout voltage in this application is calculated as

$V_{DO} = 1\ \Omega \bullet 170\ mA = 170\ mV$. In this example, this is still not low enough to ensure regulation. The designer must find an LDO with a lower dropout voltage at 170 mA to meet requirements desired.

Several factors affect an LDO's minimum dropout resistance. The main contributor is the size of the pass element. A characteristic of both discrete FETs and an LDO's integrated FET is that their resistance is inversely proportional to the die-size. With all other factors being equal, a larger die-size has a lower resistance. Fig. 6 shows a graph of minimum LDO resistance versus package-size for several different LDOs. This graph is not linear for two reasons: the entire package size is not devoted to the pass element, and because not all LDOs are produced with the same manufacturing process. This graph shows that an extremely low dropout voltage may be achieved by using a larger LDO at only a fraction of its maximum current rating.

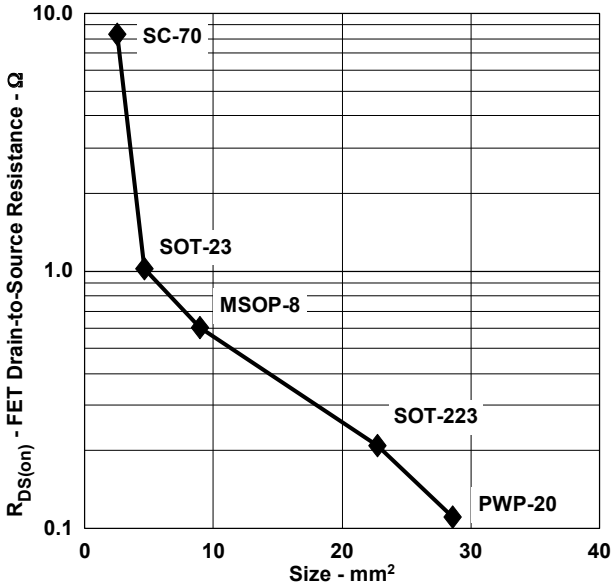

Fig. 6. $R_{DS(on)}$ variability by package-size.

TABLE 1. TPS79330 ENSURED DROPOUT VOLTAGE

PARAMETER		TEST CONDITIONS	Min	Typ	Max	Units
Dropout voltage[2] (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)	TPS79328	I_{OUT} – 200 mA		120	200	mV
	TPS793285	I_{OUT} – 200 mA		120	200	
	TPS79330	I_{OUT} – 200 mA		112	200	
	TPS79333	I_{OUT} – 200 mA		102	180	
	TPS793475	I_{OUT} – 200 mA		77	125	

TABLE 2. TPS79430 ENSURED DROPOUT VOLTAGE

PARAMETER		TEST CONDITIONS	Min	Typ	Max	Units
Dropout voltage[2] (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)	TPS79428	I_{OUT} – 250 mA		155	210	mV
	TPS79430	I_{OUT} – 250 mA		155	210	
	TPS79433	I_{OUT} – 250 mA		145	200	

Another factor affecting an LDO's minimum dropout resistance is the input voltage to the device. This is a second-order effect, but is worth noting. The higher output voltage options require a higher input voltage, which allows the device to drive the pass element harder, and in turn provides a slightly lower resistance. Most discrete FET datasheets show a change in $R_{DS(on)}$ versus gate-to-source voltage. Some LDO datasheets provide a graph (Fig. 7) of dropout versus input voltage, but this is rare. Even without a graph, this information is evident from the dropout data shown in Fig. 4. The 3.0-V option (TPS79330) in Fig. 3 has a 200-mV dropout voltage while the 4.75-V option (TPS793475) has a 125-mV dropout voltage. This is a 37 % reduction in dropout voltage.

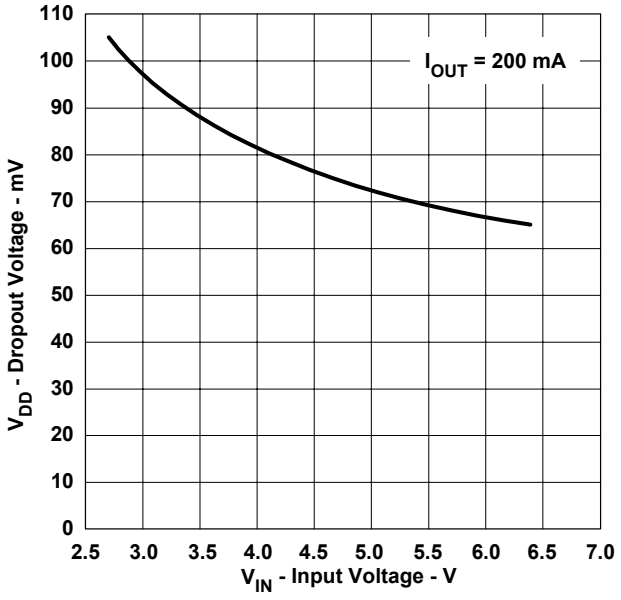

Fig. 7. TPS79901 dropout voltage vs. input voltage.

Different manufacturers test dropout differently which leads to confusion when reading different datasheets. Even various LDOs from the same manufacturer are tested differently, and one method is not necessarily better than another. The choice to test one way or another is typically driven by manufacturing and test constraints. One test method is to apply an input voltage that is some number of millivolts below the nominal output voltage and then load the LDO with the test current. For example, 3.2 V is applied to a 3.3-V LDO and then the output voltage is measured. The dropout voltage is the differential between the input voltage and the output voltage. If V_{OUT} is 2.9 V, the LDO has a 300 mV dropout voltage. An LDO tested in this method has a note similar to that shown below.

$$V_{IN} = V_{OUT(nom)} - 0.1\ V \quad (4)$$

Another test method is to measure the output voltage when V_{IN} is 1 V above the nominal output voltage and then load the LDO with the specified test current. The input voltage is then reduced until V_{OUT} drops by a specified number of millivolts. For example, 4.3 V is applied to a 3.3-V LDO. The output voltage is measured (assuming at 3.3 V), and then the input voltage is reduced until the output voltage measures 3.2 V. Dropout is defined as the input voltage minus the output voltage at this point. If V_{IN} = 3.5 V when V_{OUT} = 3.2 V, the LDO has a 300-mV dropout voltage. An LDO tested in this method will have a note similar to that shown below.

"Dropout voltage is defined as the differential voltage between V_{OUT} and V_{IN} when V_{OUT} drops 100 mV below the value measured with $V_{IN} = V_{OUT} + 1$ V "

Some LDO parameters are affected when an LDO is in or near dropout. One parameter affected is the power supply rejection ratio (PSRR). Most manufacturers specify and measure PSRR with an input voltage that is 1 V above the nominal output voltage. This specification and measurement ensures that the LDO is not on the edge of dropout when PSRR is measured. PSRR is measured by modulating the input voltage to the LDO and measuring the change on the output. The test results are only valid if the LDO's pass element stays in the active region. If the LDO starts to enter dropout, the data is invalid. When the LDO starts to enter dropout, the error-amplifier output voltage reaches a maximum value because it is trying to drive the pass element harder to maintain regulation.

At that point, the error amplifier is said to be in saturation. Since the pass element is already in saturation, its resistance is at the minimum value and cannot be decreased any further. .

At this point, the LDO cannot react to changes in the input voltage and the PSRR drops significantly. This data is not typically provided in LDO datasheets and the user is left to generate these curves on their own. Fig. 8 shows a typical plot of PSRR versus an LDO's input to output voltage differential. The LDO starts entering dropout at about V_{IN}-$V_{OUT=}$=0.4 V. If high PSRR is a system requirement, LDOs should be operated with enough headroom to stay away from the saturation region. For most LDOs, this is usually about 1 V.

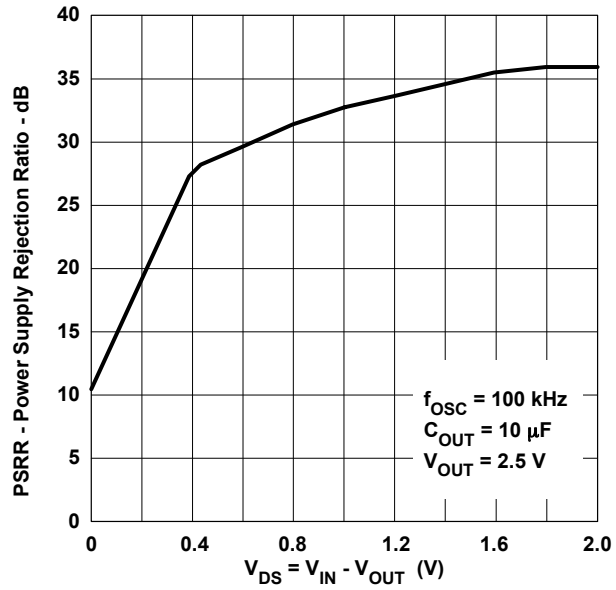

Fig. 8. Typical LDO power supply rejection ratio vs V_{IN} - $V_{OUT.}$

Entering dropout also affects an LDO's output noise. An LDO's output noise is reduced when the LDO is in or near dropout. All bandgap references (V_{REF}) produce noise, and in an LDO, the bandgap noise is fed directly into the error amplifier as shown in Fig. 1. The noise on the output of the amplifier modulates the pass element's gate voltage which generates noise on the LDO output. When an LDO is in dropout, the error amplifier output voltage is at its maximum, and its ability to pass bandgap noise from its input to its output is reduced. This reduces output noise. This feature is sometimes used with standard LDOs in a low noise application like powering a phased lock loop (PLL). If tight regulation is not needed, the LDO can be intentionally operated in dropout to provide this feature. For example, a 3.3-V LDO can be powered from a 3.3-V input to drive a PLL that requires a low noise input, but not a tightly-regulated input. The input voltage to the PLL is 3.3-V minus the LDO dropout voltage. If the LDO has a high-current rating and the PLL has a low-load current, the dropout voltage may be 50 mV or lower. A drop of 50 mV is only 1.5% of a 3.3-V output. However, PSRR may be a big concern in this case. The user must determine the tradeoff between PSRR and low-noise performance. If the input voltage has a lot of power supply ripple voltage, a high PSRR, low noise LDO must be used. If the input voltage comes from a battery or another LDO and has very little ripple, a standard LDO can be used in dropout to achieve a low noise output.

CONCLUSION

In summary, LDO dropout is rarely specified for a designer's specific operating conditions. The actual dropout is easily determined by interpolating the available datasheet information. LDO dropout is influenced by FET size and input voltage, and LDOs entering dropout affect circuit performance. Once a designer understands this information, he can select an LDO that is optimized for his specific circuit requirements.

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