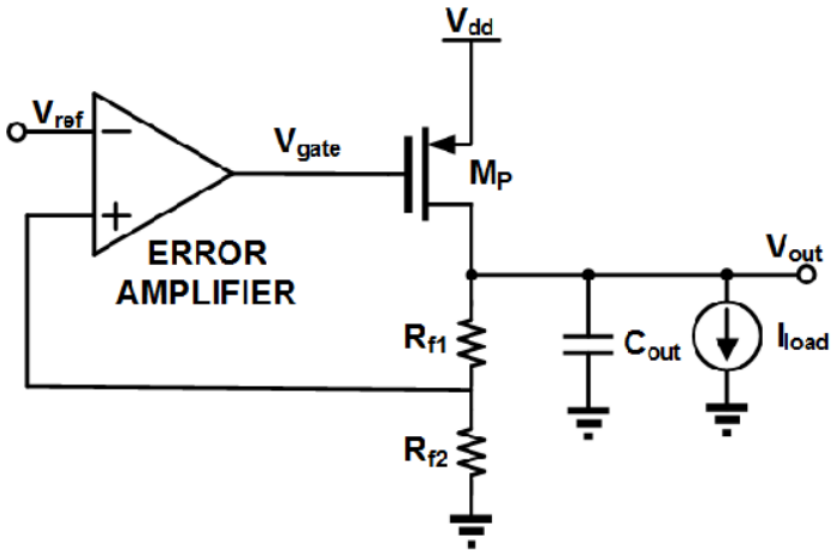
Lab 11

LDO Design



1) Build a simple LDO using the 5t OTA (designed in lab 05 and verified across PVT in lab 09), two feedback resistors, and pass-device.
2) Size the pass device to handle 1.5mA load current (use resistive load or dc current load) and get 300 mV dropout on the pass device (Keep it in saturation). For example. If typical supply is 1.2 V, V_{out} should be 0.9 V.
3) Choose the resistors values so that $V_{feedback}$ is a ratio of Vout ($V_{fb} = V_{ref}$) which should be the common mode voltage of the opamp input pair (use V_{ref} = 600 mV).
4) Use C_{out}= 10 µF so that the dominant pole is at the LDO output.
5) Check the DC operating point of all MOS devices and try to consume <21 µA IQ (in feedback resistors and OTA).
6) Run Dc simulations and check V_{out} Vs input supply “1.32V to 1.08V” range (line regulation).
7) Run Dc simulations and check V_{out} Vs load current “500 µA to 1.5 mA” range (load regulation).
8) Check transient response of the LDO (Ramp the supply then V_{ref} then plot V_{out} Vs them).
9) Check AC simulations and plot PSR of the LDO output (Use 1 V ac at V_{in} and plot 20 dB of V_{out}).
10) Check the LDO loop stability (PM and GM). Should be > 50 degrees and 12dB respectively.