EE230-02 RFIC II
Fall 2018

Lecture 21: PLL Wrap-up

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ENG-259

Schedule

No Class – I am traveling

- Nov.15, Thursday
- Nov. 20, Tuesday HW#3 Due

Remaining schedule

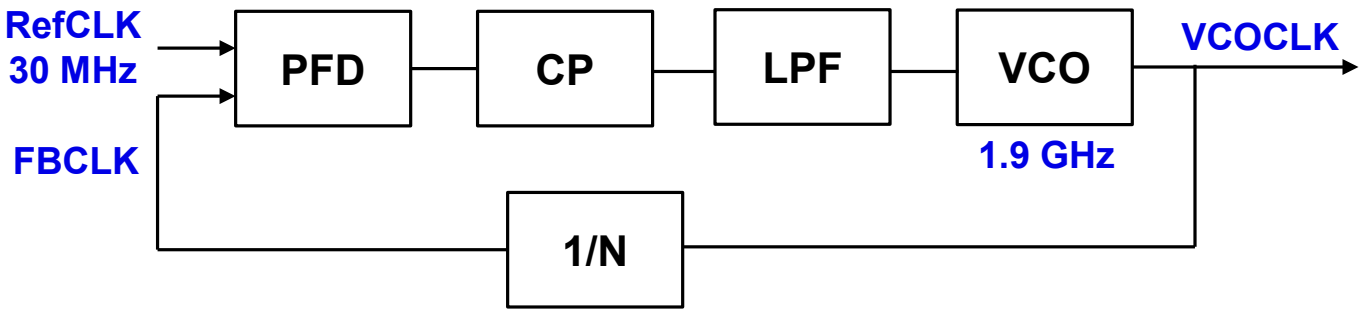
- Nov. 27 Project Presentation Group 1-3
- Nov. 29 Project Presentation Group 4-6
- Dec. 4 Project Presentation Group 7-9 & PA Lecture
- Dec. 6 PA lecture & Final Review
- Dec. 10 Project Report Due
- Dec. 14 Final Exam at 2:45 PM

Project Presentation

Group	Student 1	Student 2	Presentation Order
1	Chad	Muhammad	8
2	Khoa	Yueyang	5
3	Jesus		4
4	Lenny		3
5	Ashley	Lava	2
6	Justin	Arthur	1
7	Hoa	Cuong	6
8	Xing	Alex	7
9	Yu-Chung		9

Project Description

1.9 GHz Charge Pump PLL
VDD=1V



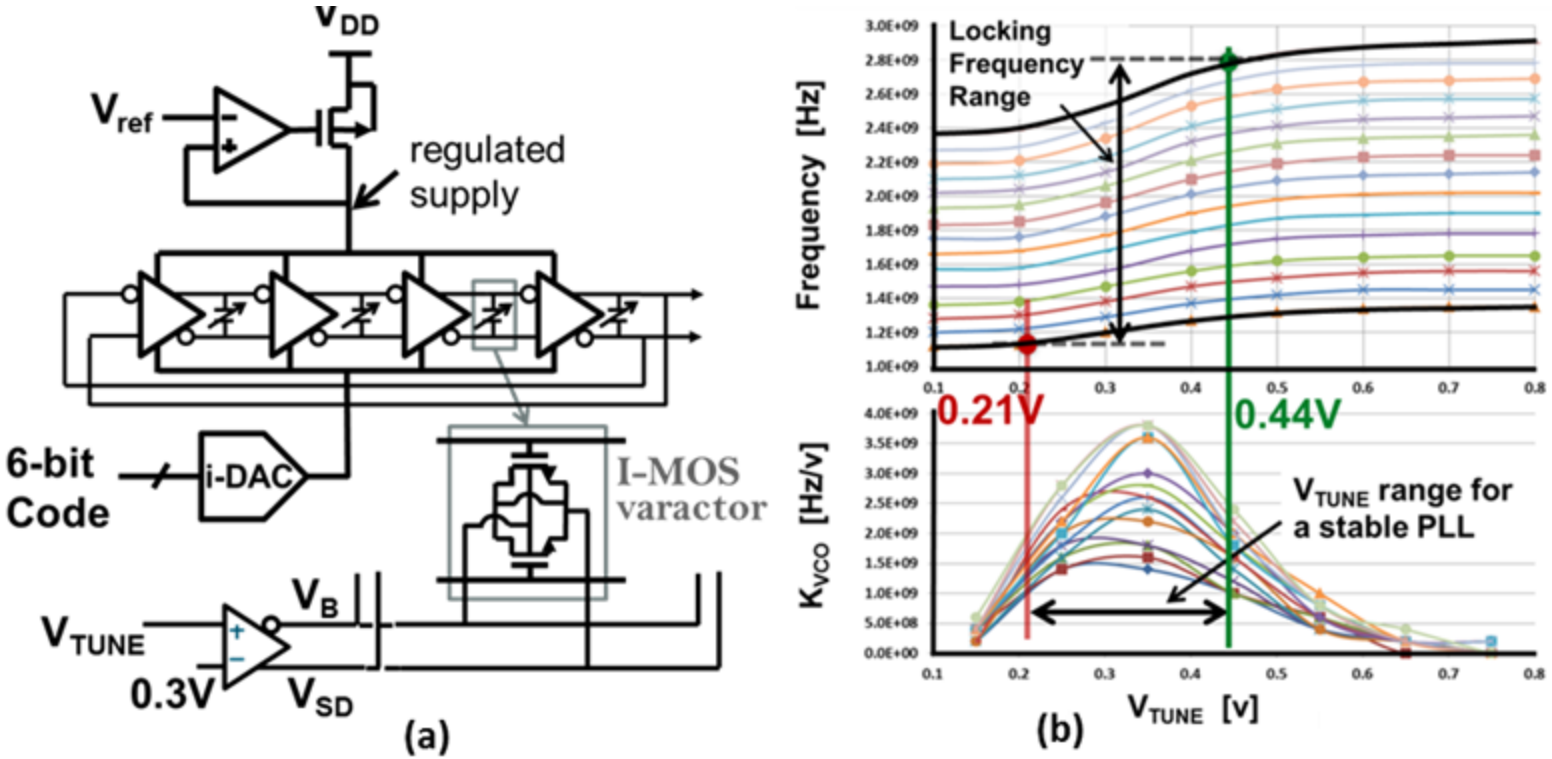
Project Report

One Project Report per group

- Report should include the followings
  - Verilog-A or Verilog-AMS model and simulation results
  - Matlab behavioral simulation showing stability
  - Schematic capture of major blocks
  - Key Simulation results
  - Summary table showing the performance achieved
- Report should be in IEEE conference paper format
- Project Report due : 5 PM, Dec 10

Project Reference

Reference: Charge Pump PLL*



* A 216μW 281MHz-1.126GHz Self-Calibrated SSCG PLL
with 0.6V Supply Voltage in 55nm DDC™ CMOS Process – Unpublished work by Ahn & Lee

Target Spec – Beat the best

TABLE I
PERFORMANCE COMPARISON

	Ref[4]	This Work	
Process	0.13µm CMOS	Conventional 55nm CMOS	DDC 55nm CMOS
Supply Voltage	0.5V	0.85V	0.6V
PLL Locking Range [MHz]	360 ~ 610	257 ~ 1,218	281 ~ 1,126
RMS Jitter	8.01ps @550MHz	12.75ps @800MHz	8.16ps @800MHz
Power Comsumption	1.25mW @550MHz	701µW @800MHz	216µW @ 800MHz
Active Die Area	0.04mm^2	0.06mm^2	0.06mm^2
FoM [dB]	-221	-219	-228

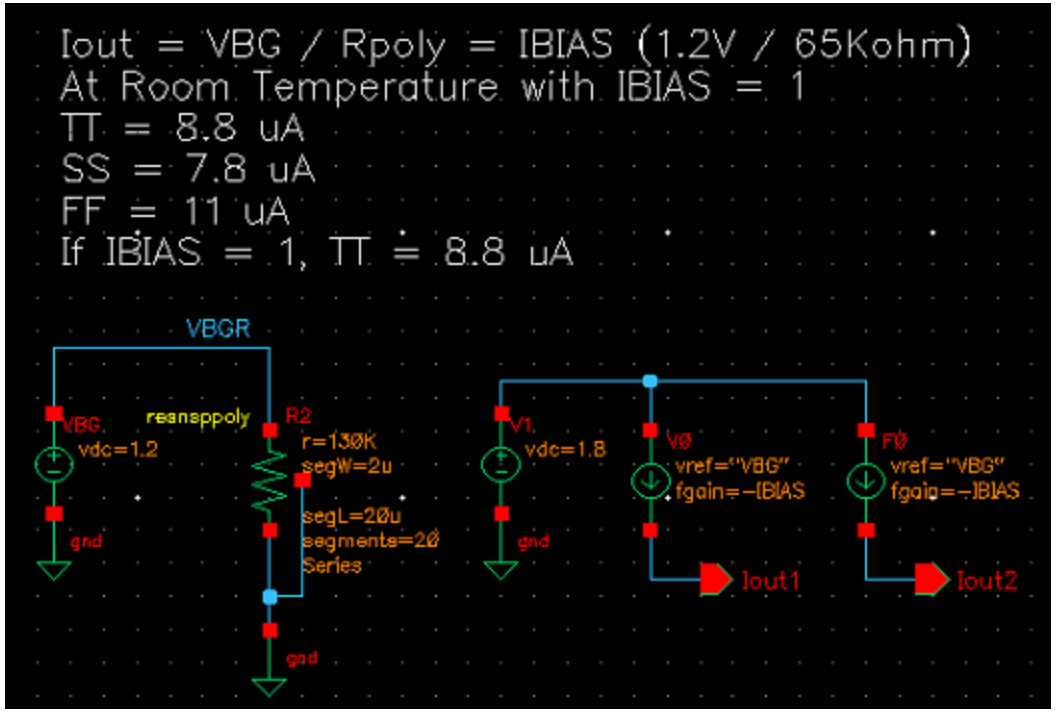
* $\mathbf{FoM} = 10 \cdot \log\left(Jitter^2 \cdot Power / 1mW\right)$

Design Constraint

- Architecture: Type-II Integer-N Charge Pump PLL
- Goal is to achieve FoM < -220 dB with the following constraint
  - Use 45nm technology PDK in gpdk045
  - VDD=1V
  - Device types available for the design
  - → nmos1v, pmos1v, resnsppoly, Ideal cap
  - RefCLK = 30 MHz
  - Bias Current : Use “ideal_bias” current cell in the next slide
  - PVT corners
    - TT, 1V, 27C
    - SS, FF
    - 0.9V, 1.1V
    - -40C, 125C

Bias Current

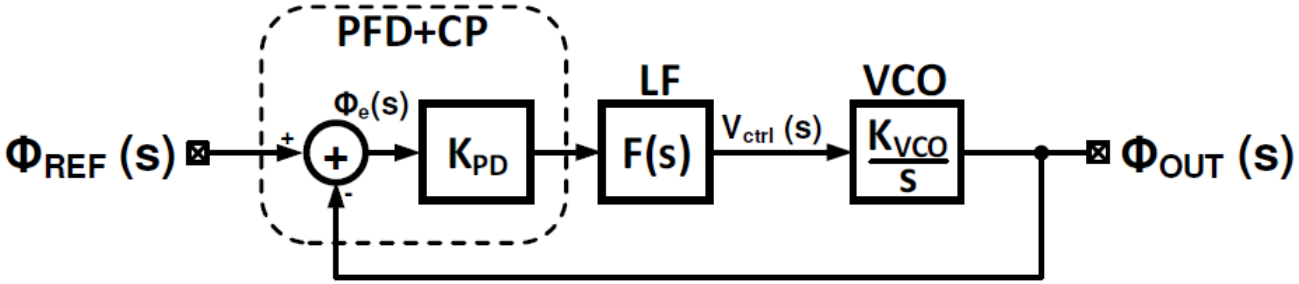
Lib: ee288lib
Cell: ideal_bias
Choose different value for IBIAS to vary the output current level

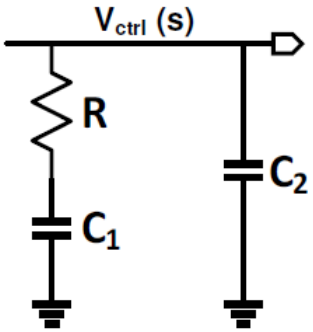


References

- PLL
  - Rishi Ratan, From Chapter 3, MS Thesis, UIUC, 2014
  - H. Ahn and S. Lee*, File name: VLSI2014_PLL_v7*
- Verilog-A
  - VCO_VerilogA_ECE546_UIUC
  - PLL_Jitter_measurement_in_Spectre
- Verilog-AMS
  - Rishi Ratan, Chapter 6, MS Thesis, UIUC, 2014
- Jitter measurement
  - PLL_Jitter_measurement_in_Spectre
  - https://www.youtube.com/watch?v=VvkHPoSVpVc

Modeling of Charge-Pump PLL





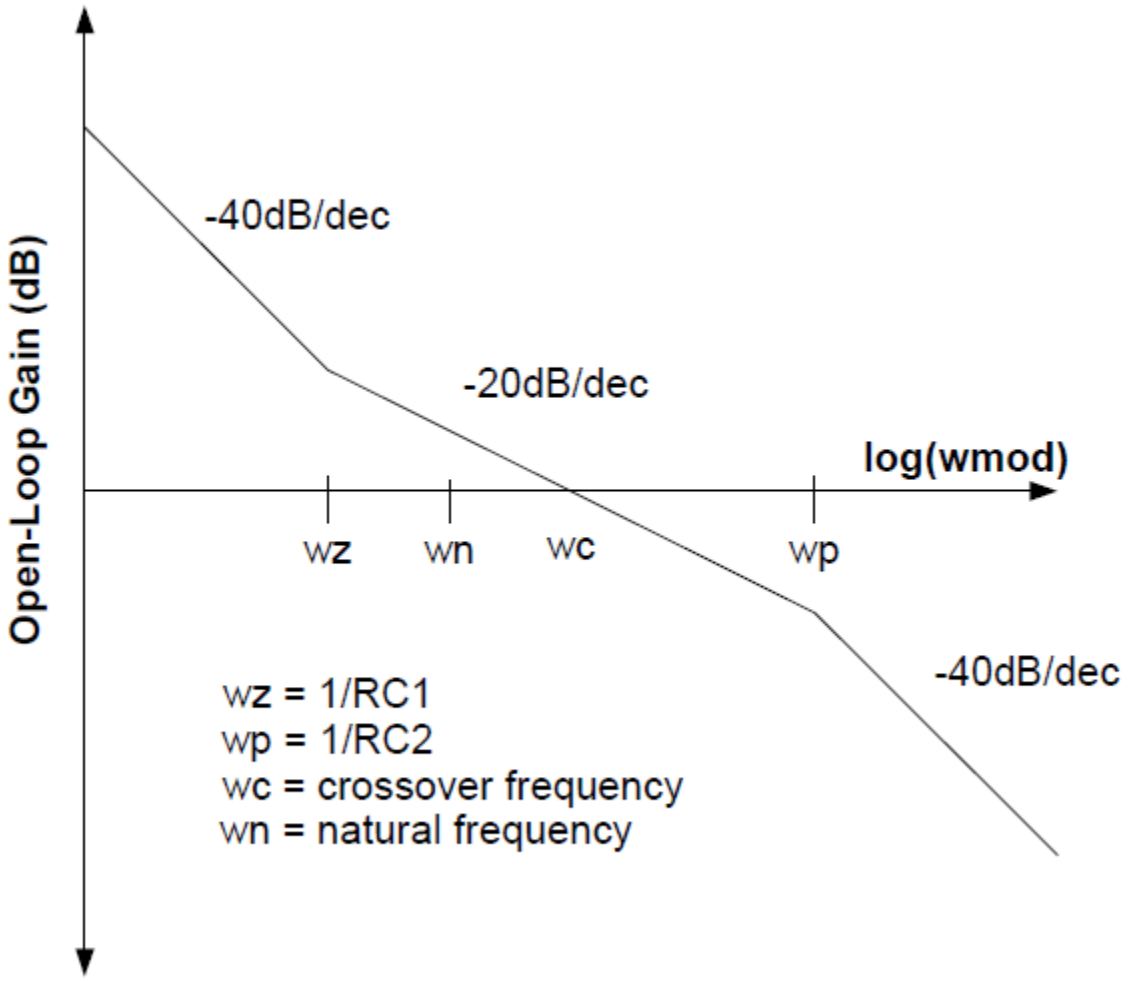
$$LG(s) = K_{PD} \cdot F(s) \cdot \frac{K_{VCO}}{s}$$

$$= K_{PD} \cdot K_{VCO} \cdot \frac{s + \frac{1}{RC_1}}{C_2 s^2 \left(s + \frac{C_1 + C_2}{RC_1C_2} \right)}$$

$$\omega_z = \frac{1}{RC_1};\ \omega_{p1} = \omega_{p2} = 0; \omega_{p3} = \frac{C_1 + C_2}{RC_1C_2}$$

$$\phi_M = \arctan\left(\frac{\omega_{ugb}}{\omega_z}\right) - \arctan\left(\frac{\omega_{ugb}}{\omega_{p3}}\right)$$

Open Loop Transfer Function



Linear Model of Charge-Pump PLL

$$LG(s) = K_{PD} \cdot F(s) \cdot \frac{K_{VCO}}{s}$$
$$= K_{PD} \cdot K_{VCO} \cdot \frac{s + \frac{1}{RC_1}}{C_2 s^2 \left(s + \frac{C_1 + C_2}{RC_1 C_2}\right)}$$

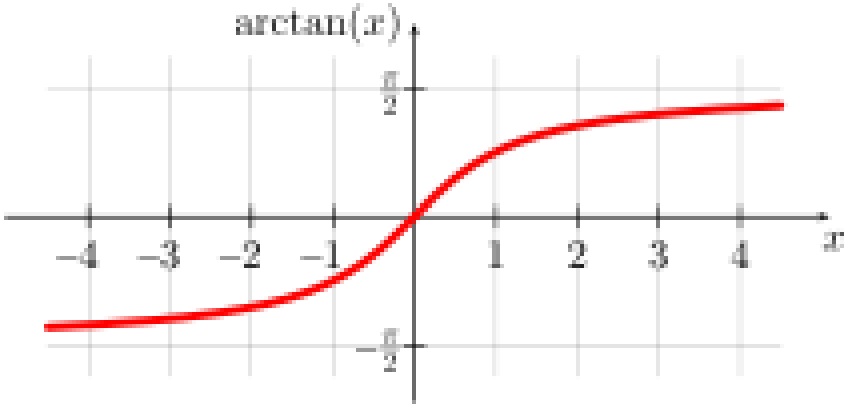
$$\omega_z = \frac{1}{RC_1};\ \omega_{p1} = \omega_{p2} = 0; \omega_{p3} = \frac{C_1 + C_2}{RC_1 C_2}$$

$$\phi_M = \arctan\left(\frac{\omega_{ugb}}{\omega_z}\right) - \arctan\left(\frac{\omega_{ugb}}{\omega_{p3}}\right)$$

$$\omega_{ugb} = \omega_z \sqrt{\frac{C_1}{C_2} + 1}$$

$$\phi_{M\_max} = \arctan\left(\sqrt{\frac{C_1}{C_2} + 1}\right) - \arctan\left(\frac{1}{\sqrt{\frac{C_1}{C_2} + 1}}\right)$$

What is arctangent ?



If C_1/C_2 = 10, then Phase Margin is

arctan(sqrt(11)) = 73.2213451 degree — arctan(1 / sqrt(11)) = 16.7786549 degree = **57 degree**

Loop Filter Design Procedure

1. Choose desired bandwidth ω_{ugb}, phase margin ϕ_M and resistor R according to specification. Then calculate the K_c from Eq. 4.6:

$$K_c = \frac{C_1}{C_2} = 2(\tan^2(\phi_M) + \tan(\phi_M \sqrt{\tan^2(\phi_M) + 1})) \tag{4.6}$$

2. From Eq. 4.4 we have:

$$\omega_z = \frac{\omega_{ubg}}{\sqrt{\frac{C_1}{C_2} + 1}} \tag{4.7}$$

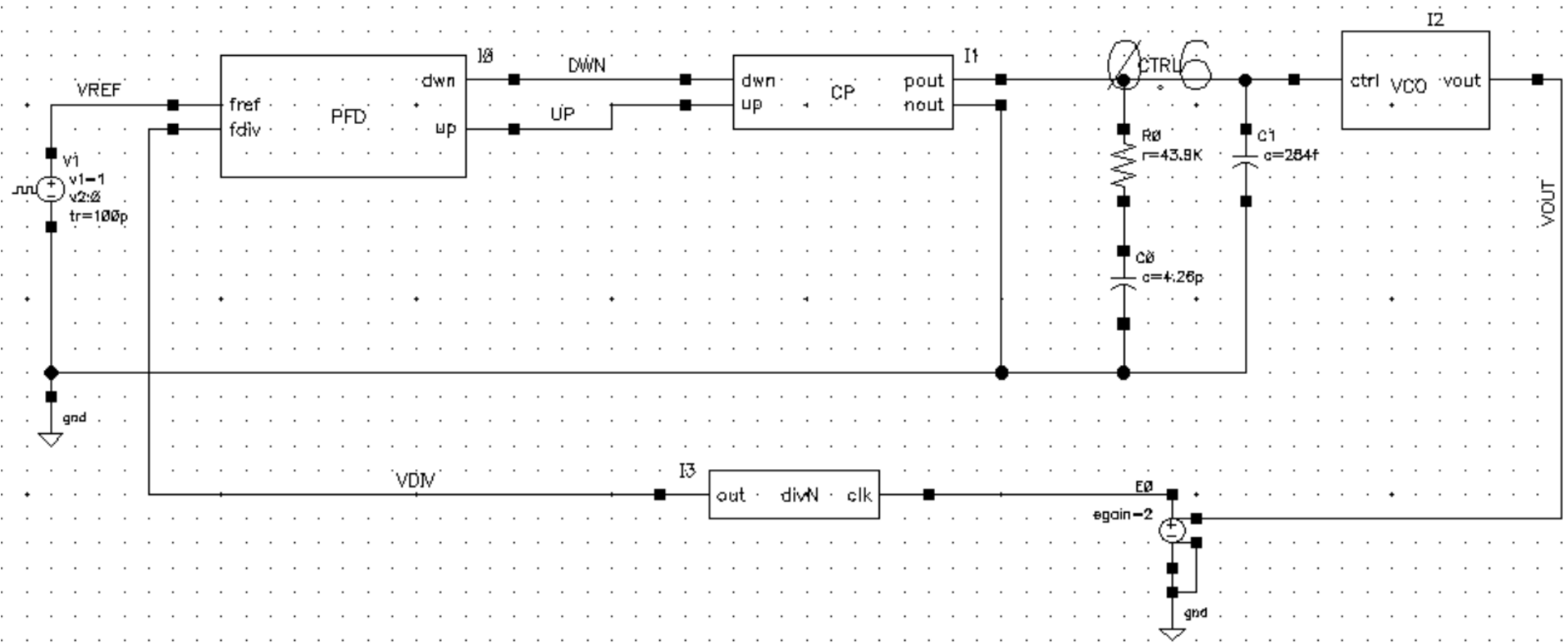
$$C_1 = \frac{1}{\omega_z R}; C_2 = \frac{C_1}{K_c}; \tag{4.8}$$

3. From aforementioned equations, we can determine the value for I_{CP}:

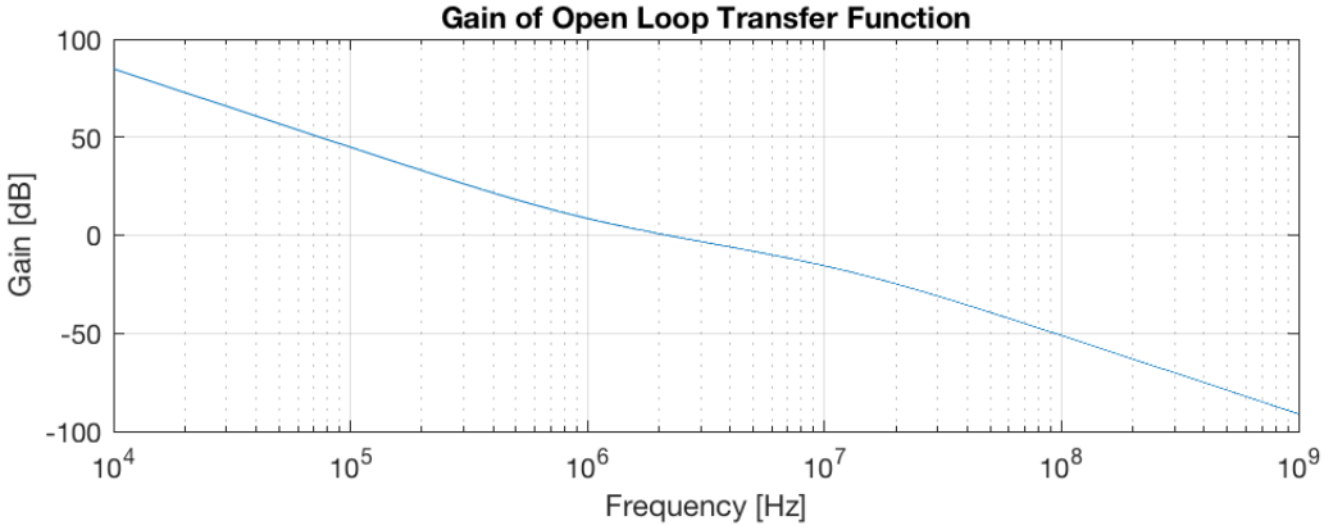
$$I_{CP} = \frac{2\pi C_2}{K_{VCO}} \cdot \omega_{ugb}^2 \cdot \sqrt{\frac{\omega_{p3}^2 + \omega_{ugb}^2}{\omega_z^2 + \omega_{ugb}^2}} \tag{4.9}$$

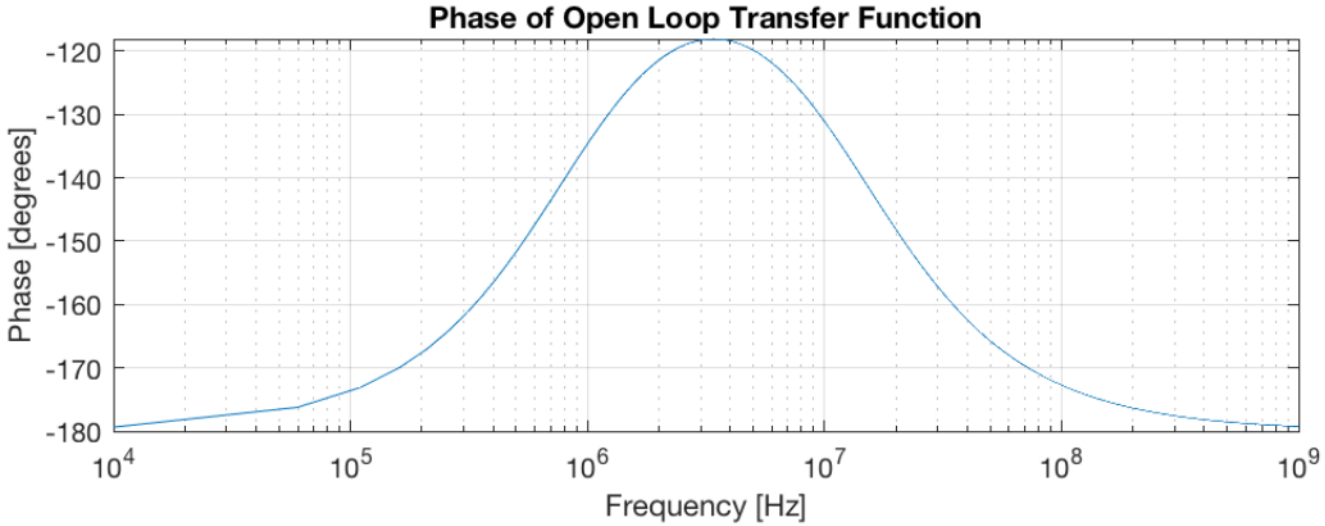
PLL Verilog AMS Modeling from Ashley

*Adapted from Ratan Thesis "Design of a Phase Locked Loop Based Clocking Circuit for High Speed Serial Link Applications"



MATLAB Simuation





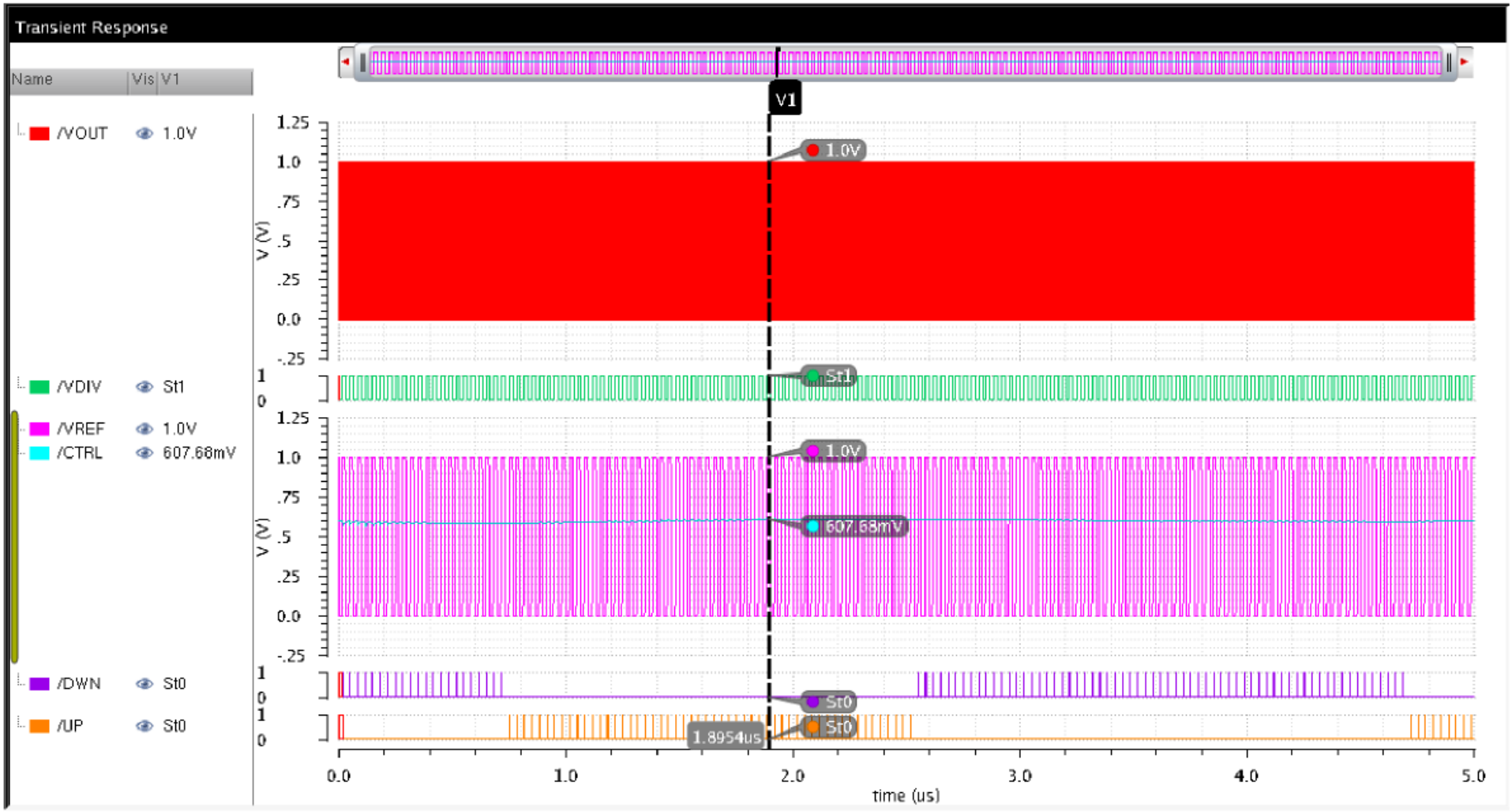

```
>> R1, C1, C2, Phase_Margin

R1 =

      4.386805741739931e+04

C1 =

      4.256896951639885e-12

C2 =

      2.837931301093257e-13

Phase_Margin =

  59.466816794831374
```

Transient Simulation

```
average(freq(v("/VOUT" ?result "tran") "rising" ?xName "time" ?mode "auto" ?threshold
0.0))
```

average(freq(v("/VOUT" ?res...

	Expression	Value
1	average(freq(v...	1.920E9



PLL Practical Design Example

	Spec.	Result
Kvco	< 300MHz/V	216 ~ 274MHz/V
Power	< 9mW	2.0 ~ 2.5mW @ 324MHz
Locking Time	< 30us	< 10usec
Wc	< (1/10)*Wi	22 ~ 45
Wz	> 3Wc	3.76 ~4.77
Wp	< Wc/3	3.94 ~ 4.64
Damping Factor	~ 1.0	1.006 ~ 1.133
Phase Margin	> 50	> 51.97
Jitter(peak-to-peak)	< 0.1 UI (~300ps)	VCO: ~50ps, PLL: ~65ps
Jitter_rms	10^{-7} BER (~30ps)	VCO: ~7.5ps, PLL: ~11 ps

- ICP = 16uA, Rz=21.8k, Cz=29.1pF, Cp=1.77pF

Behavioral Model

- Open-Loop Transfer Function

$$TF(s) = \frac{I_{CP} K_{VCO}}{2\pi N} \frac{1 + sR_z C_z}{s^2 (C_z + C_p)(1 + sR_z C_p)}$$

- Natural Frequency (Wn)

$$\omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{2\pi C_z N}}$$

- Damping Factor (ζ)

$$\zeta = \frac{R_z}{2} \sqrt{\frac{C_z I_{CP} K_{VCO}}{2\pi N}}$$

- Crossover Frequency (Wc)

$$\omega_c = \frac{I_{CP} K_{VCO} R_z}{2\pi C_z N} \frac{C_z}{C_z + C_p}$$

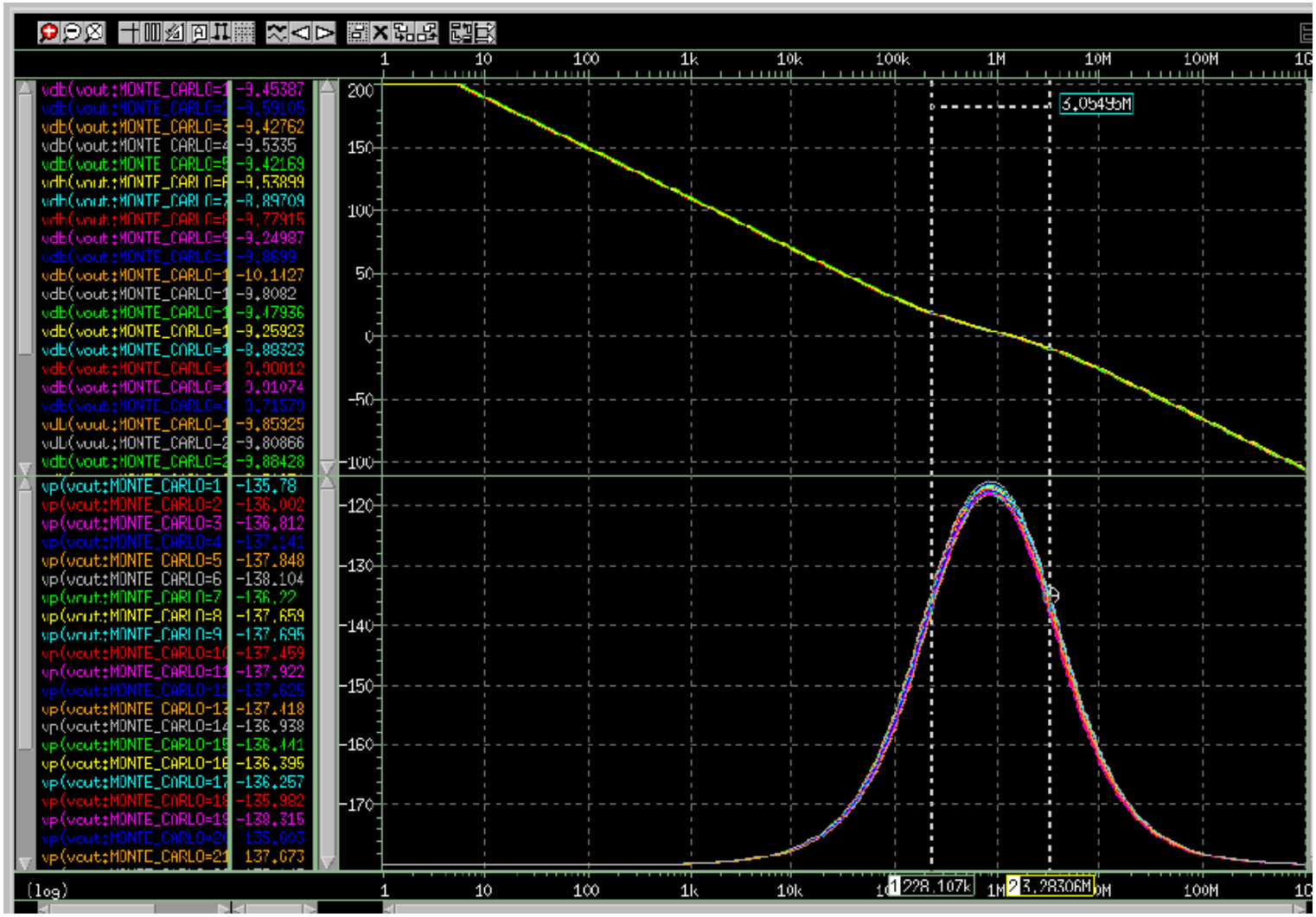
- Stability Criteria

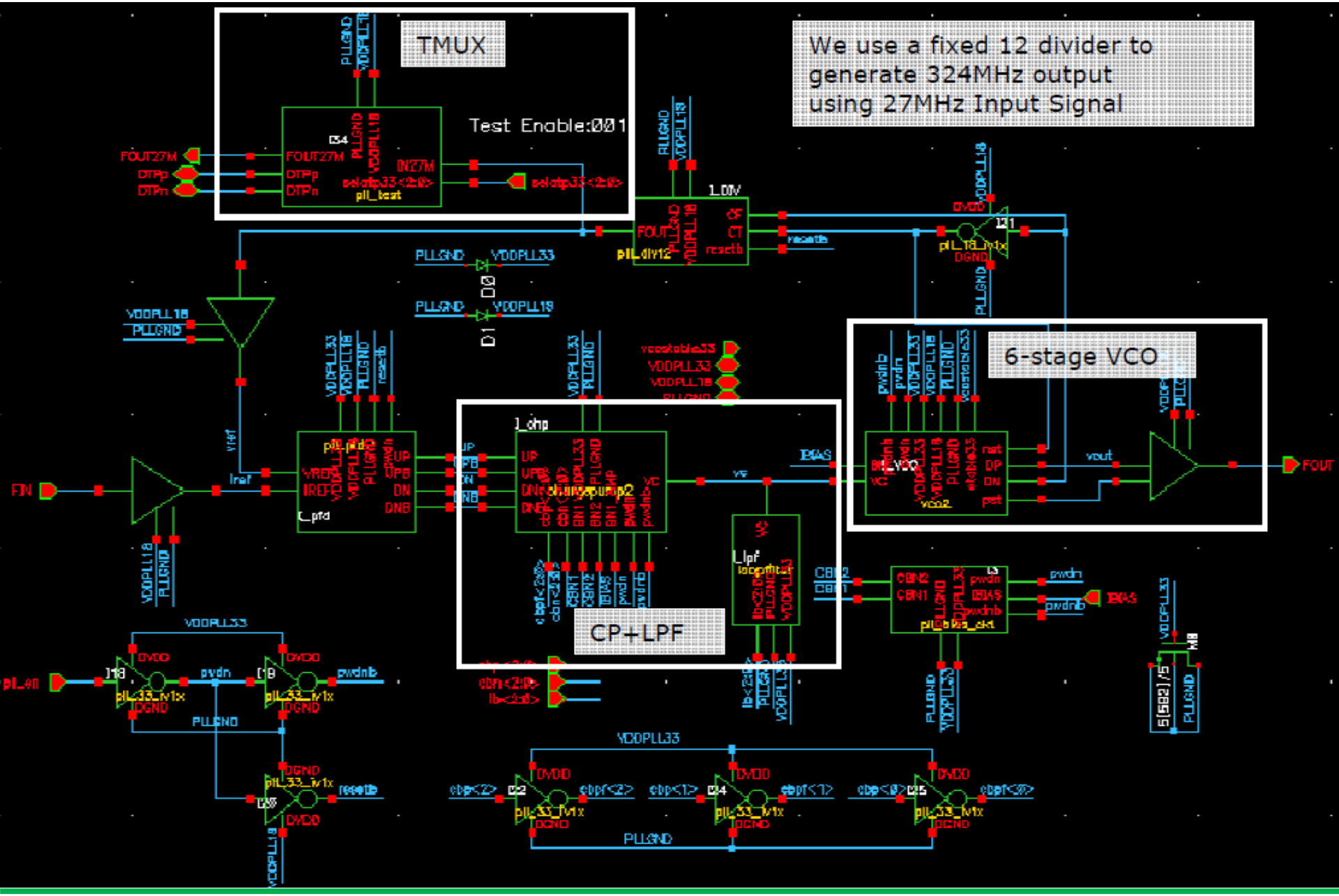
$$\omega_n^2 < \frac{\omega_{in}^2}{\pi (C_z R_z \omega_{in} + \pi)}$$

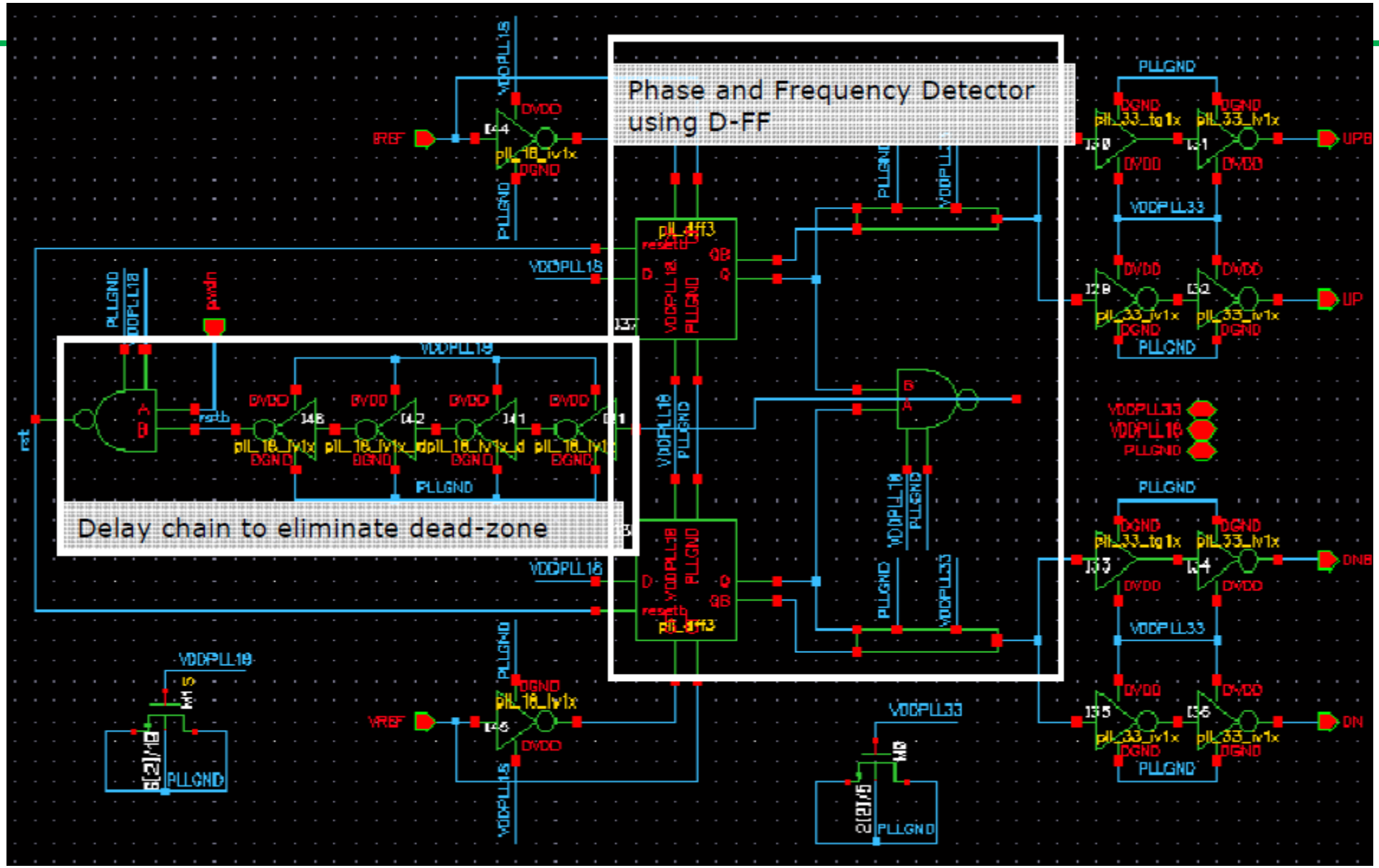
- Phase Margin

$$PM = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right)$$

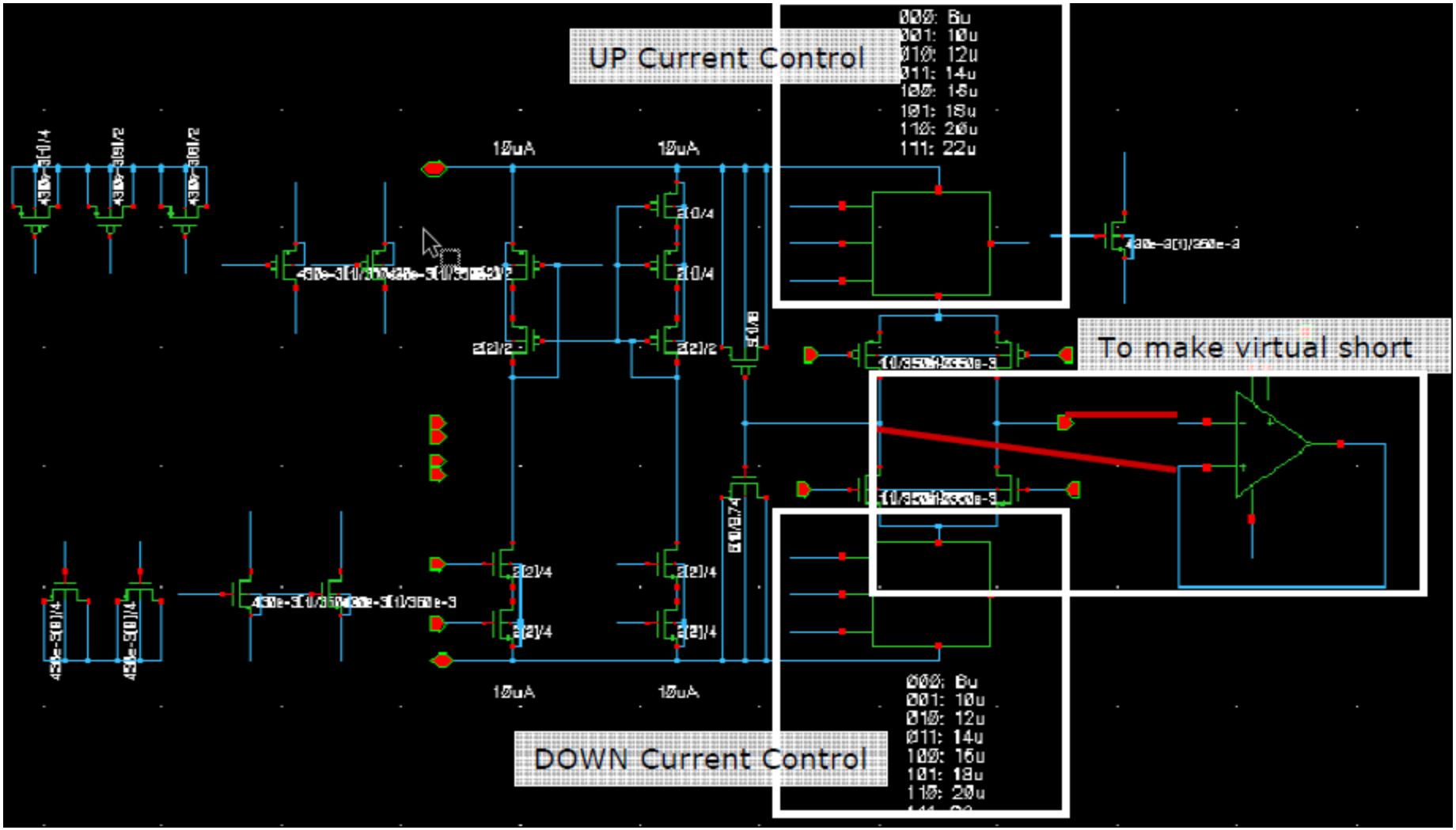
Behavioral Simulation

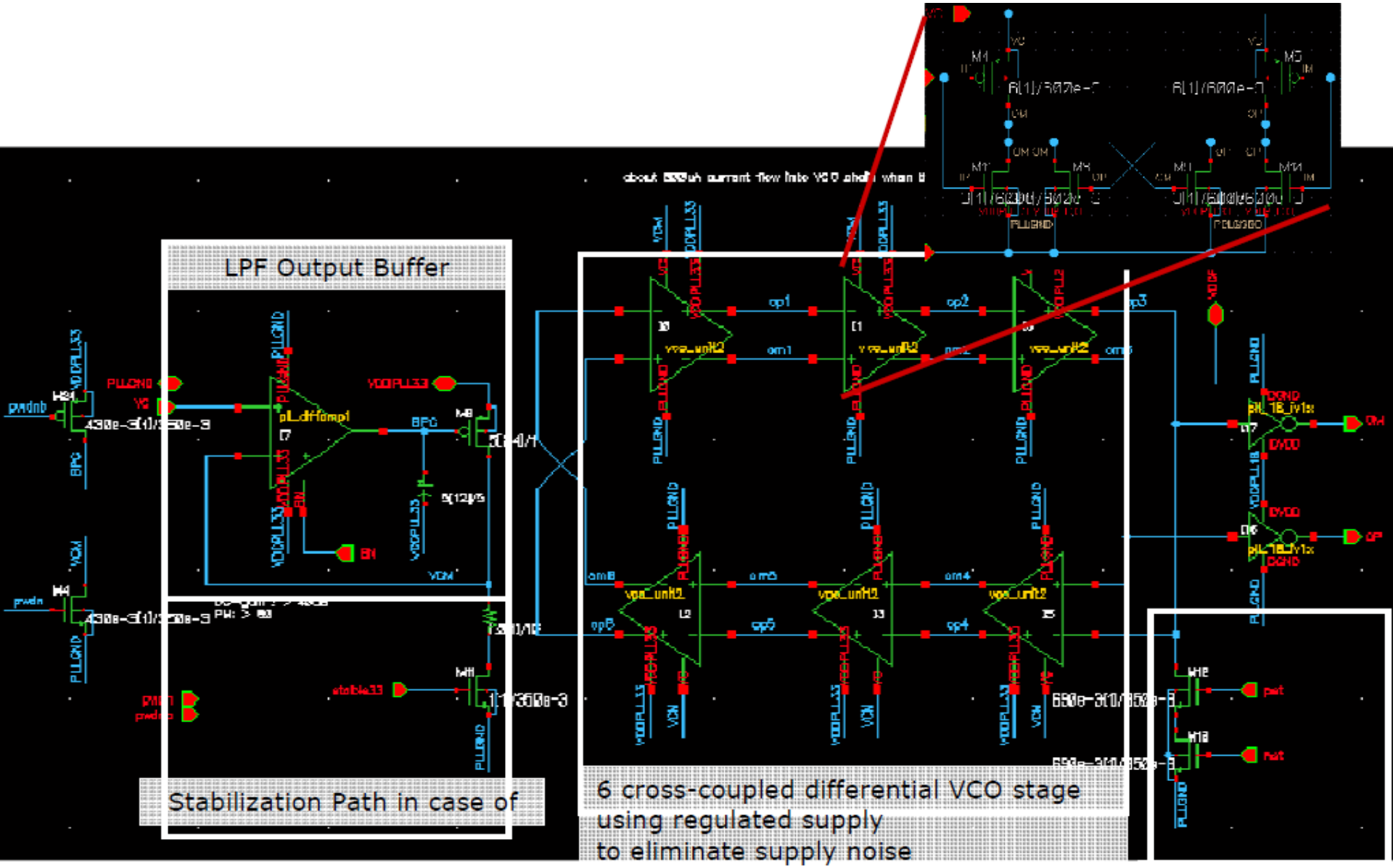


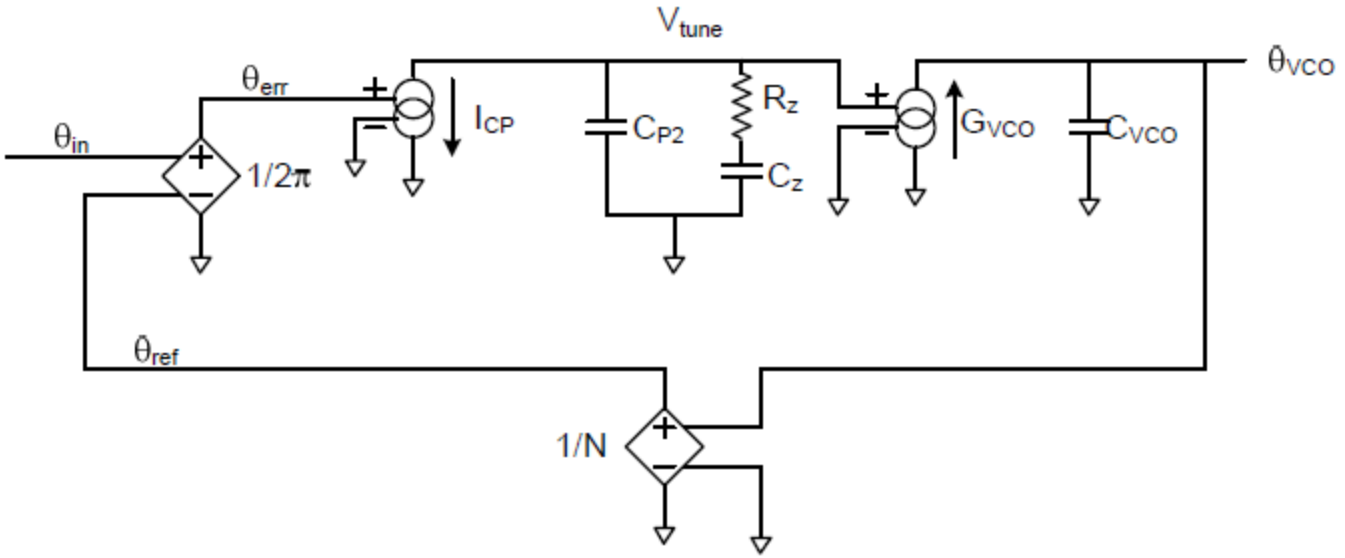

TMUX
Test Enable:001
We use a fixed 12 divider to generate 324MHz output using 27MHz Input Signal
6-stage VCO
CP+LPF
FIN
FOUT
FOUT27M
DTPp
DTPn
PLLGND
VDDPLL33
VDDPLL18
DVDD
DGND
pwdn
pwdnb
BIAS
vout
vref
iref

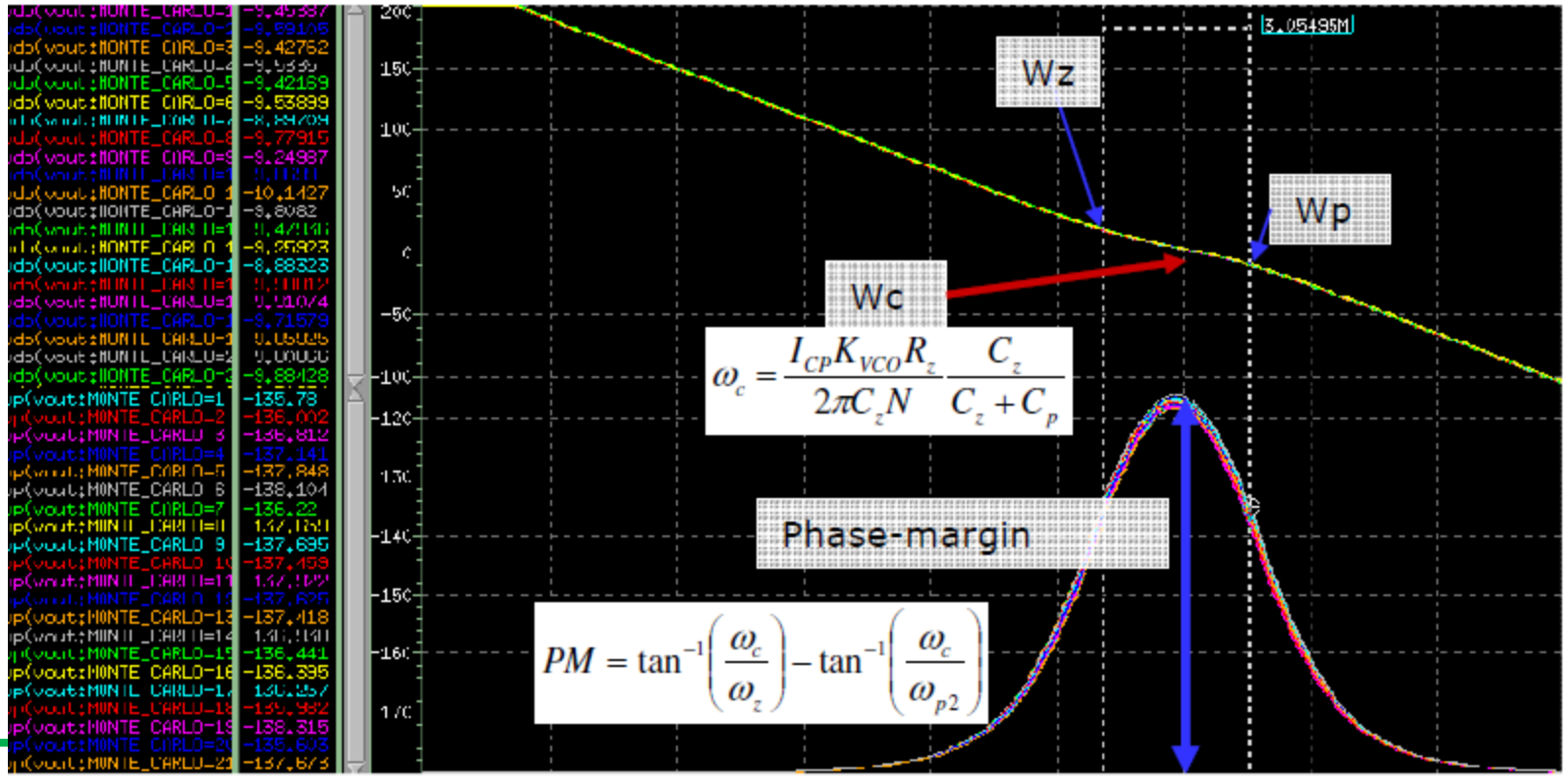

Phase and Frequency Detector using D-FF
Delay chain to eliminate dead-zone
VDDPLL18
VDDPLL33
PLLGND
DVDD
DGND
VREF
UPB
UP
DNB
DN
rst
pwdn
rstb

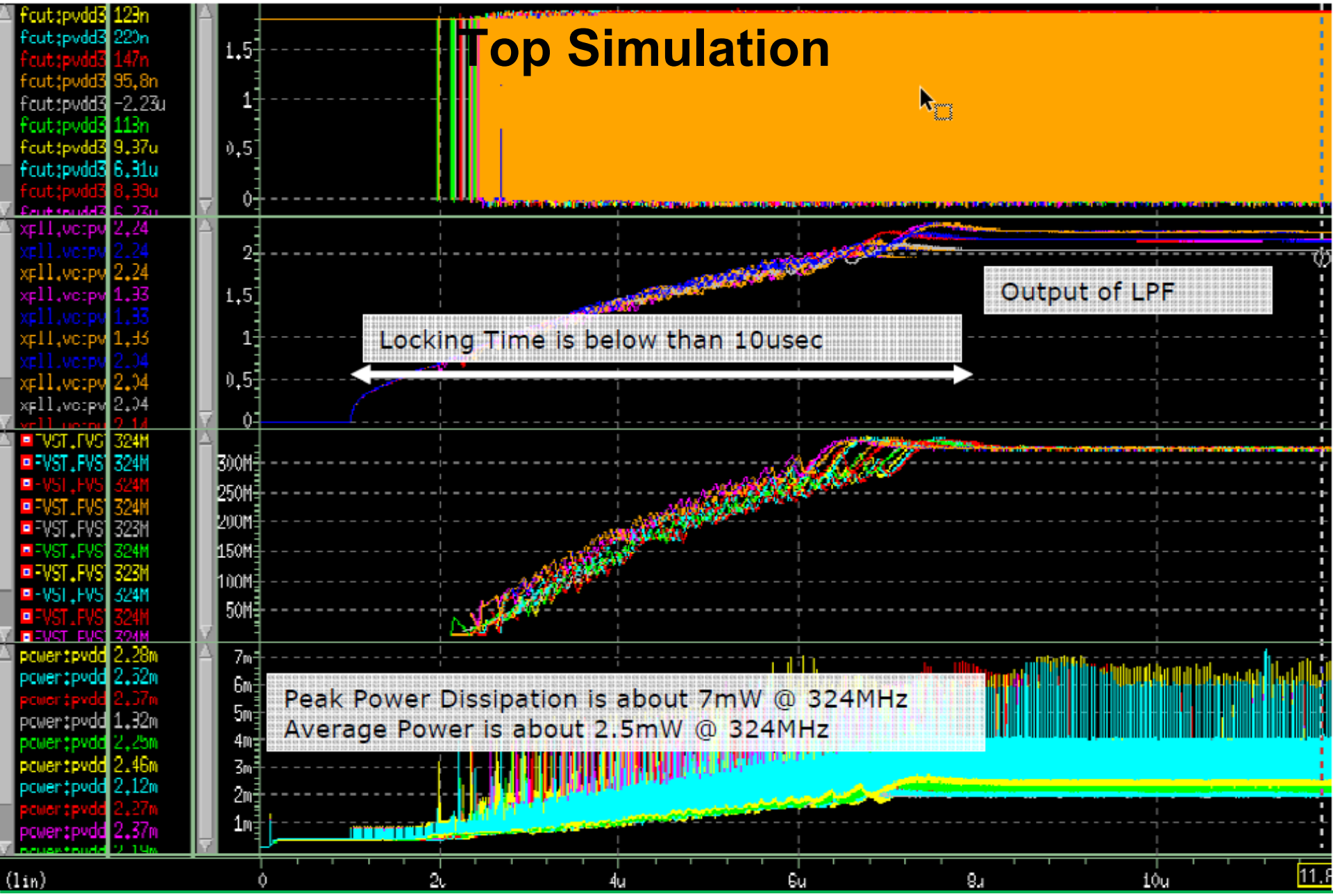
Charge Pump


UP Current Control
000: 8u
001: 10u
010: 12u
011: 14u
100: 16u
101: 18u
110: 20u
111: 22u
10uA
10uA
To make virtual short
DOWN Current Control
000: 8u
001: 10u
010: 12u
011: 14u
100: 16u
101: 18u
110: 20u
10uA
10uA


LPF Output Buffer
Stabilization Path in case of
6 cross-coupled differential VCO stage
using regulated supply
to eliminate supply noise
Star-up Circuit
for 11 state


Vtune
θvco
θerr
θin
1/2π
ICP
CP2
Rz
Cz
Gvco
Cvco
θref
1/N


Wz
Wp
Wc
Phase-margin
$\omega_c = \frac{I_{CP} K_{VCO} R_z}{2\pi C_z N} \frac{C_z}{C_z + C_p}$
$PM = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right)$


Top Simulation
Output of LPF
Locking Time is below than 10usec
Peak Power Dissipation is about 7mW @ 324MHz
Average Power is about 2.5mW @ 324MHz

Top Simulation