EE230-02 RFIC II
Fall 2018

Lecture 18: Phase-Locked Loops 3

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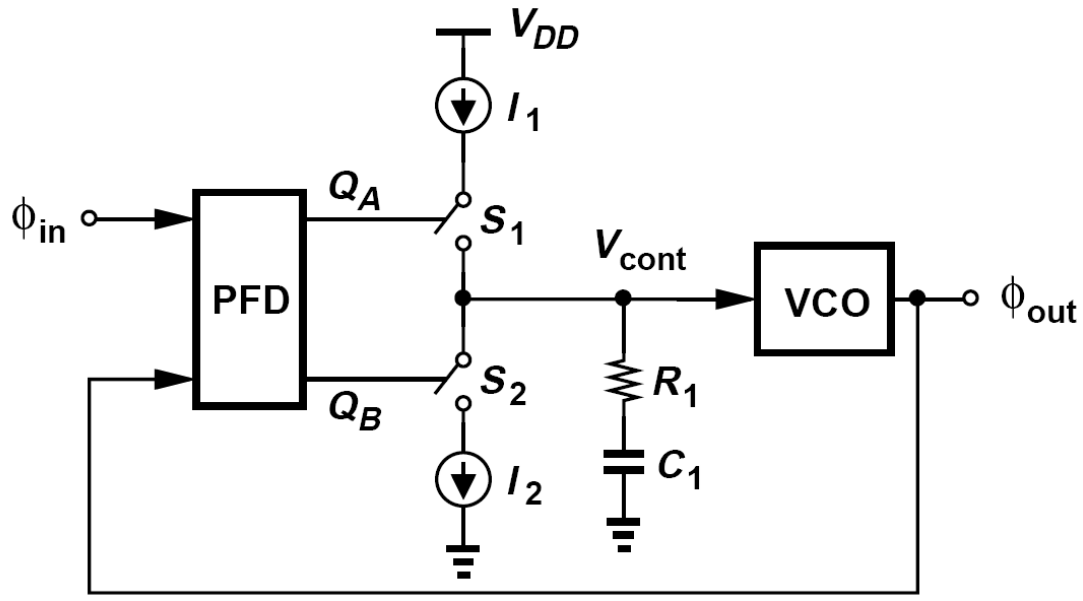
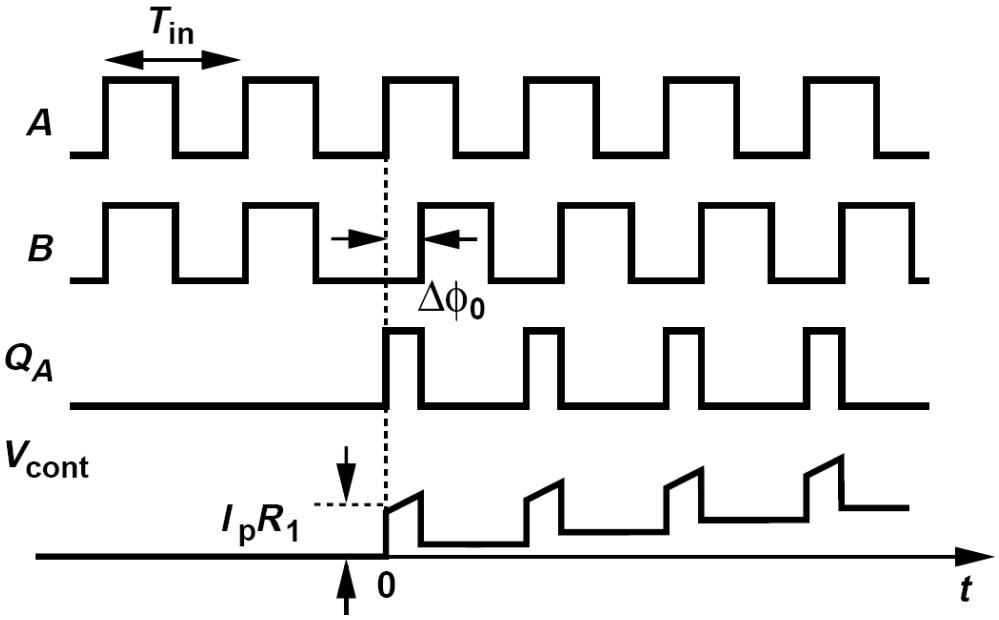
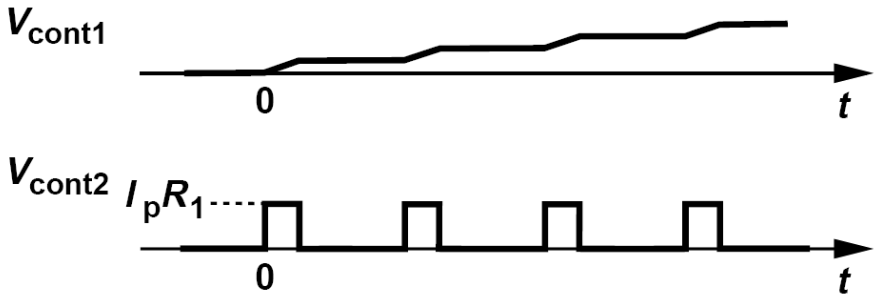
Charge-Pump PLL



- If one of the integrators becomes lossy, the system can be stabilized.
- This can be accomplished by inserting a resistor in series with C_1. The resulting circuit is called a “Charge Pump PLL” (CPPLL)

Computation of the Transfer Function





Approximate the pulse sequence by a step of height $(I_pR_1)[\Delta\Phi_0/(2\pi)]$:

$$V_{cont}(t) = \frac{\Delta\phi_0}{2\pi}\frac{I_p}{C_1}tu(t) + \frac{\Delta\phi_0}{2\pi}I_pR_1u(t)$$

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_p}{2\pi}\left(\frac{1}{C_1 s} + R_1\right) \Rightarrow$$

$$H(s) = \frac{\frac{I_pK_{VCO}}{2\pi C_1}(R_1C_1s+1)}{s^2 + \frac{I_p}{2\pi}K_{VCO}R_1s + \frac{I_p}{2\pi C_1}K_{VCO}}$$

Stability of Charge-Pump PLL

Write the denominator as $s^2 + 2\zeta\omega_n s + \omega_n 2$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi}}$$

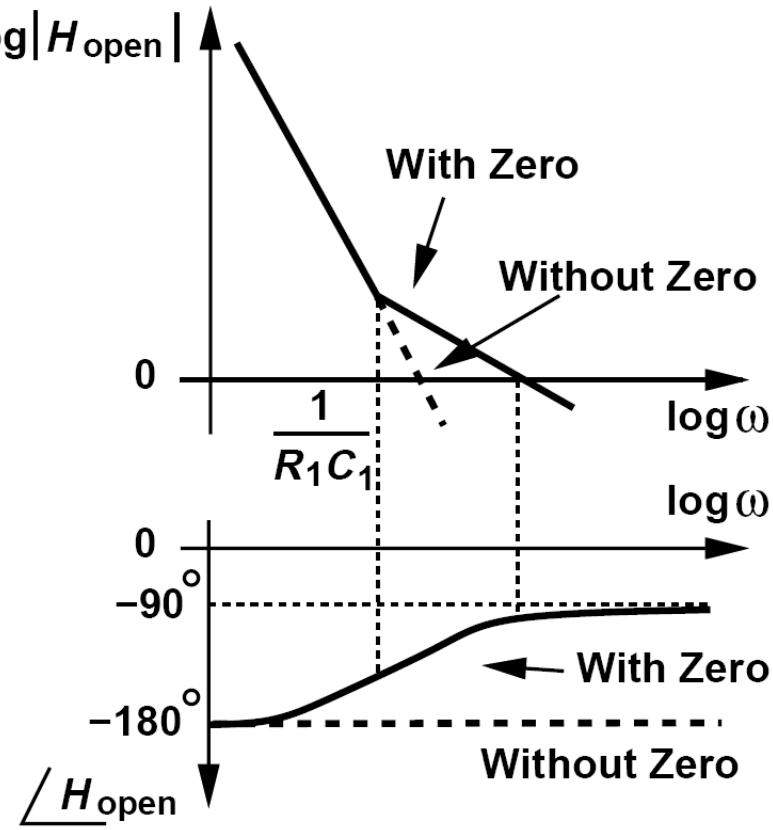
$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}}.$$

- As C_1 increases, so does ζ --- a trend opposite to that observed in type-I PLL
- No trade-off between stability and ripple amplitude

Closed-loop poles are given by

$$\omega_{p1,2} = [-\zeta \pm \sqrt{\zeta^2 - 1}]\omega_n$$

A closed-loop zero at $-\omega_n / 2\zeta$



$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_p}{2\pi}\left(\frac{R_1 C_1 s + 1}{C_1 s}\right)$$

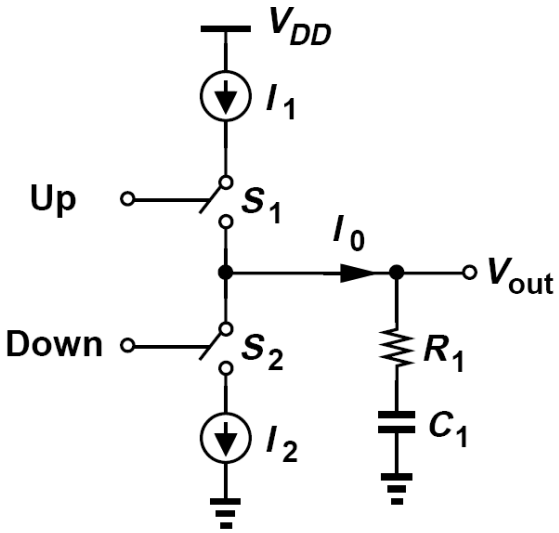
Frequency-Multiplying CPPLL

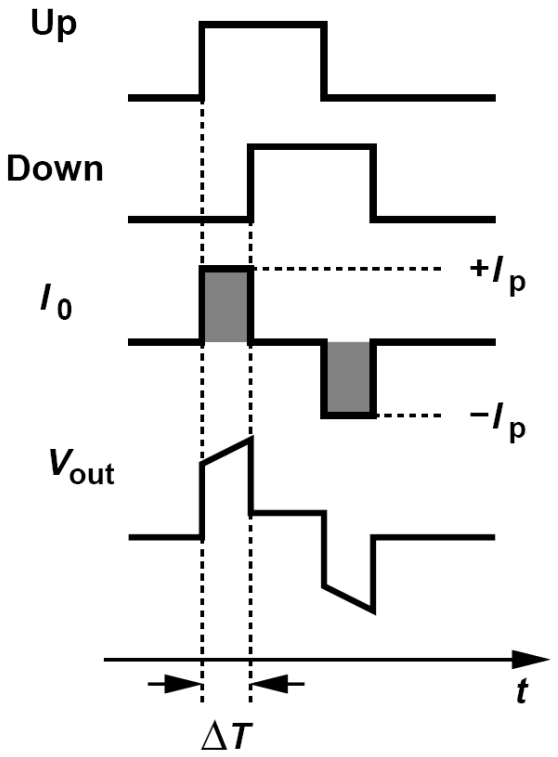
$$H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_1}(R_1 C_1 s + 1)}{s^2 + \frac{I_p}{2\pi}\frac{K_{VCO}}{M}R_1 s + \frac{I_p}{2\pi C_1}\frac{K_{VCO}}{M}}$$

$$\begin{aligned} \zeta &= \frac{R_1}{2}\sqrt{\frac{I_p C_1}{2\pi}\frac{K_{VCO}}{M}} \\ \omega_n &= \sqrt{\frac{I_p}{2\pi C_1}\frac{K_{VCO}}{M}}. \end{aligned}$$

Division of K_{VCO} by M makes the loop less stable, requiring that I_p and/or C_1 be larger.

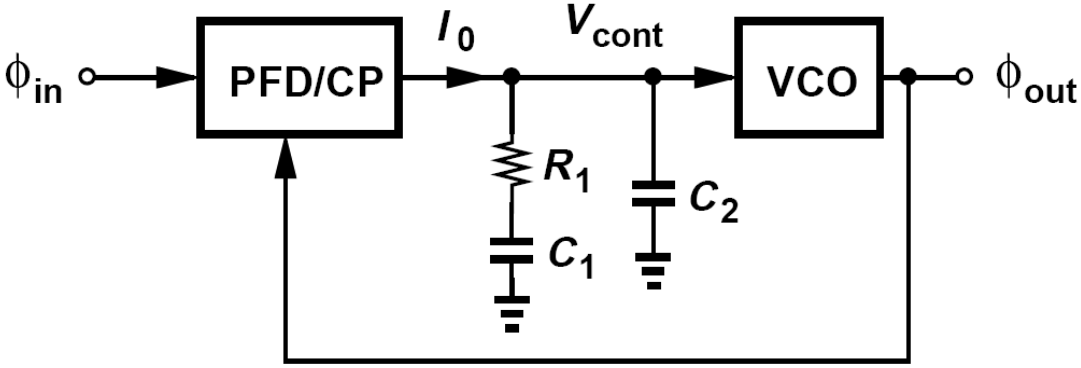
Higher-Order Loops: Drawback of Previous Loop Filter

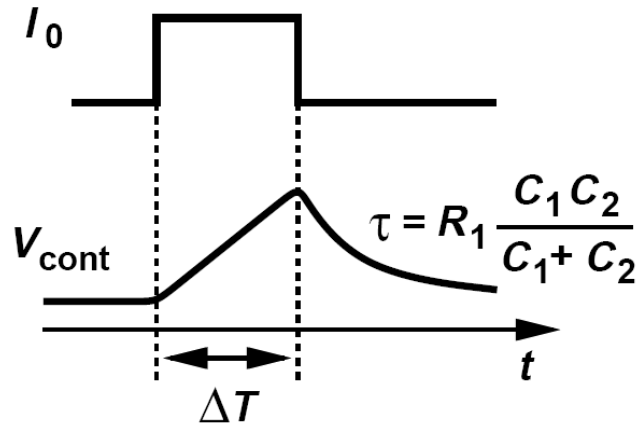




- The loop filter consisting of R_1 and C_1 proves inadequate because, even in the locked condition, it does not suppress the ripple sufficiently.
- The ripple consists of positive ad negative pulses of amplitude I_pR_1 occurring every T_{in} seconds.

Addition of Second Capacitor to Loop Filter





- Add C_2

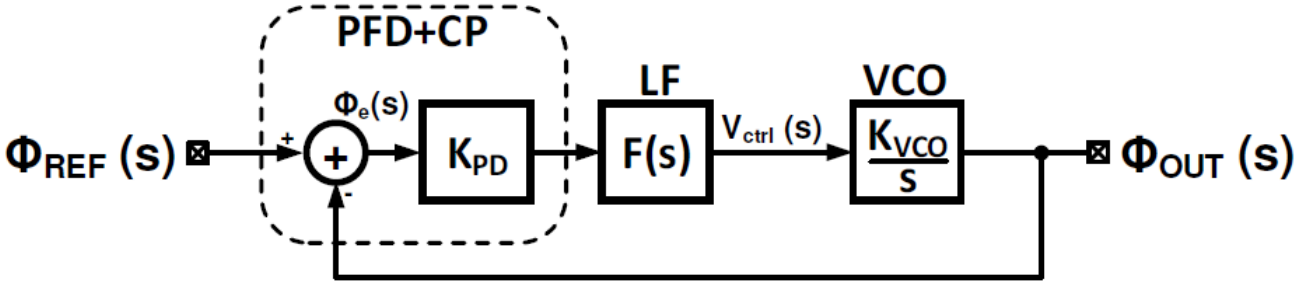
$$\mathrm{PM} \approx \tan^{-1}(4\zeta^2) - \tan^{-1}\left(4\zeta^2 \frac{C_{eq}}{C_1}\right)$$

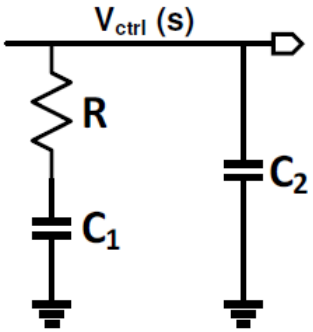
We therefore choose $\zeta = 0.8$ -1 and $C_2 \approx 0.1C_1$ in typical designs.

An upper bound derived for R_1 :

$$R_1^2 \leq \frac{2\pi}{I_p K_{VCO} C_{eq}}$$

Modeling of Charge-Pump PLL





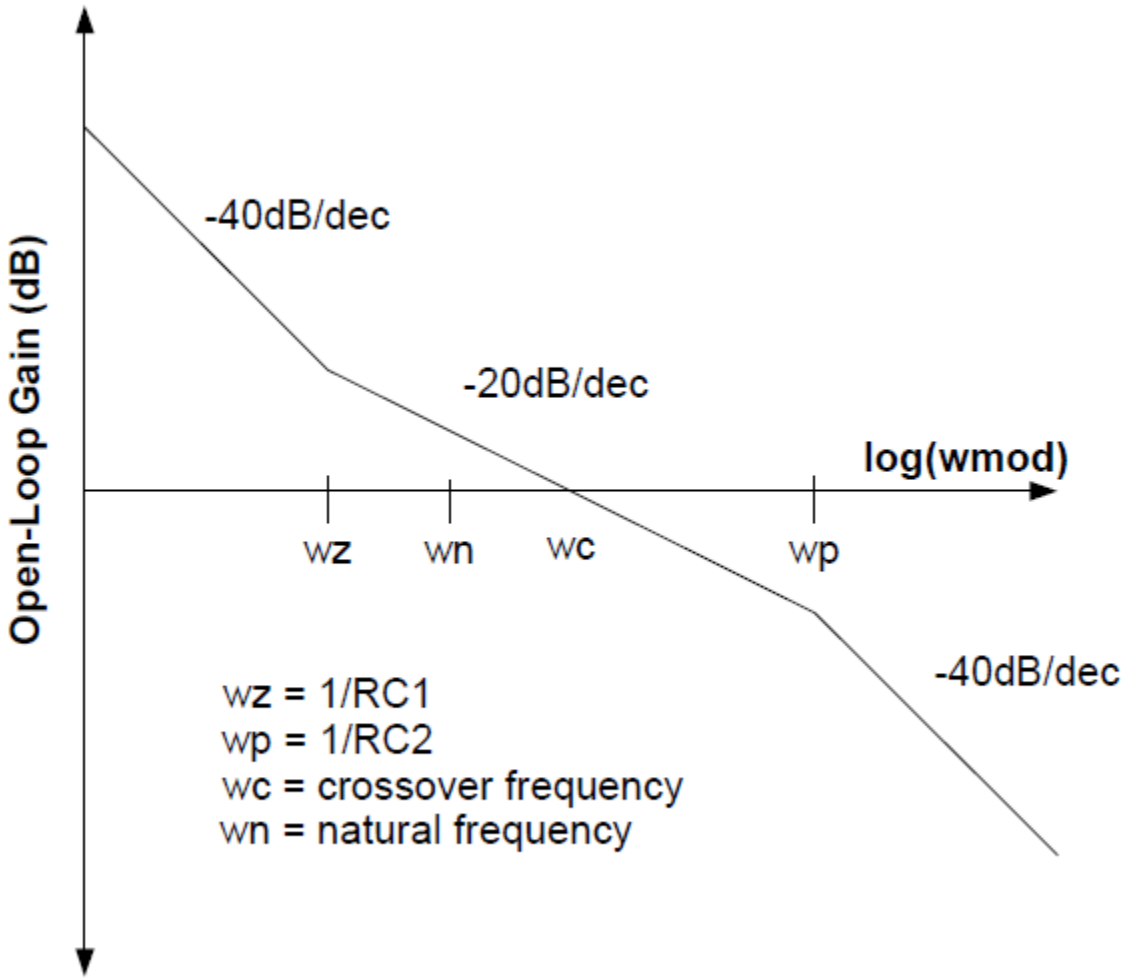
$$LG(s) = K_{PD} \cdot F(s) \cdot \frac{K_{VCO}}{s}$$

$$= K_{PD} \cdot K_{VCO} \cdot \frac{s + \frac{1}{RC_1}}{C_2 s^2 \left(s + \frac{C_1 + C_2}{RC_1C_2} \right)}$$

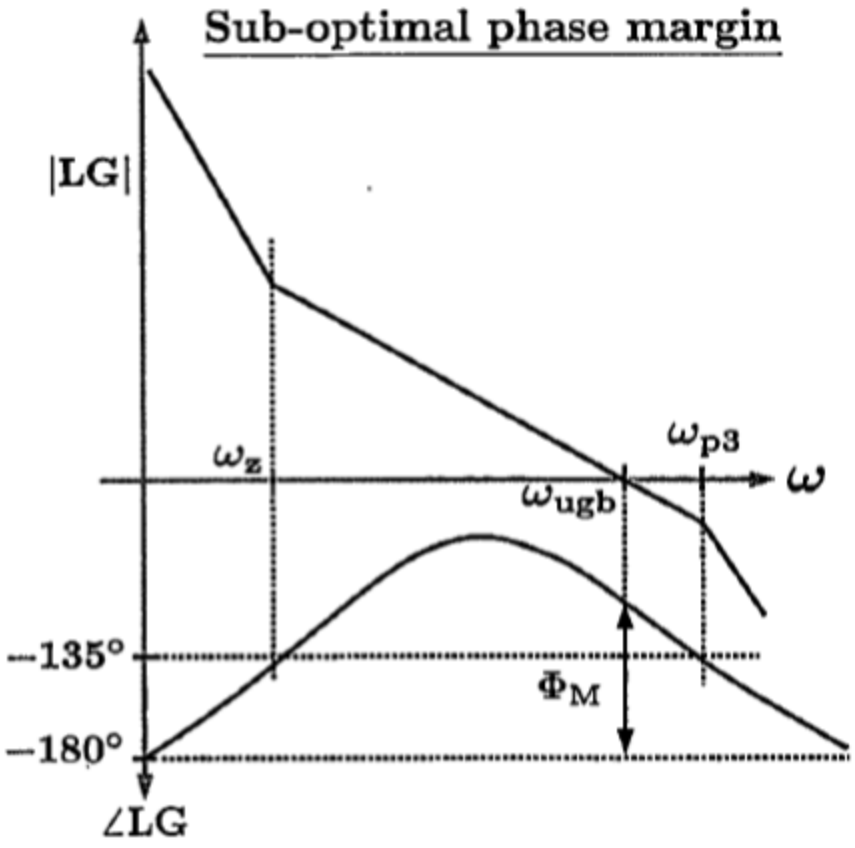
$$\omega_z = \frac{1}{RC_1};\ \omega_{p1} = \omega_{p2} = 0; \omega_{p3} = \frac{C_1 + C_2}{RC_1C_2}$$

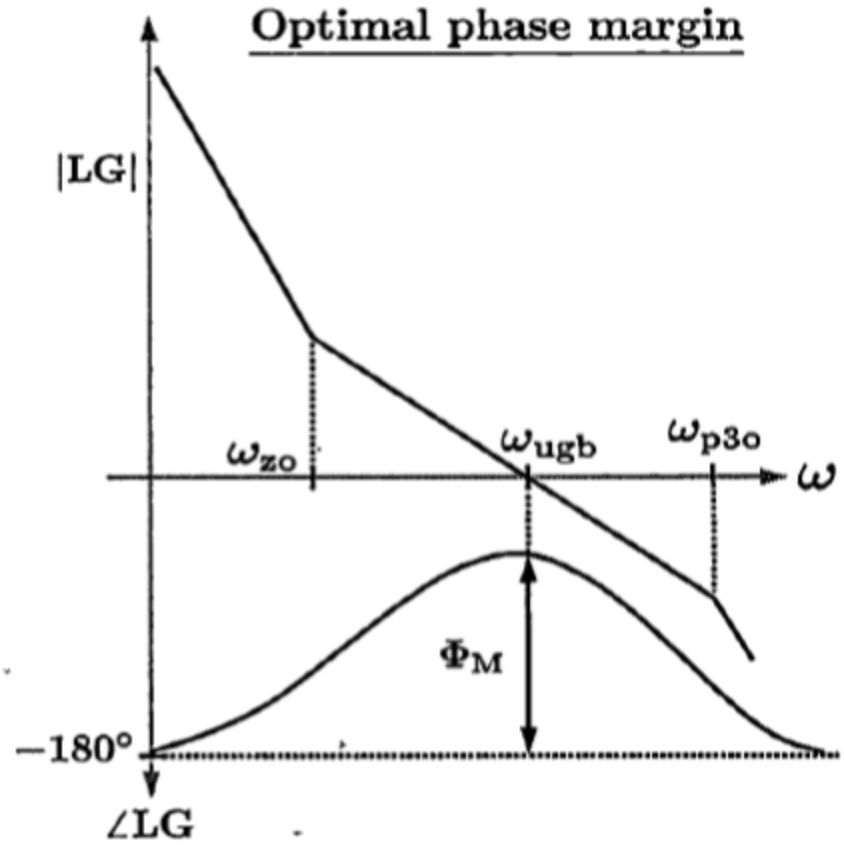
$$\phi_M = \arctan\left(\frac{\omega_{ugb}}{\omega_z}\right) - \arctan\left(\frac{\omega_{ugb}}{\omega_{p3}}\right)$$

Open Loop Transfer Function



Loop Gain and Phase Margin





Linear Model of Charge-Pump PLL

$$LG(s) = K_{PD} \cdot F(s) \cdot \frac{K_{VCO}}{s}$$
$$= K_{PD} \cdot K_{VCO} \cdot \frac{s + \frac{1}{RC_1}}{C_2 s^2 \left(s + \frac{C_1 + C_2}{RC_1 C_2}\right)}$$

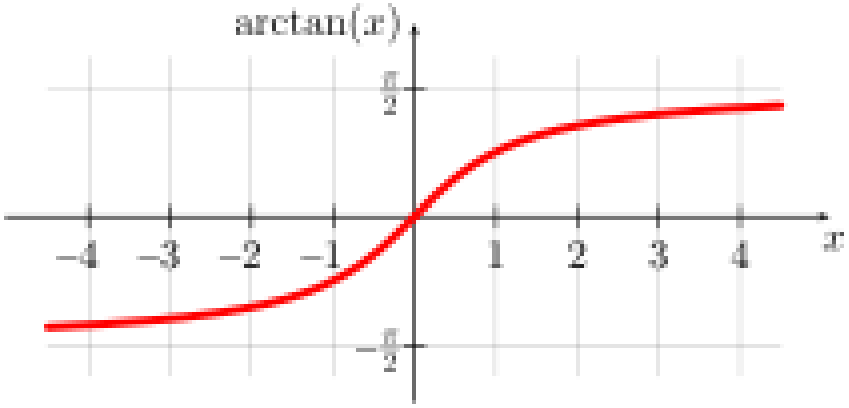
$$\omega_z = \frac{1}{RC_1};\ \omega_{p1} = \omega_{p2} = 0; \omega_{p3} = \frac{C_1 + C_2}{RC_1 C_2}$$

$$\phi_M = \arctan\left(\frac{\omega_{ugb}}{\omega_z}\right) - \arctan\left(\frac{\omega_{ugb}}{\omega_{p3}}\right)$$

$$\omega_{ugb} = \omega_z \sqrt{\frac{C_1}{C_2} + 1}$$

$$\phi_{M\_max} = \arctan\left(\sqrt{\frac{C_1}{C_2} + 1}\right) - \arctan\left(\frac{1}{\sqrt{\frac{C_1}{C_2} + 1}}\right)$$

What is arctangent ?



If C_1/C_2 = 10, then Phase Margin is

arctan(sqrt(11)) = 73.2213451 degree — arctan(1 / sqrt(11)) = 16.7786549 degree = **57 degree**

Loop Filter Design Procedure

1. Choose desired bandwidth ω_{ugb}, phase margin ϕ_M and resistor R according to specification. Then calculate the K_c from Eq. 4.6:

$$K_c = \frac{C_1}{C_2} = 2(\tan^2(\phi_M) + \tan(\phi_M \sqrt{\tan^2(\phi_M) + 1})) \tag{4.6}$$

2. From Eq. 4.4 we have:

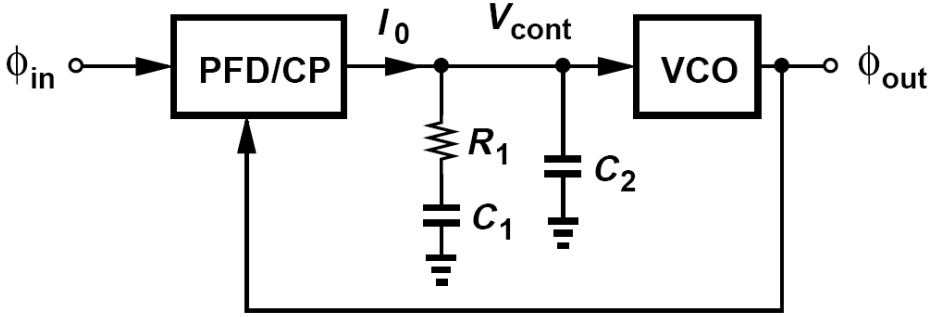
$$\omega_z = \frac{\omega_{ubg}}{\sqrt{\frac{C_1}{C_2} + 1}} \tag{4.7}$$

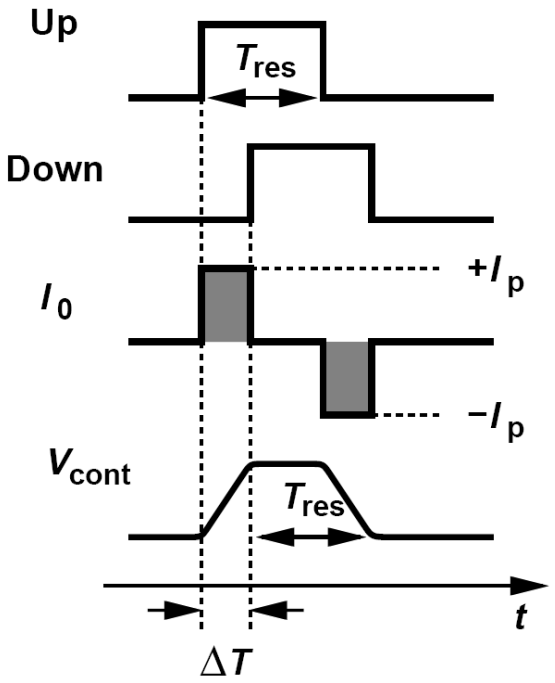
$$C_1 = \frac{1}{\omega_z R}; C_2 = \frac{C_1}{K_c}; \tag{4.8}$$

3. From aforementioned equations, we can determine the value for I_{CP}:

$$I_{CP} = \frac{2\pi C_2}{K_{VCO}} \cdot \omega_{ugb}^2 \cdot \sqrt{\frac{\omega_{p3}^2 + \omega_{ugb}^2}{\omega_z^2 + \omega_{ugb}^2}} \tag{4.9}$$

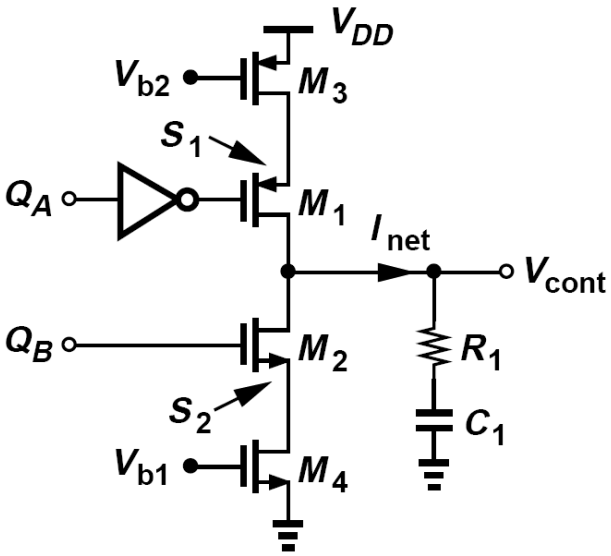
PFD/CP Nonidealities: Up and Down Skew and Width Mismatch

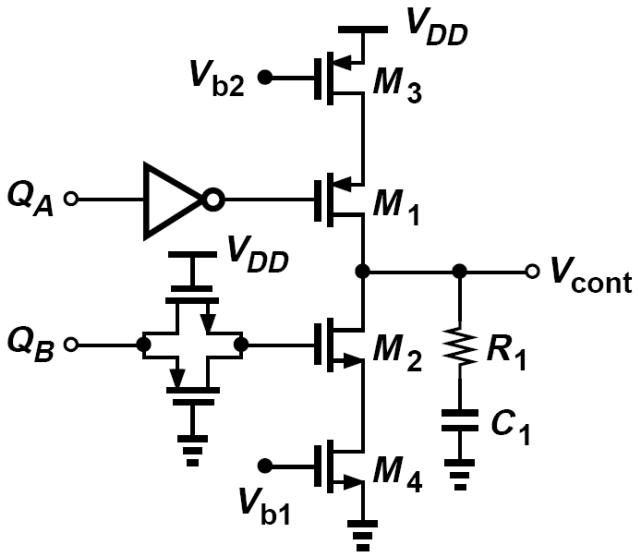


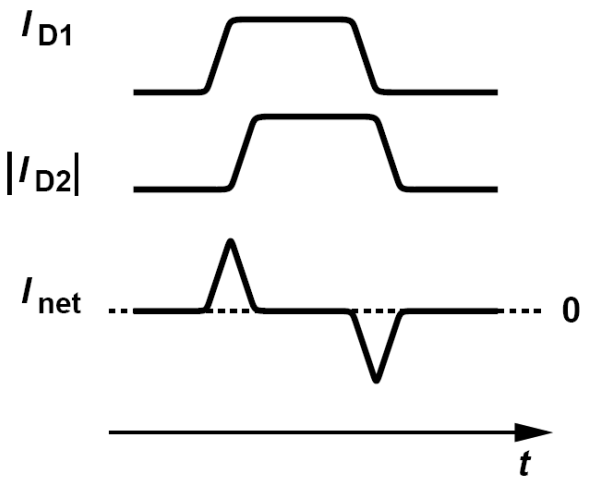


- The width of the pulse is equal to the width of the reset pulses, T_{res} (about 5 gate delays), plus ΔT.
- The height of the pulse is equal to $\Delta T\, I_p/C_2$

Systematic Skew

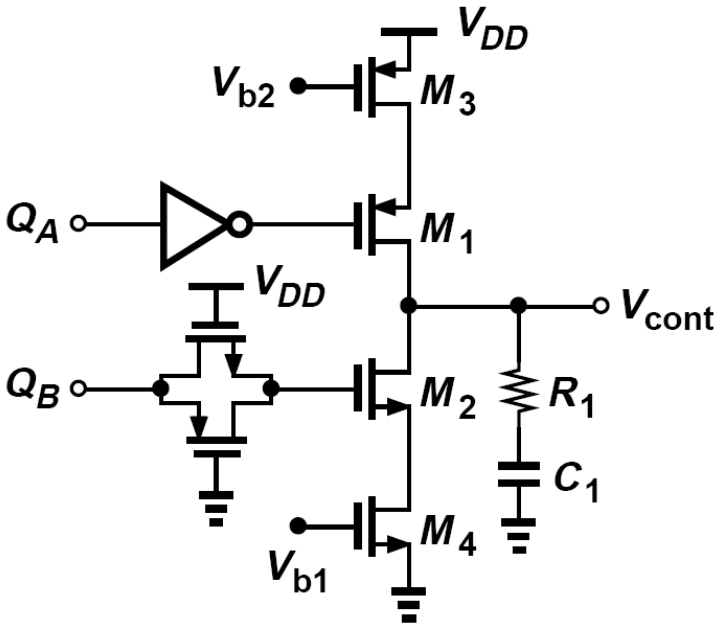






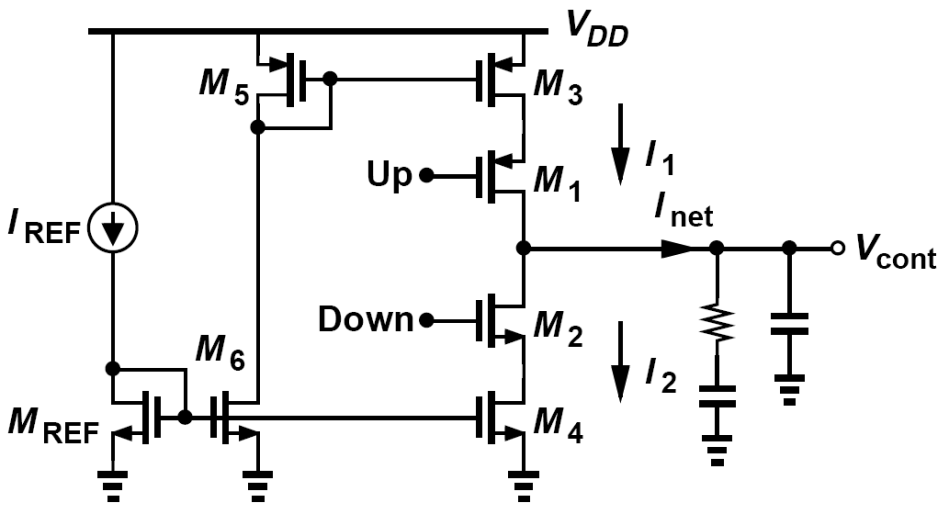
- The delay of the inverter creates a skew between the Up and Down pulses.
- To alleviate this issue, a transmission gate can be inserted
- The quantity of interest is in fact the skew between the Up and Down current waveforms, or ultimately, the net current injected into the loop filter

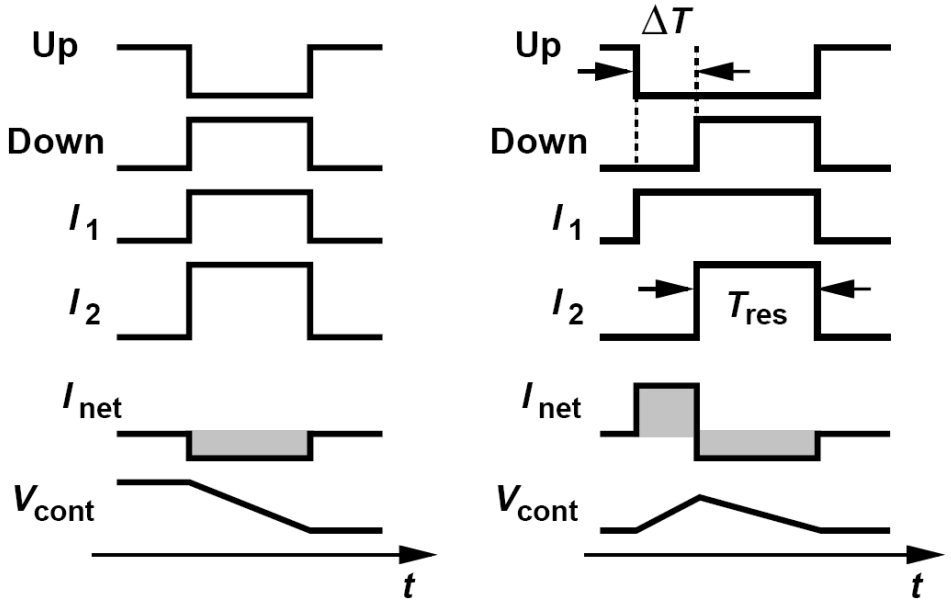
Voltage Compliance



- Desirable for V_{out} to swing as close to the supply rails as possible.
- Each current source requires a minimum drain-source voltage and each switch sustains a voltage drop.
- The output compliance is equal to V_{DD} minus two overdrive voltages and two switch drops

Random Mismatch Between Up and Down Currents





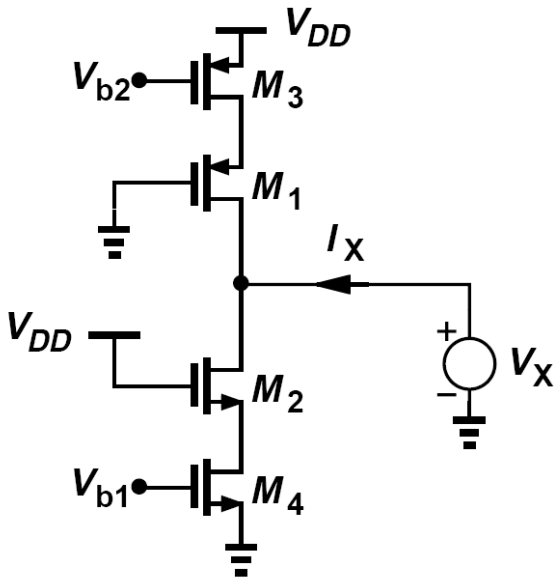
The net current is zero if:

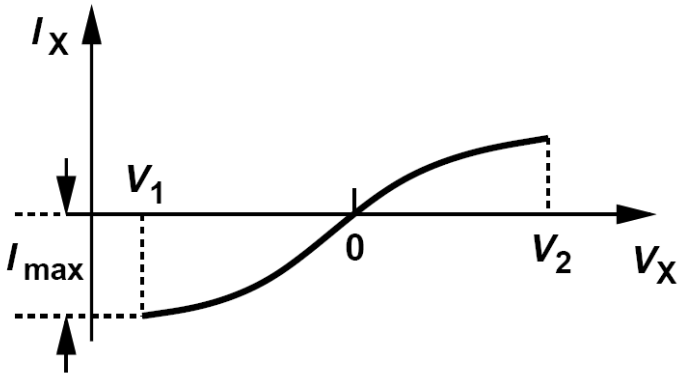
$$I_p \cdot \Delta T = \Delta I \cdot T_{res} \qquad \Delta T = T_{res}\frac{\Delta I}{I_p}$$

The ripple amplitude is equal to:

$$\Delta T \cdot I_p / C_2 = T_{res}\Delta I / C_2.$$

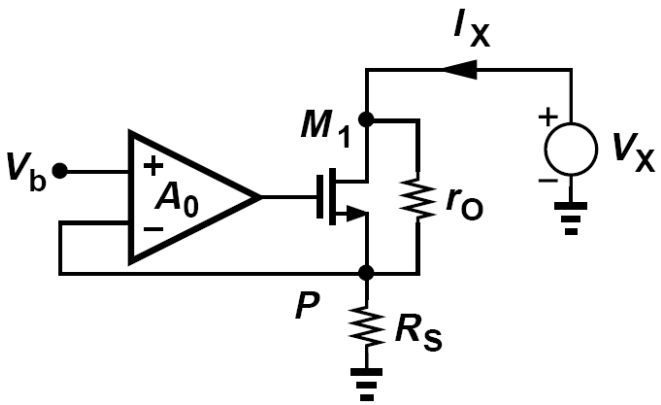
Channel Length Modulation Effect

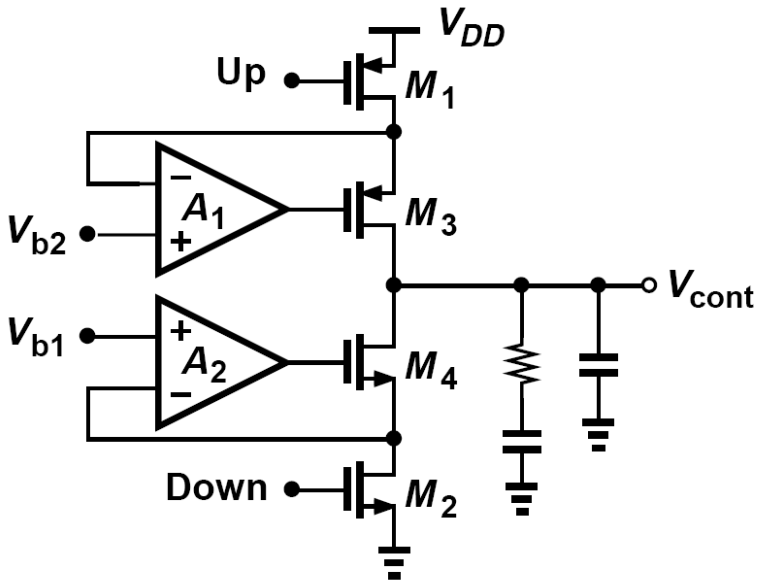




- Different output voltages inevitably lead to opposite changes in the drain-source voltages of the current sources, thereby creating a larger mismatch.
- The maximum departure of I_X from zero, I_{max}, divided by the nominal value of I_p quantifies the effect of channel-length modulation.

Circuit Techniques to deal with Channel Length Modulation Effect

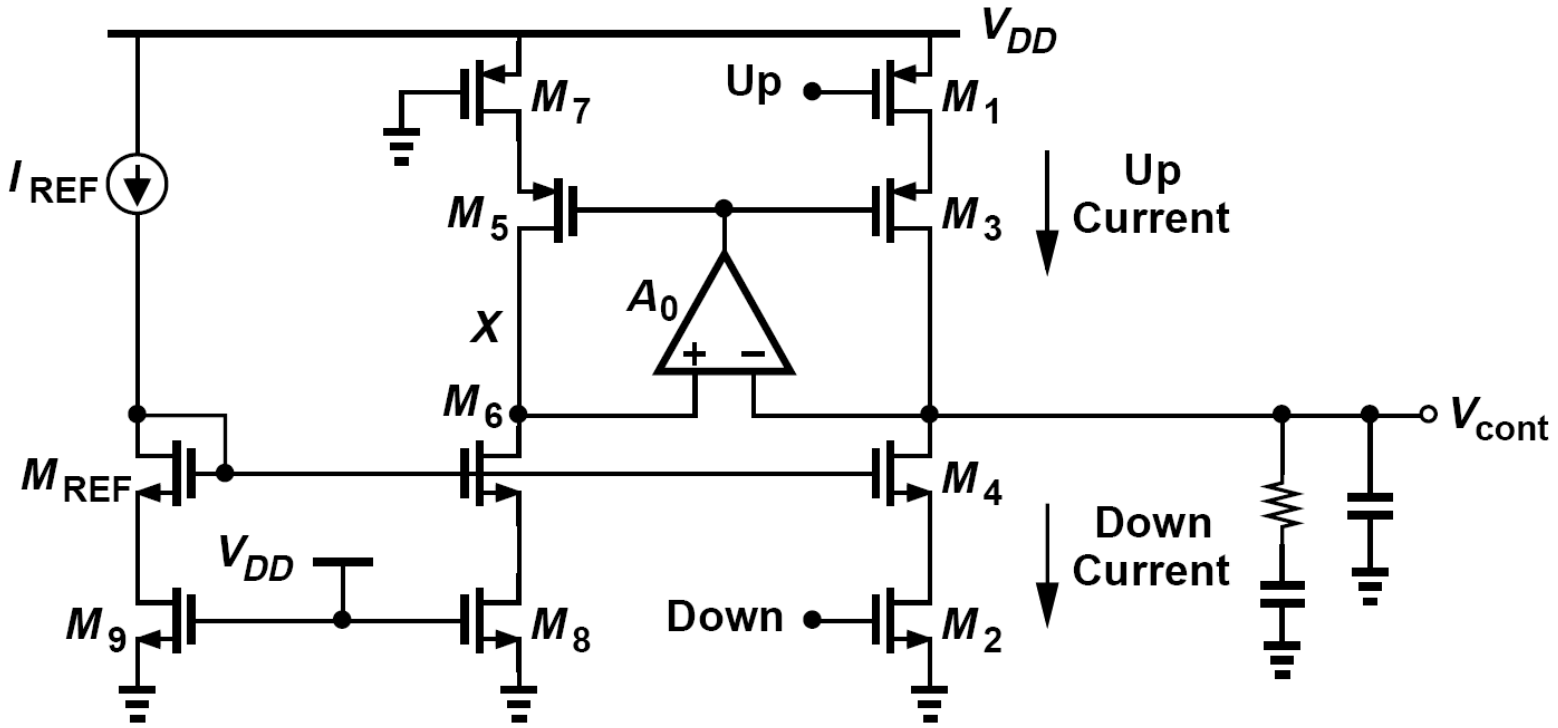




$$\frac{V_X}{I_X} = (1 + A_0) g_m r_O R_S + r_O + R_S$$

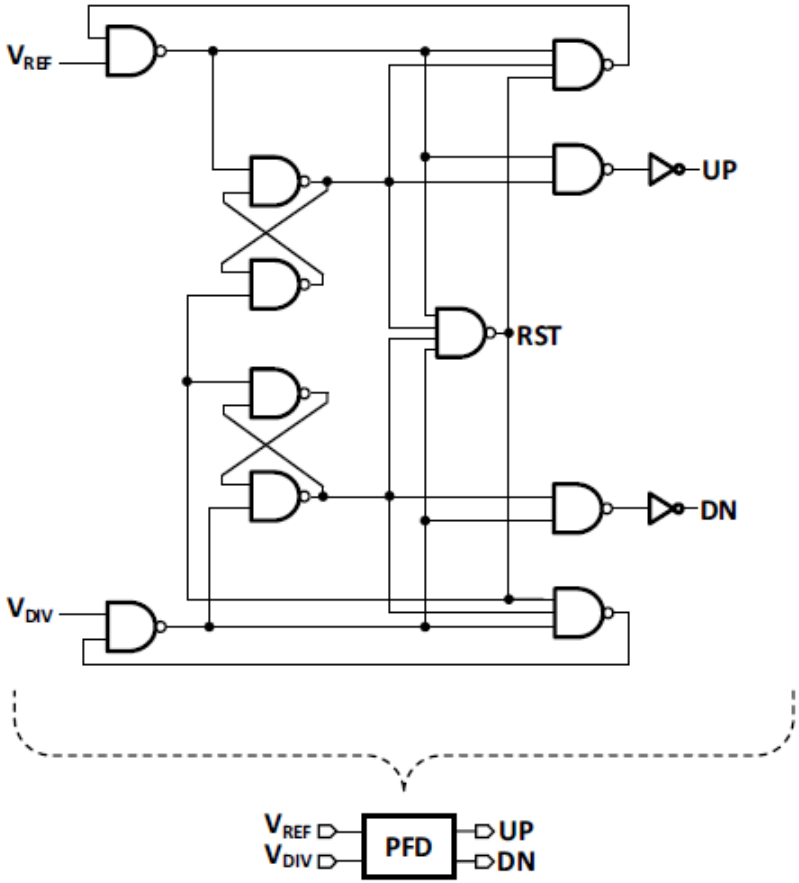
- The output impedance is raised
- Drawback stems from the finite response of the auxiliary amplifiers

Circuit Techniques to deal with Channel Length Modulation Effect – Use of Servo Loop



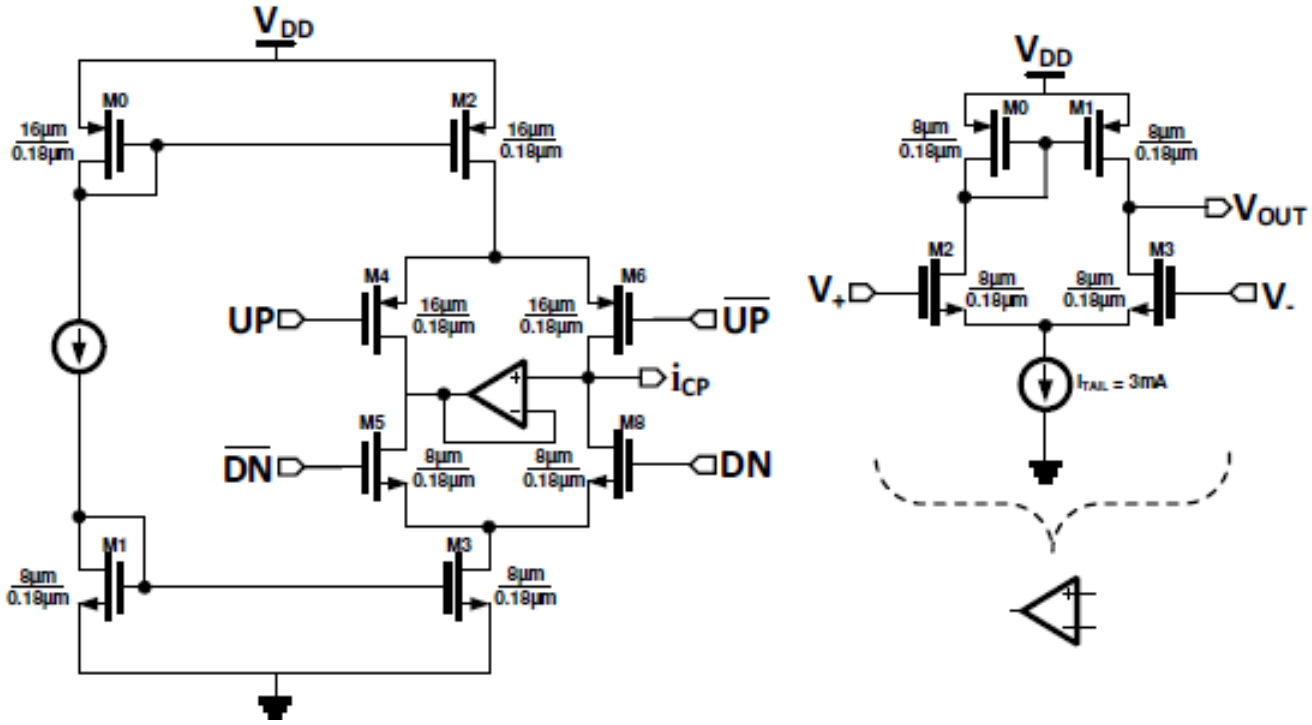
- A_0 need not provide a fast response
- Performance limited by random mismatches between NMOS current sources and between PMOS current sources. Also the op amp must operate with a nearly rail-to-rail input common-mode range.

Example Circuit* - PFD

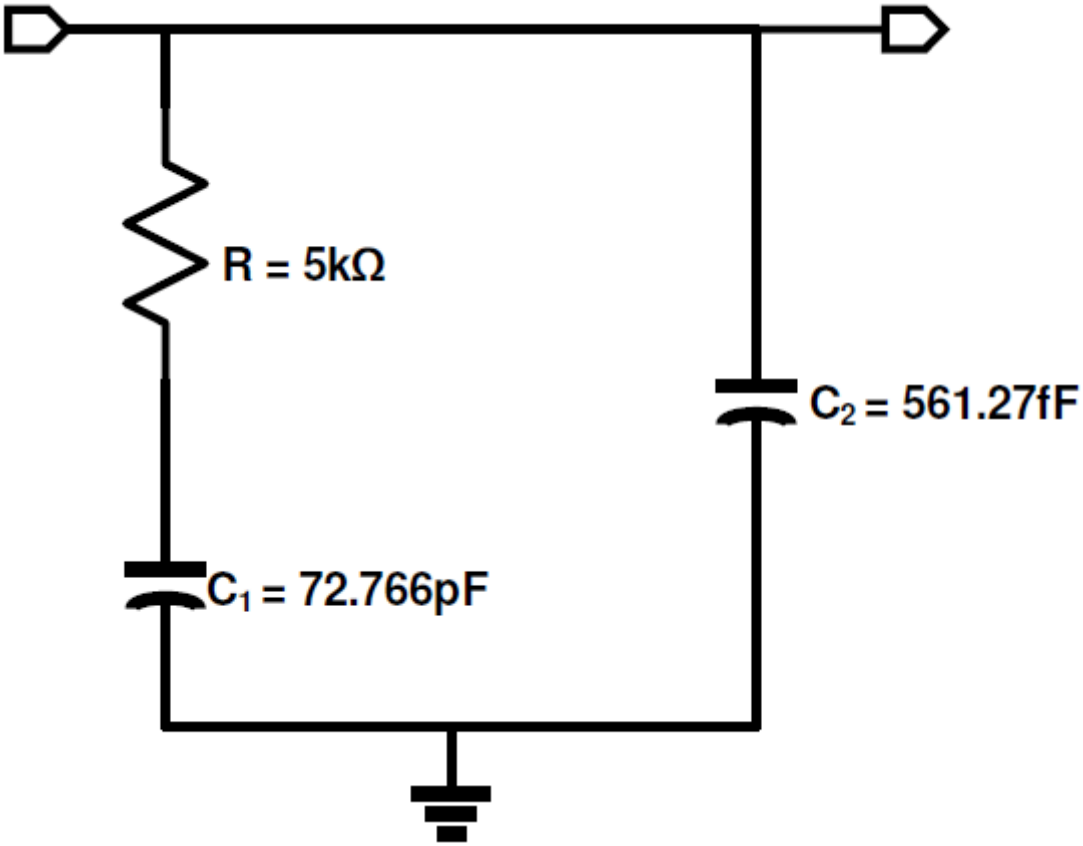


*Rishi Ratan, MS Thesis, UIUC, 2014

Example Circuit - CP

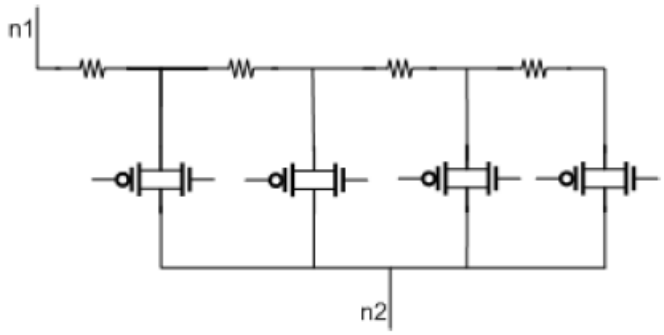


Example Circuit – Loop Filter



Example Circuit – Loop Filter Resistors

- Resistance may be programmable using switches
- Parasitic switch resistance varies with control voltage
  - Usually lowest at Vctl extremes if CMOS transmission gate
  - Large Rswitch variation vs. Vctl if NMOS or PMOS only
  - Usually Rswitch < 5-10% of Rlpf
- Minimize gate leakage and noise coupling from switches
  - Coupling less of a problem if using voltage regulators
- Typical values: $500\Omega < R_{lpf} < 50k$
- Poly, Diffusion, Nwell R's most common

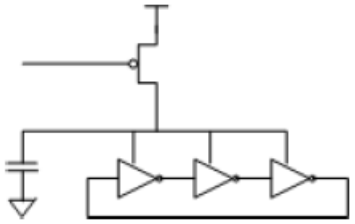


- MOSFET R's sometimes used if R placed "below" C1 cap
  - Constant Vgs needed

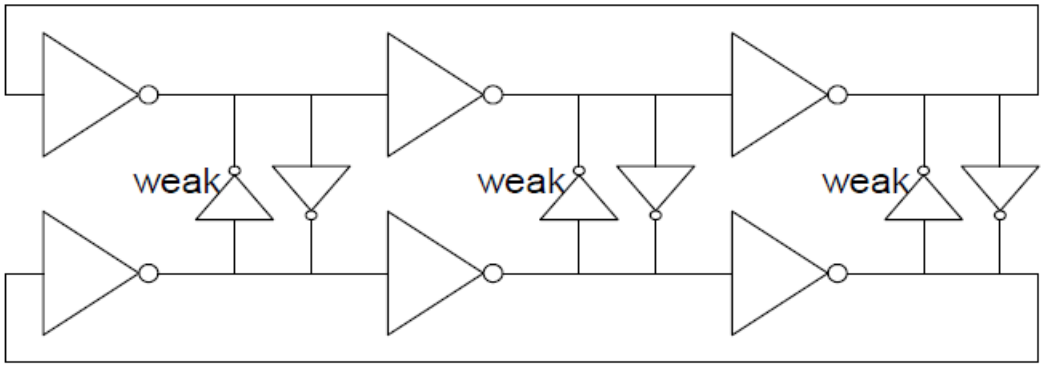
Example Circuit – Loop Filter Capacitors

- Reference capacitor to same supply as VCO V-to-I reference → makes power supply noise common mode
- Gate Leakage in MOSFET caps can be a HUGE problem
  - Exponential I_{leak} vs. V: $I_{leak} \sim V_{gate}^4$ (approximate)
  - Weak temperature dependence
  - I_{leak} vs. t_{ox} → ~2-3× per Angström
  - Use metal caps (2-10X larger) or thick-gate (IO) oxide caps to minimize leakage
  - If MOSFET caps, *accumulation* mode preferred – flatter C_{gate} vs. V
- I_{leak} causes large refclk spurs (jitter) and static phase error
- Typical values:
  - $5pF < C_1 < 200\ pF$
  - 1% (low phase error) $< C_2/C_1 < 10\%$ (low period jitter)
  - Smaller C_1 caps are becoming more common w/ higher reference frequencies and metal cap usage

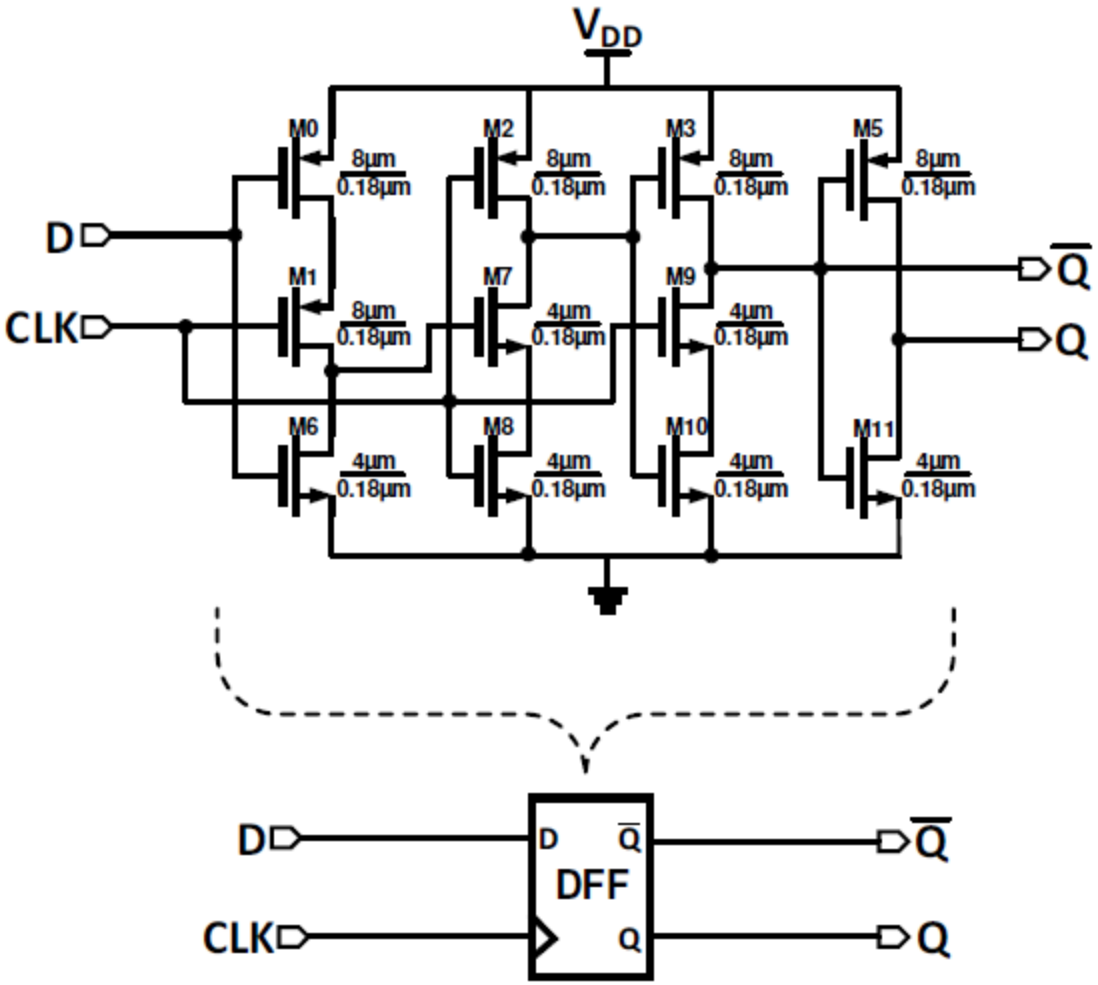
Example Circuit - VCO



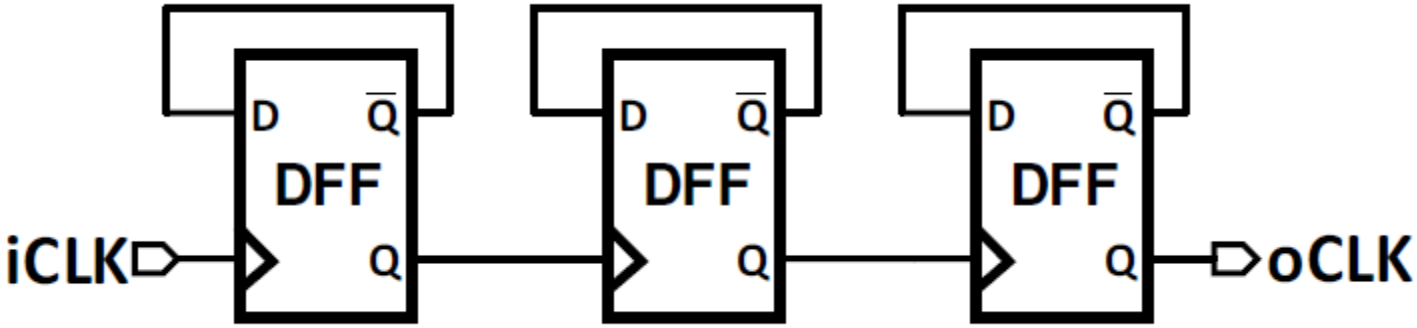
- RO VCO usually consists of two circuits
  - bias generator (e.g. V_{ctl} to I_{ctl})
  - voltage or current controlled ring oscillator (RO)
- Usually odd # of stages (usually 5+). Even # ok if differential RO
- Feedback INV → usually weaker by > ~3-4×
- Tune frequency by adjusting "VDD" of inverters – changes delay
- "Vdd" for inverters is regulated output of VCO V2I



Example Circuit – DFF Using TSPC

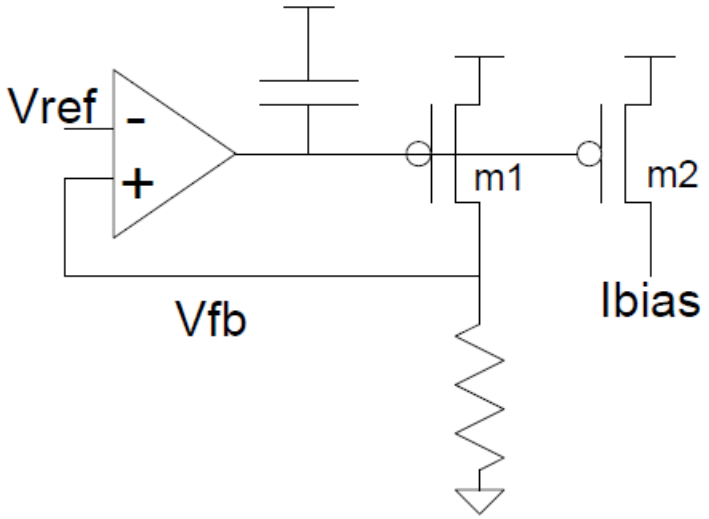


Example Circuit – Divider



Example Circuit – Ibias

- $I_b \sim V_{ref} / R$
- V_{ref} generated from PVT-insensitive bandgap reference
- Con: feedback loop may oscillate
  - capacitor added to improve stability
  - resistor in series w/cap provides stabilizing zero *(not shown)*
- Pro: VDD-independent, mostly Temp independent
- Pro: Icp*Rlpf = constant → less PVT-sensitive loop dynamics



Example Circuit – Voltage Regulator

- Hard to stabilize over wide Iload and Cload ranges
- NMOS source-follower output stage
  - Requires more headroom
  - Faster response and easier to stabilize
- PMOS common-source output stage
  - Can handle larger current loads → larger Vgs