

# *Phase Locked Loop Design*

## *For USB v3.0 TX*

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2024 Fall & 2025 Spring

# Project Background

In most SoC system, high-frequency clocks are generated using Phase-Locked Loops (PLLs), which multiply the crystal oscillator frequency.

In this Design, based on TSMC65nm, I focus on Design and simulation of Charge Pump, Loop Filter and VCO, while collaborated on others included PFD, Frequency Divider, etc;

The PLL Specs are based on the [Universal Serial Bus \(USB\) v3.0 Specification](#)

--- Physical Layer Diagram.

The SSUSB Tx PLL provides the clock signal for the Tx-side digital logic, Serializer (SER), and Driver, etc.

## Phy Layer Tx Block Diagram

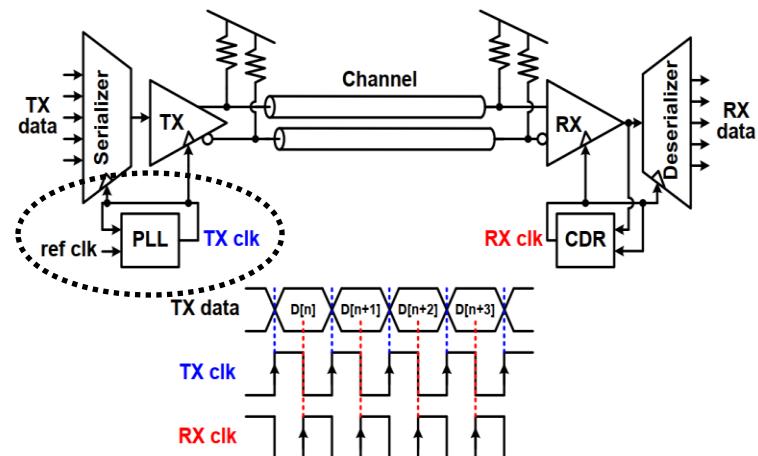
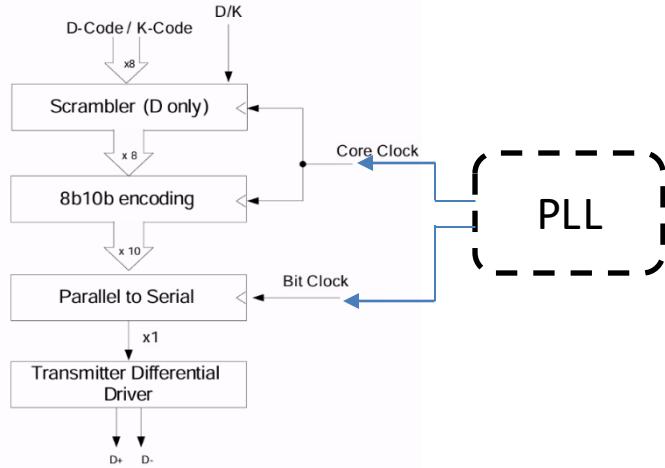


Figure 6-2. Transmitter Block Diagram

# Specification Definition

## 6.5.1 Informative Jitter Budgeting

The jitter for USB 3.0 is budgeted among the components that comprise the end to end connections: the transmitter, channel (including packaging, connectors, and cables), and the receiver. The jitter budget is derived at the pads of the device. The Dj distribution is the dual Dirac method. Table 6-8 lists Tx, Rx, and channel jitter budgets.

**Table 6-8. Informative Jitter Budgeting at the Device**

Jitter Contribution (ps)	Rj <sup>1,2</sup>	Dj <sup>3</sup>	Tj <sup>4</sup> at 10 <sup>-12</sup>
Tx <sup>6</sup>	2.42	41	75
Media <sup>5</sup>	2.13	45	75
Rx	2.42	57	91
Total:	4.03	143	200

Notes:

1. Rj is the sigma value assuming a Gaussian distribution
2. Rj Total is computed as the Root Sum Square of the individual Rj components
3. Dj budget is using the Dual Dirac method
4. Tj at a 10<sup>-12</sup> BER is calculated as  $14.068 * Rj + Dj$
5. The media budget includes the cancellation of ISI from the appropriate Rx equalization function
6. Tx is measured after JTF

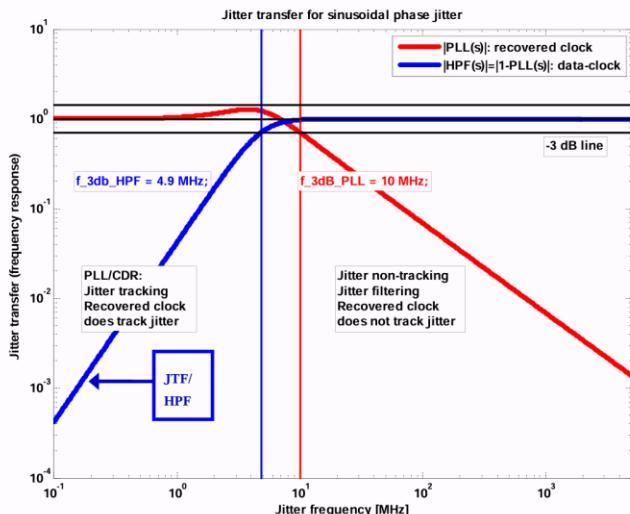


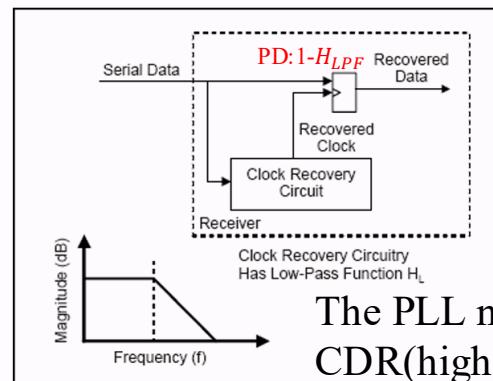
Figure 6-9. "Golden PLL" and Jitter Transfer Functions

*Specs of Jitter:*

$$TJ = DJ + N * RJ = 14.068 * RJ + DJ < 75 \text{ ps}$$

$$RJ < 2.42 \text{ ps} \text{ (Pass CDR BW 4.9MHz)}$$

The system exhibits perfect tracking at low freq, while its response degrades at high freq.



The PLL need to pass through the CDR(high pass) before output

Figure 6-8. Jitter Filtering – "Golden PLL" and Jitter Transfer Functions

# Specification Definition

*Specs of Output Frequency:*

For the 5 Gbps(200ps) data rate defined by USB v3.0,  
I adopted a **half-rate** output--- generated **2.5 GHz** signals with **0/180 phase error**,  
then combined to achieve 5 GHz output.

be measured into a 50 ohm load.

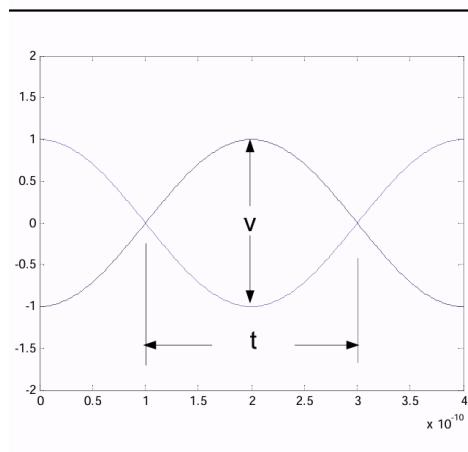
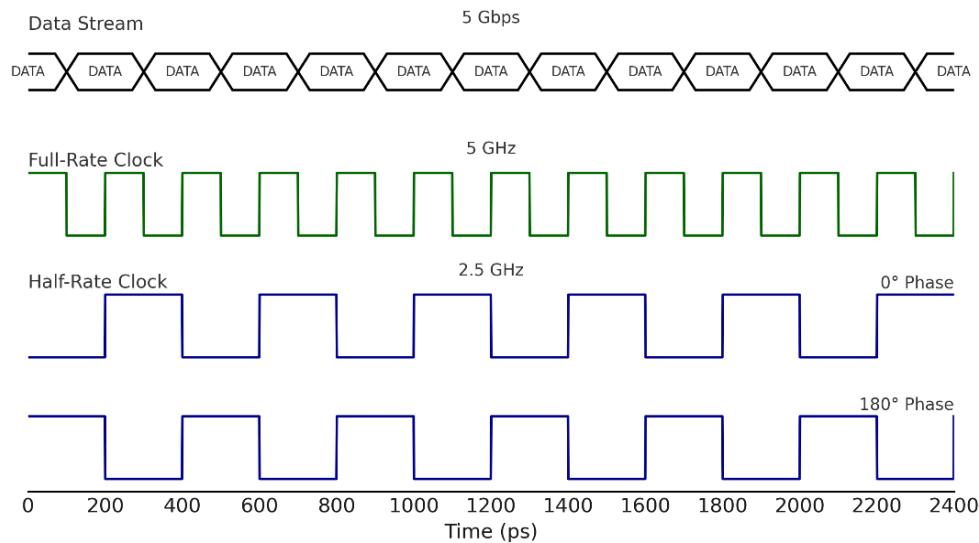


Figure 6-11. Generic Eye Mask



In practical designs, the choice between full-rate and half-rate should be made based on system-level requirements on the Tx side.

# Specification Definition

## 6.5.3 Normative Spread Spectrum Clocking (SSC)

All ports are required to have Spread Spectrum Clocking (SSC) modulation. Providing the same SSC clock to two different components is allowed but not required, the SSC can be generated asynchronously. The SSC profile is not specified and is vendor specific. The SSC modulation requirement is given in table 6-10. The SSC modulation may not violate the phase slew rate described in Section 6.5.4.

**Table 6-9. SSC Parameter**

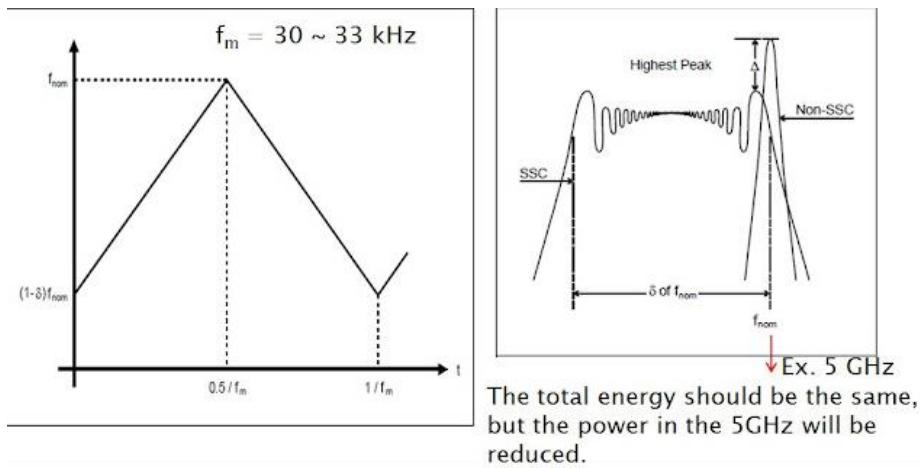
Symbol	Description	Limits		Units	Note
		Min	Max		
T <sub>SSC-MOD-RATE</sub>	Modulation Rate	30	33	kHz	
T <sub>SSC-FREQ-DEVIATION</sub>	SSC deviation	+0.0 / -0.4	+0.0/-0.5	%	1

Note:

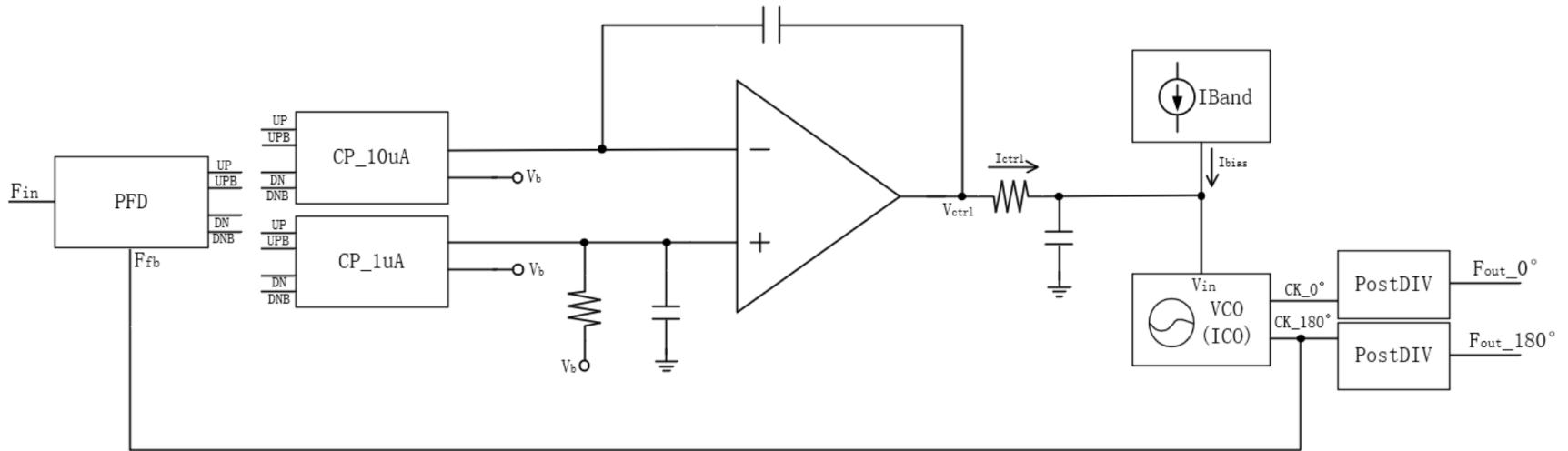
1. The data rate is modulated from +0% to -0.5% of the nominal data rate frequency and scales with data rate.
2. This is measured below 1 MHz only

Spread Spectrum Clocking (SSC) typically adds around 30 kHz of jitter to improve EMI issues.

SSC is highly important in PLL systems, but it is challenging to implement.  
So, it is not considered in this design.



# PLL architecture



- 1) The CP adopts a current-steering architecture, with an internal op-amp to stabilize the output node voltage and then reduce ripple.
- 2) The dual-path LPF not only achieves capacitor multiplication, but also relax CP output voltage range, simplifying CP design, meanwhile the op-amp gain reduces the CP's output drive requirement.
- 3) Since the LPF op-amp introduces additional noise, use a low-noise current reference (IBand) to supply large current while the op-amp provides only small current, minimizing the op-amp noise impact on the VCO and reducing the op-amp's output current burden.

# PLL BW Analysis

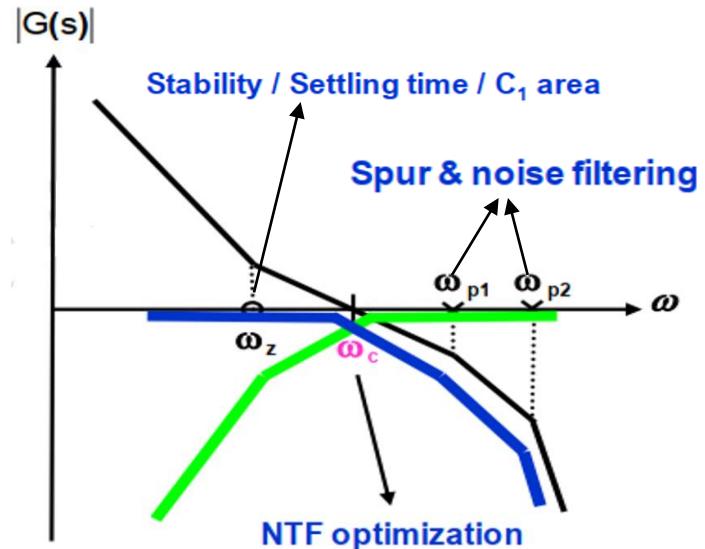
1) The PLL BW is based on phase noise.

In PLLs, HPF module: VCO;

LPF module: REF, PFD&CHP, DIV;

Optimal BW  $\Rightarrow [\sum(PN@f_{high}, PN@f_{low})]_{min}$

$\Rightarrow$  I set PLL BW = 1MHz at first.

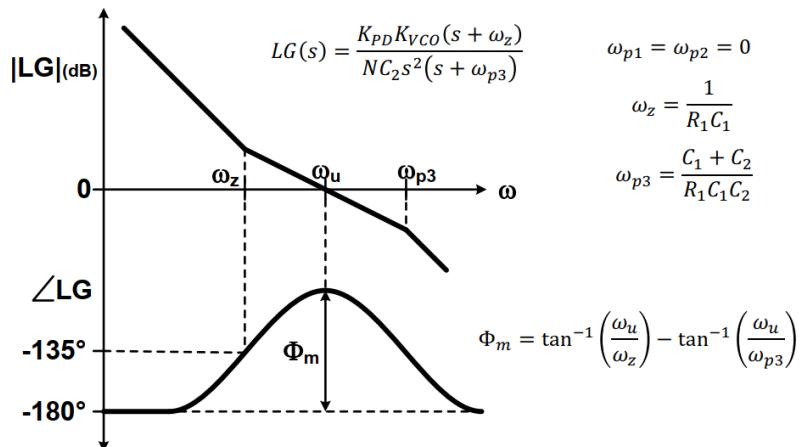


2) BW  $< \frac{1}{10} REF$ , ensured conversion between time-domain and s-domain signals

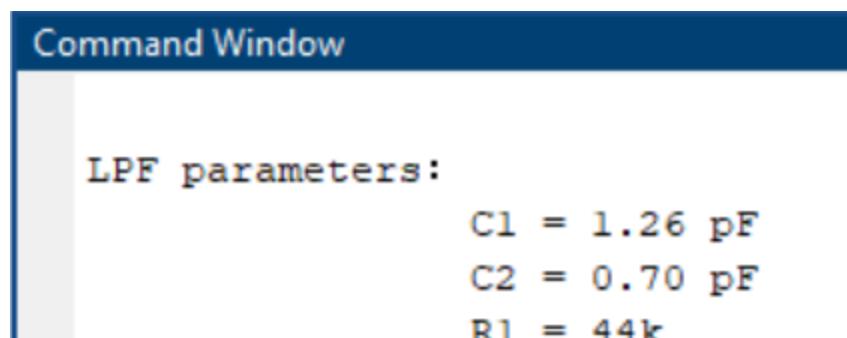
3) BW---Phase Margin vs Settle time, to ensure settle time  $< 20\mu s$

$\Rightarrow$  Finally, PLL BW = 1.8MHz.

# Design for Max phase margin



Matlab:



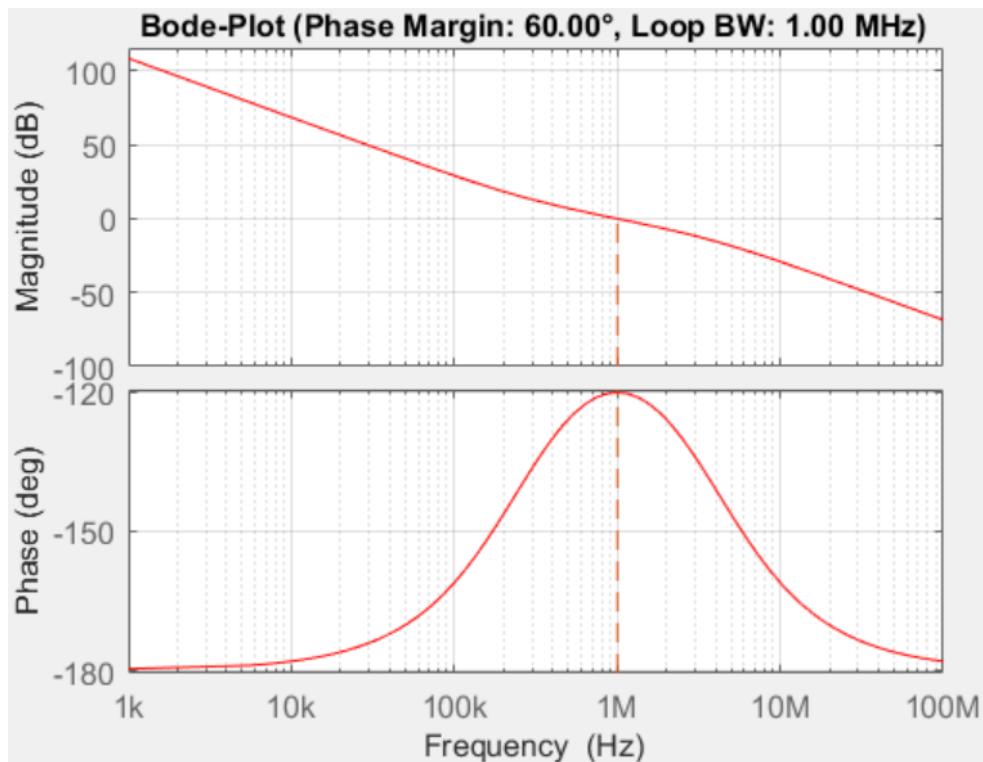
After BW is set, align  $\omega_u$  with  $\Phi_m$  for max phase margin.

$$\Rightarrow \text{Set } b = \frac{C_1}{C_2}, \quad \text{BW} = \sqrt{\omega_Z * \omega_{p3}}$$

$$\omega_Z = \frac{BW}{\sqrt{b+1}} \quad \omega_{p3} = \sqrt{b+1} * \text{BW}$$

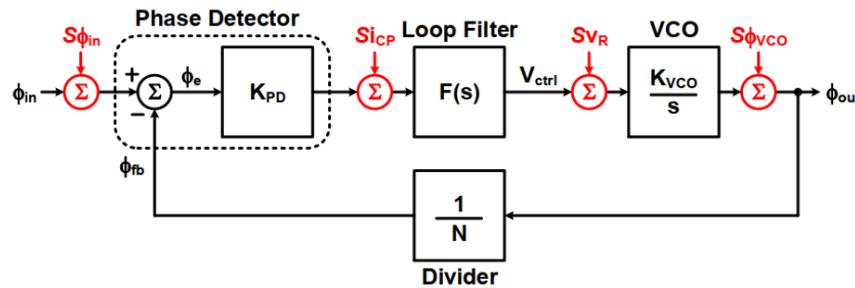
$$\Rightarrow R, C_1, C_2$$

$b \leftarrow \rightarrow$  Phase Margin



# PLL Noise

Common PLL Noise Sources:



$$S_{\phi_{out}}^{\phi_{in}} = S_{\phi_{in}} |NTF_{IN}(s)|^2$$

$$S_{\phi_{out}}^{i_{CP}} = S_{i_{CP}} |NTF_{CP}(s)|^2$$

$$S_{\phi_{out}}^{v_R} = S_{v_R} |NTF_R(s)|^2$$

$$S_{\phi_{out}}^{\phi_{VCO}} = S_{\phi_{VCO}} |NTF_{VCO}(s)|^2$$

$$S_{\phi_{out}}^{Total} = S_{\phi_{out}}^{\phi_{in}} + S_{\phi_{out}}^{i_{CP}} + S_{\phi_{out}}^{v_R} + S_{\phi_{out}}^{\phi_{VCO}}$$

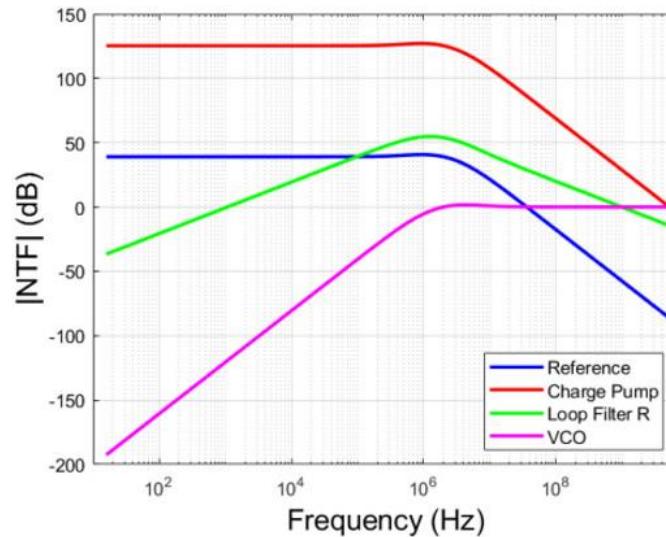
Noise Transfer Functions:

$$NTF_{IN}(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{(N)LG(s)}{1 + LG(s)}$$

$$NTF_{CP}(s) = \frac{\phi_{out}(s)}{i_{CP}(s)} = \frac{\left(\frac{N}{K_{PD}}\right) LG(s)}{1 + LG(s)}$$

$$NTF_R(s) = \frac{\phi_{out}(s)}{v_R(s)} = \frac{\frac{K_{VCO}}{s}}{1 + LG(s)}$$

$$NTF_{VCO}(s) = \frac{\phi_{out}(s)}{\phi_{VCO}(s)} = \frac{1}{1 + LG(s)}$$

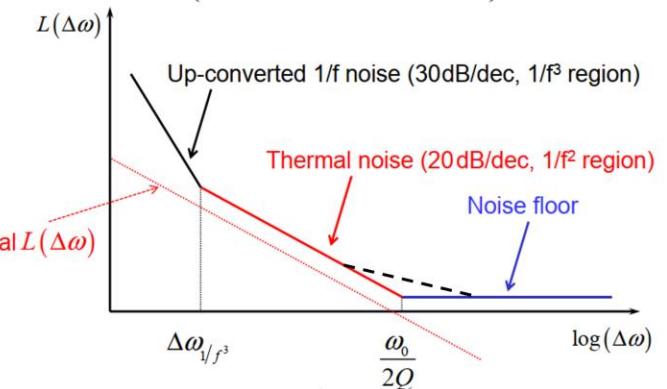


- 1) Input reference and charge pump noise are low-pass filtered.
- 2) Loop filter noise (at the VCO input) is band-pass filtered.
- 3) VCO output phase noise is high-pass filtered.

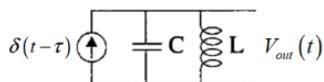
# VCO Noise

## 1) Leeson Phase Noise Model

$$L(\Delta\omega) = 10 \log_{10} \left( F \cdot \frac{2k_B T R}{A_{pk}^2 / 2} \left[ 1 + \left( \frac{1}{2Q} \cdot \frac{\omega_0}{\Delta\omega} \right)^2 \right] \right) \cdot \left( 1 + \frac{\Delta\omega_{1/f^3}}{\Delta\omega} \right)$$



## 2) Hajimiri and Lee's theory of phase noise



The conversion of noise into phase noise is time-dependent – LTV phase noise analysis needed!

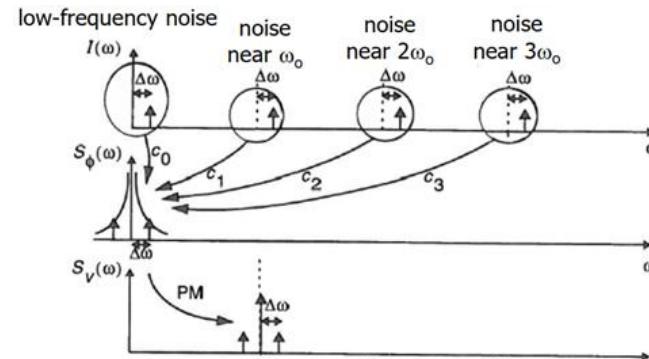
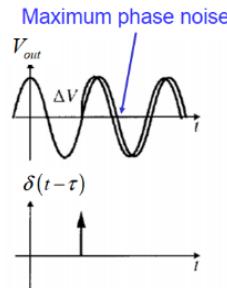
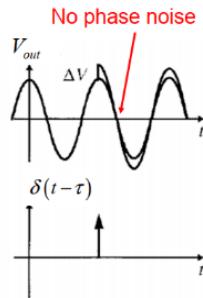
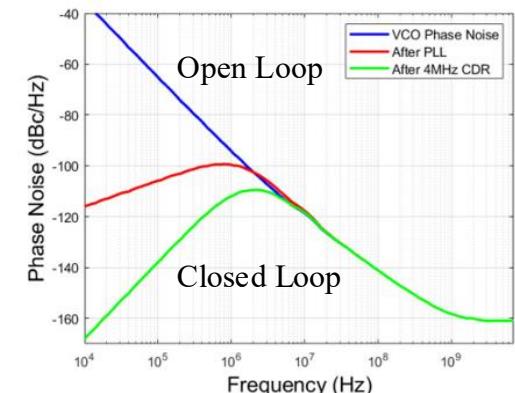
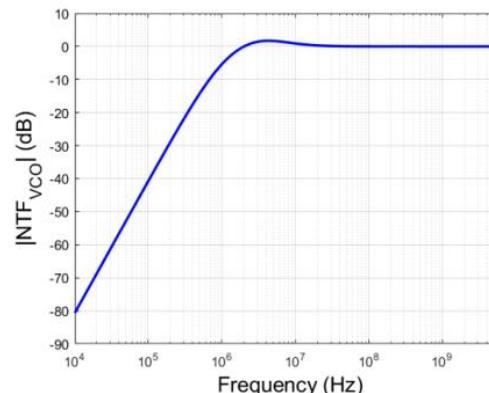


Figure 4.18: The conversion of tones in the vicinity of integer multiples of  $\omega_0$ .

## Impulse sensitivity function(1SF)

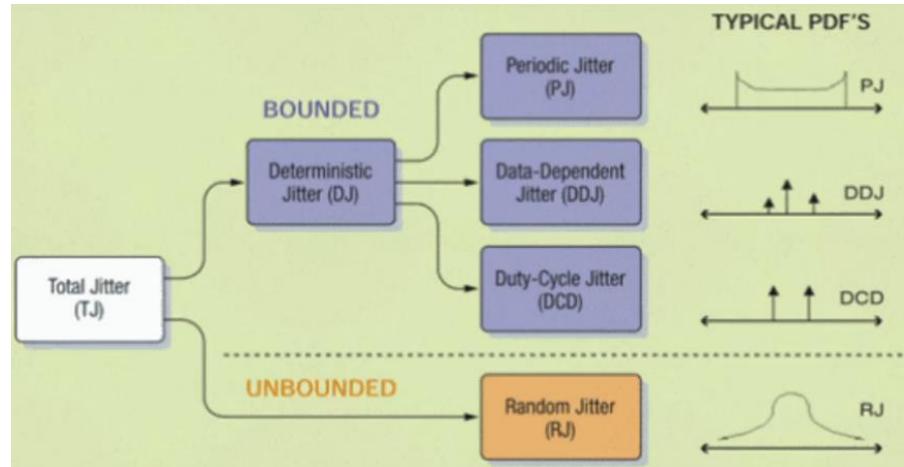
⇒ For Ring OSC,  
Adjust the W/L of PMOS to NMOS  
to ensure  $T_{PLH} = T_{PHL}$



# Jitter

- Types of jitter:
- 1) Absolute Jitter(abs jitter)
  - 2) Period Jitter
  - 3) Cycle-cycle Jitter

In the wireline systems, absolute jitter is of greater concern.



**Table 3.1** General relationships between variance of jitter and phase noise.

Jitter	Symbol	As a Function of $\mathcal{L}(f)$
Absolute	$\sigma_a^2$	$\frac{2}{\omega_0^2} \int_0^{+\infty} \mathcal{L}(f) df$
Period	$\sigma_p^2$	$\frac{8}{\omega_0^2} \int_0^{+\infty} \mathcal{L}(f) \sin^2(\pi f/f_0) df$
$N$ -period	$\sigma_{p(N)}^2$	$\frac{8}{\omega_0^2} \int_0^{+\infty} \mathcal{L}(f) \sin^2(\pi fN/f_0) df$
Allan Deviation	$\sigma_{\Delta y}^2 \left( \frac{N}{f_0} \right)$	$\left( \frac{2}{\pi N} \right)^2 \int_0^{+\infty} \mathcal{L}(f) \sin^4(\pi fN/f_0) df$

# RJ & DJ

TJ = RJ+DJ = DJ+N\*Rms, N based on BER for USB3.0 specs: N=14.069

TJ, RJ based on USB3.0 specs: RJ < 2.42ps, TJ < 75ps

**Table 6-8. Informative Jitter Budgeting at the Device**

Jitter Contribution (ps)	Rj <sup>1,2</sup>	Dj <sup>3</sup>	Tj <sup>4</sup> at 10 <sup>-12</sup>
Tx <sup>6</sup>	2.42	41	75

RJ is obtained by integrating the VCO phase noise from 1 kHz to  $\frac{f_0}{2}$

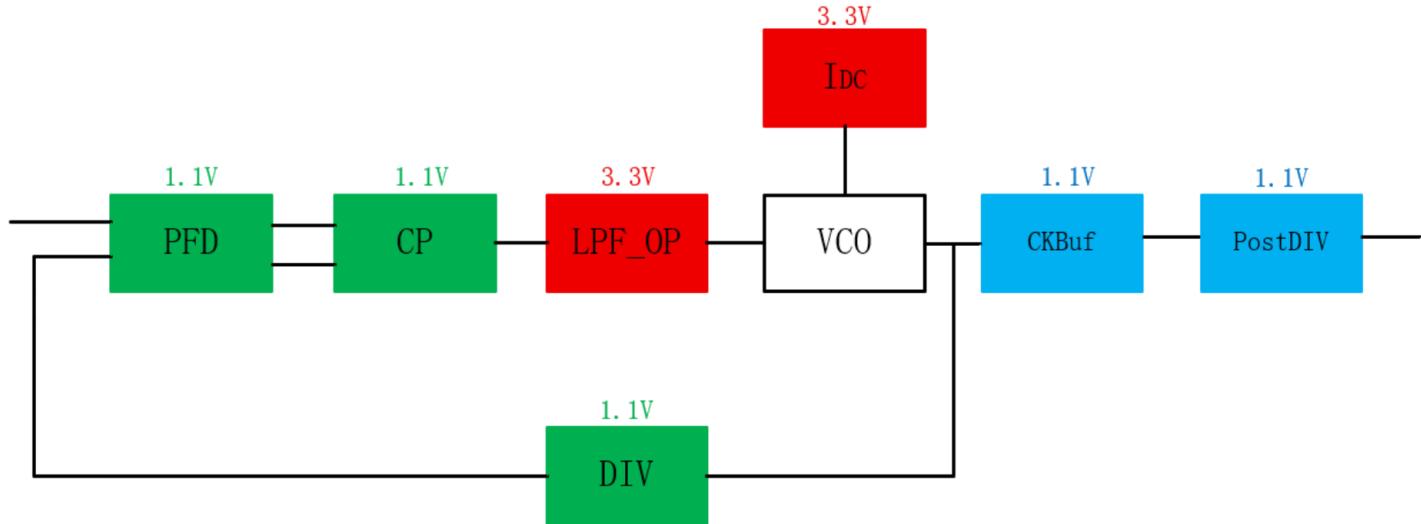
DJ is affected by:

1)PSIJ (power supply induce jitter)  
PSIJ -> Vctrl AC ripple -> VCO Spur(DJ)

2)REF Spur  
Phase error -> Vctrl AC ripple -> VCO Spur(DJ)

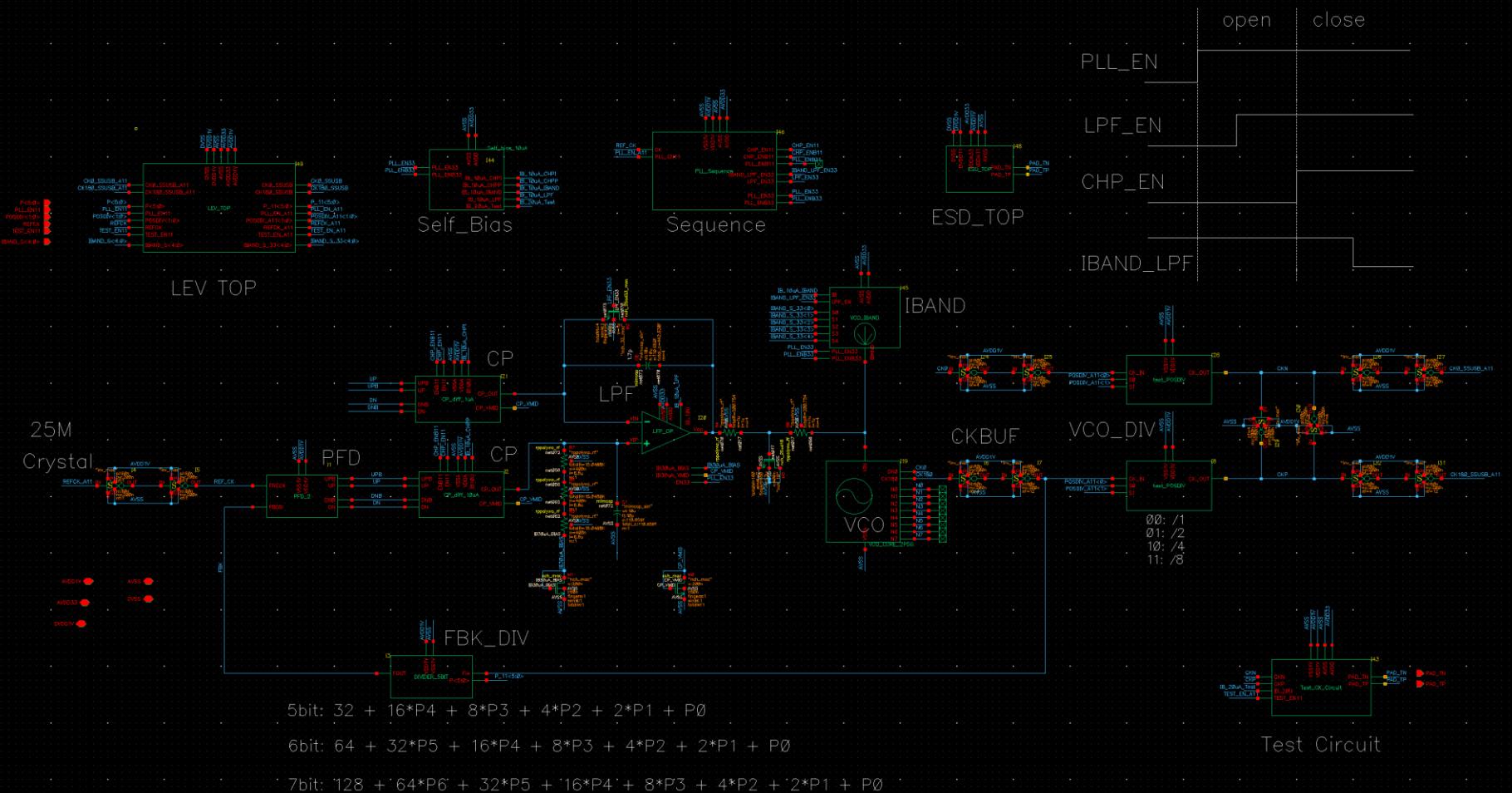
# *Power Domain*

1. LPF adopts an active op-amp architecture to relax the CP's VDD requirement;
2. PFD/CP/DIV all operate at 1 V to ensure 1V can drive CP;
3. VCO's VDD is isolated from PFD/CHP to reduce digital noise coupling.



This design employs a level shifter for the 1.1 V–3.3 V level conversion.  
In fact , High PSRR LDO supply would offer better PLL performance.

# Sch Overview



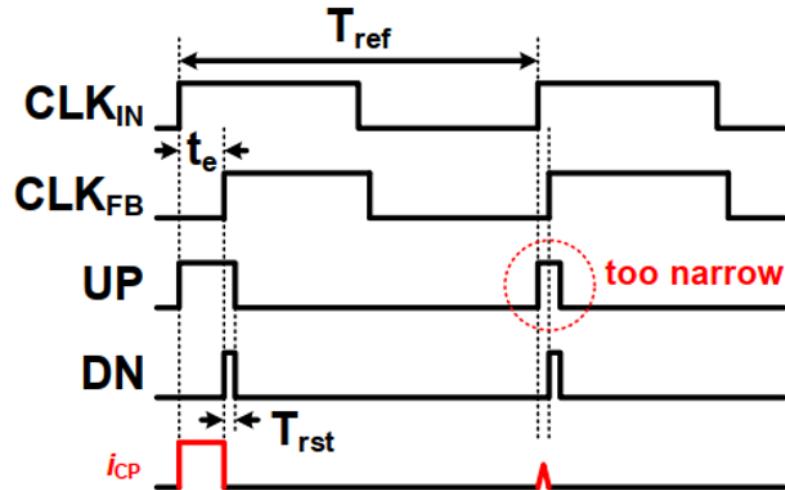
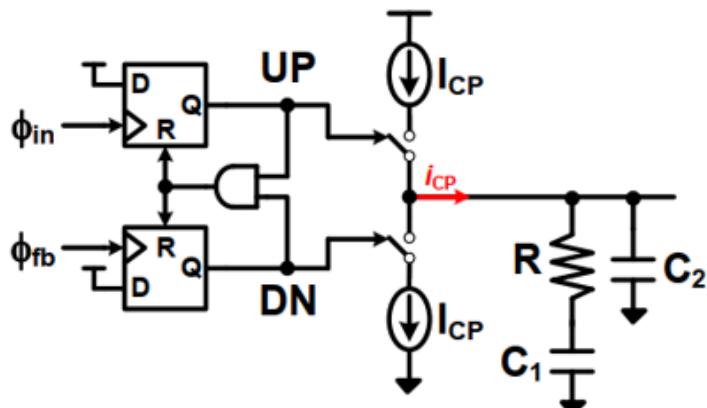
# *Specs Overview*

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	Min	Typ	Max	Unit	Note
AVDD10	0.99	1.1	1.21	V	
AVDD33	2.97	3.3	3.63	V	
Power consumption			14	mW	
Reference Clock freq		25		MHz	
PLL output Clock freq		2500		MHz	
PLL output Phase		2			Phase0/180
PLL settle time		5	20	us	
Rms jitter			2.42	ps	By USB 3.0 CDR
Area			100*200	um*um	

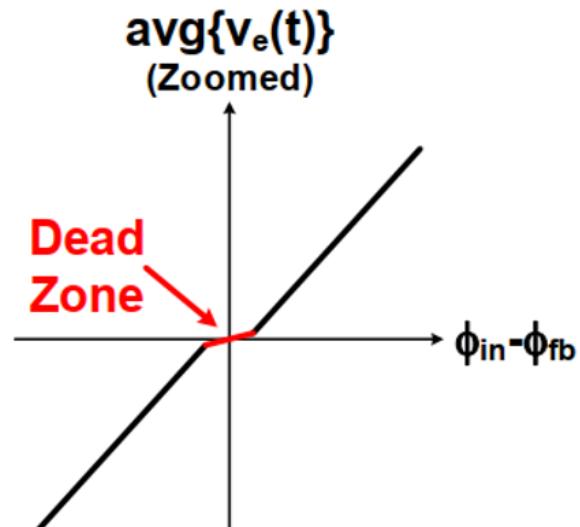
# PFD Challenge

## PFD Dead Zone



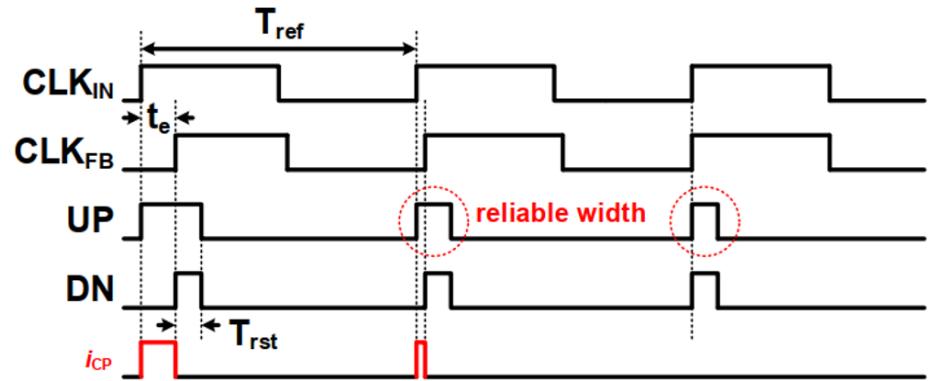
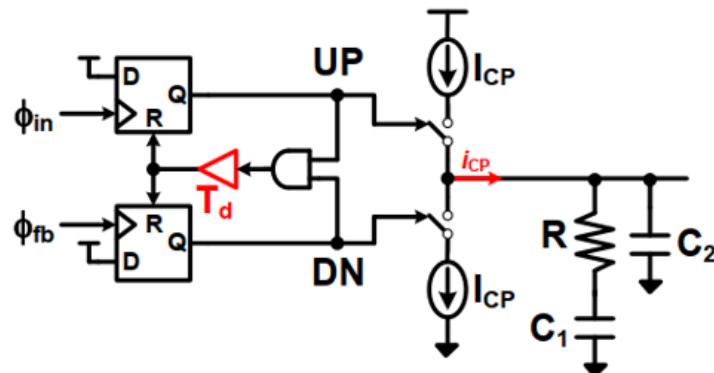
If phase error is small, then output pulses are too short to switch charge pump.

---Causes low loop gain and increased jitter



# PFD Implement

Solution: add a delay in PFD reset path  
to force a minimum Pulse length  $T_{rst}$   
to ensure CP can be switch.

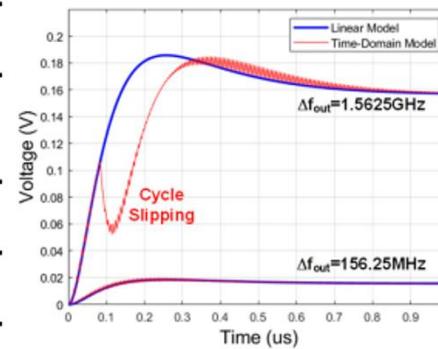
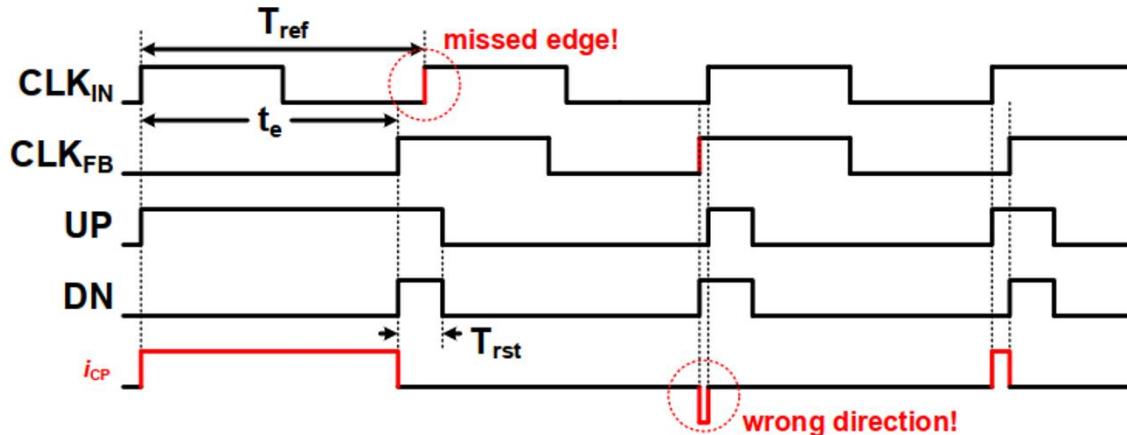


I choice  $T_d = 30ps$  based on CP switch worst-case: SSLVLT

Trade-off: 1)  $T_d$  vs Noise

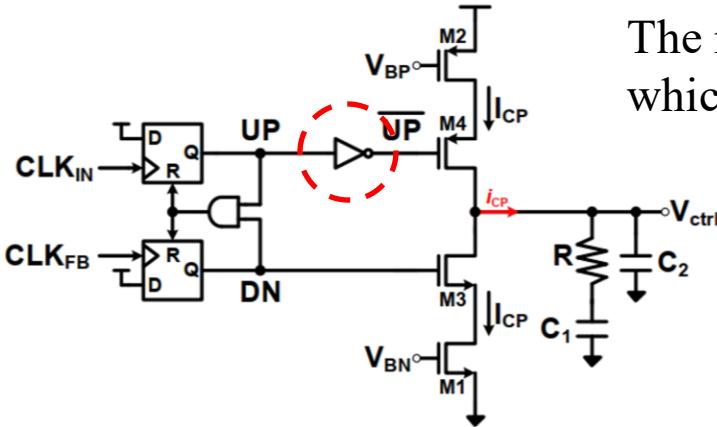
2)  $T_d$  vs Maximum Speed

3) Risk: reset time overlap rising edge ---cycle slipping

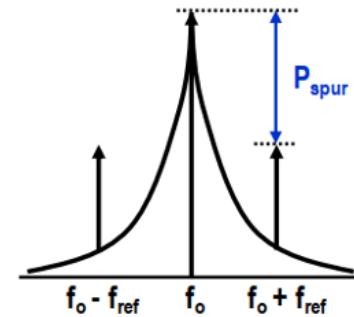


# CP Challenge

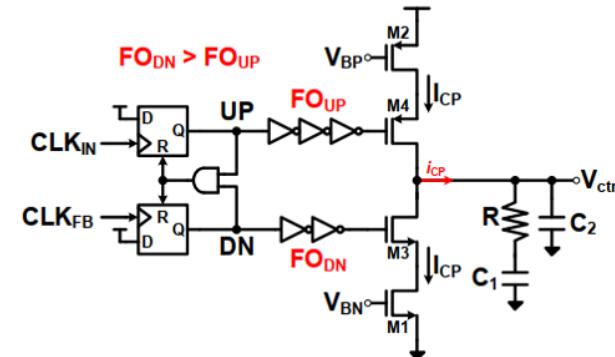
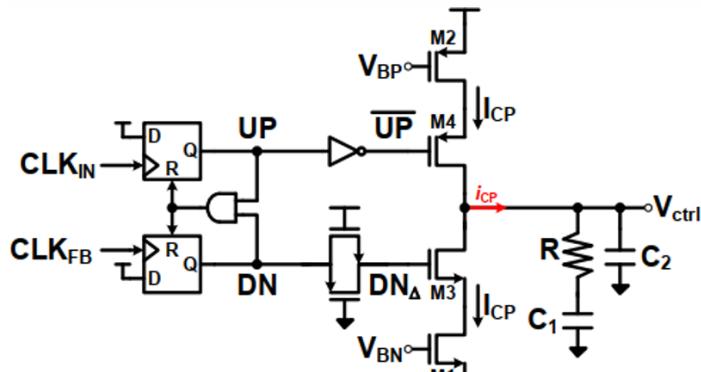
## I) Internal Skew Issue



The introduction of the inverter causes clock feedthrough, which induces ripple on  $V_{ctrl}$  and leads to ref spurs.



My solutions:



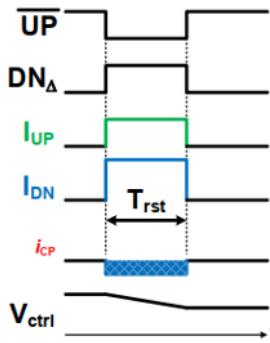
- 1) inserting a T-Gate on the DN path to introduce delay and reduce phase error.

- 2) increasing the number of inverters helps minimize the proportion of error.

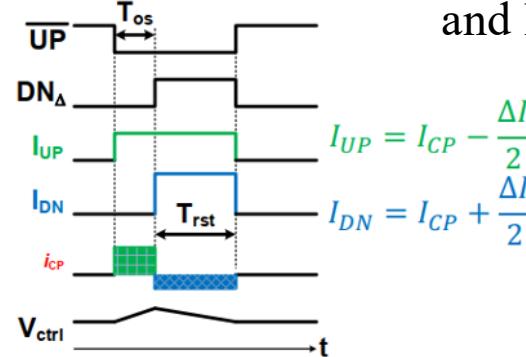
# CP Challenge

## II) Static Current Mismatch Issue

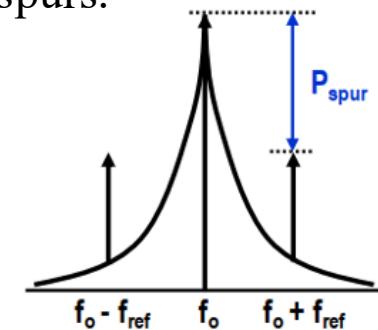
Ideal locked condition,  
but CP mismatch



Actual locked condition  
w/ CP mismatch

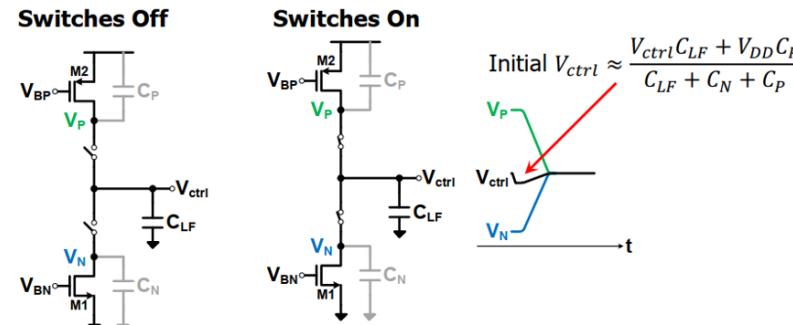


Current Mismatch also induces ripple on  $V_{ctrl}$   
and leads to ref spurs.



## III) Dynamic Current Mismatch Issue

- AC feedthrough: Parasitic capacitance couples the AC signal to the output
- Charge Injection: When the MOS turns off, injection from the MOS channel causes  $V_{out}$  glitch
- Charge Sharing: When the MOSFET turns on, the initial voltage difference causes  $V_{out}$  glitch



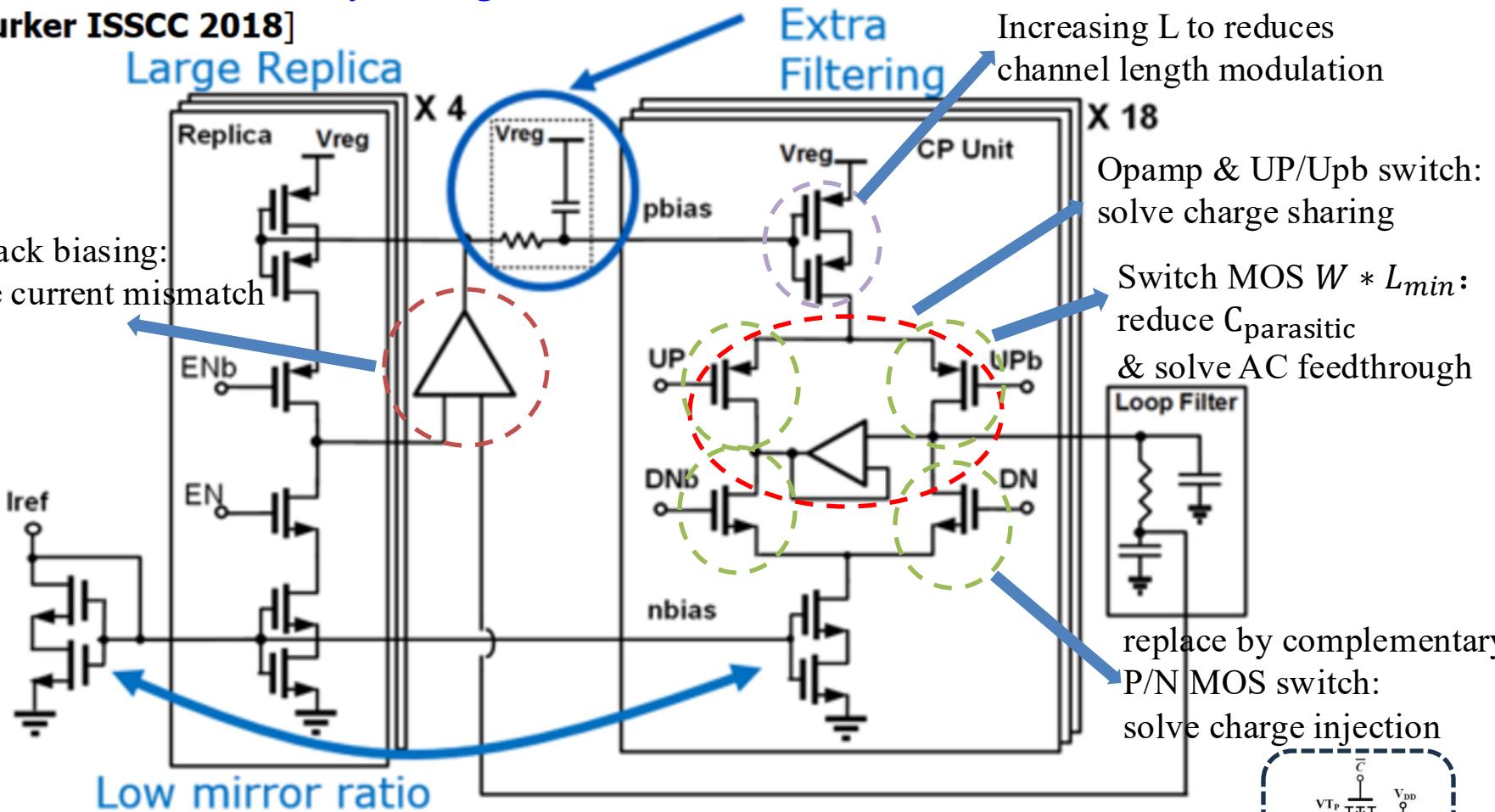
# CHP Implement

Paper reproduction |  XILINX  
ALL PROGRAMMABLE.

[ISSCC2018-23 A 7.4-14GHz PLL with 54fsrms](#)

[Jitter in 16nm FinFET for Integrated RF Data Converter SoCs](#)

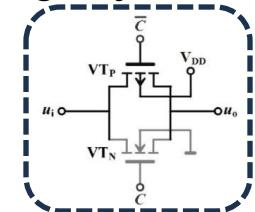
[Turker ISSCC 2018]



reproduced and optimized low-noise Charge pump:

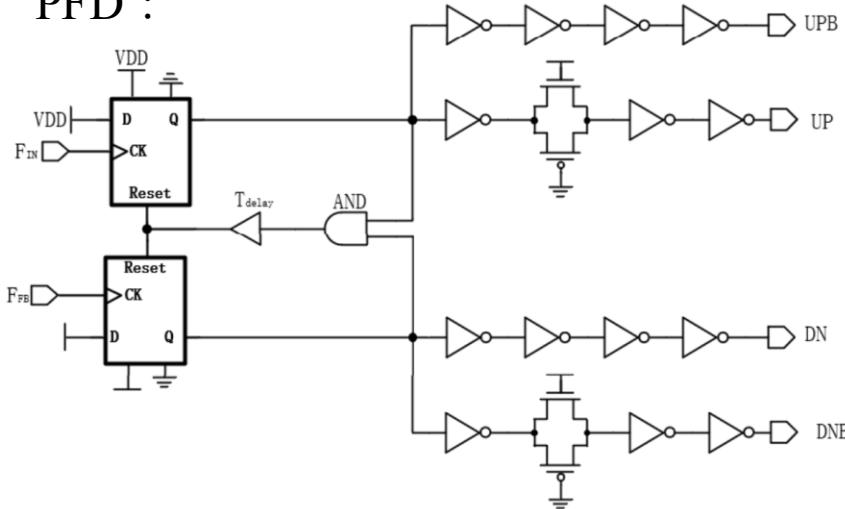
⇒ Achieved Current mismatch < 1%, Phase Noise -128dBc@1MHz

⇒ Output voltage range: 0.4–1.4 V (under 1.8V VDD)

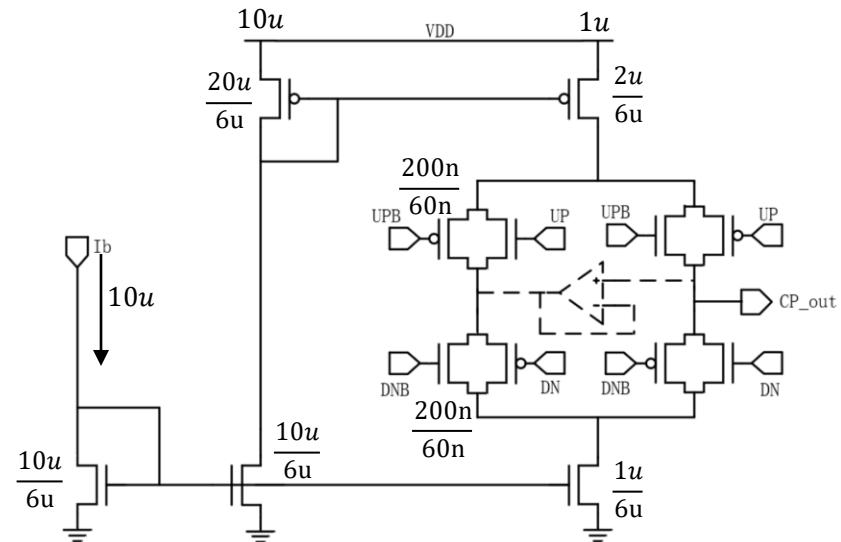


# PFD & CP

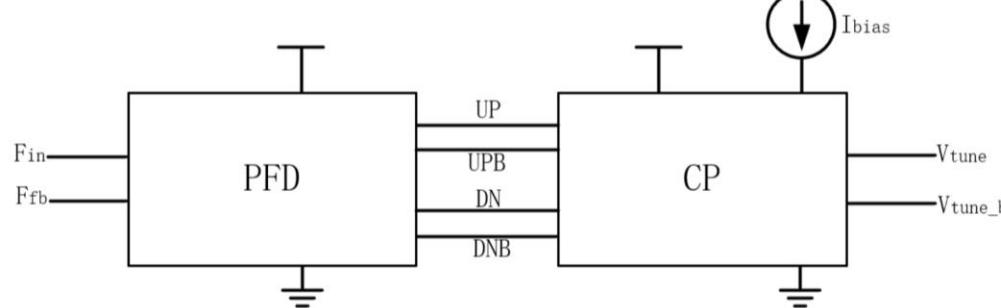
PFD :



CP: MOS uses LVT core devices.



Test Bench:

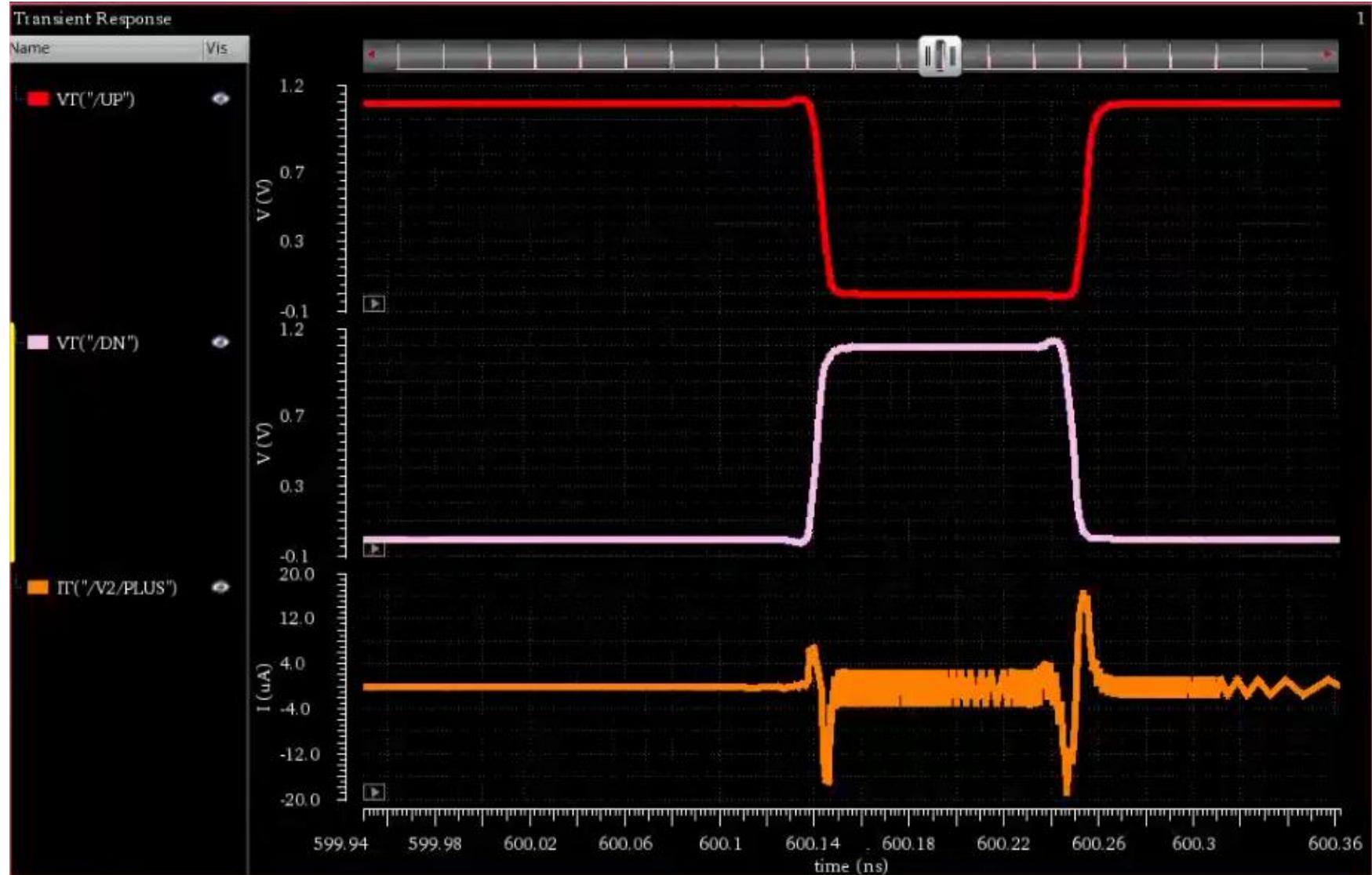


Simulation Check List:

1. DC Check
2. CP mismatch ( $I_{UP}$ & $I_{DN}$ )
3. PFD&CP Dead Zone
4. PFD&CP total phase error
5. CP Noise

# *CP\_Mismatch*

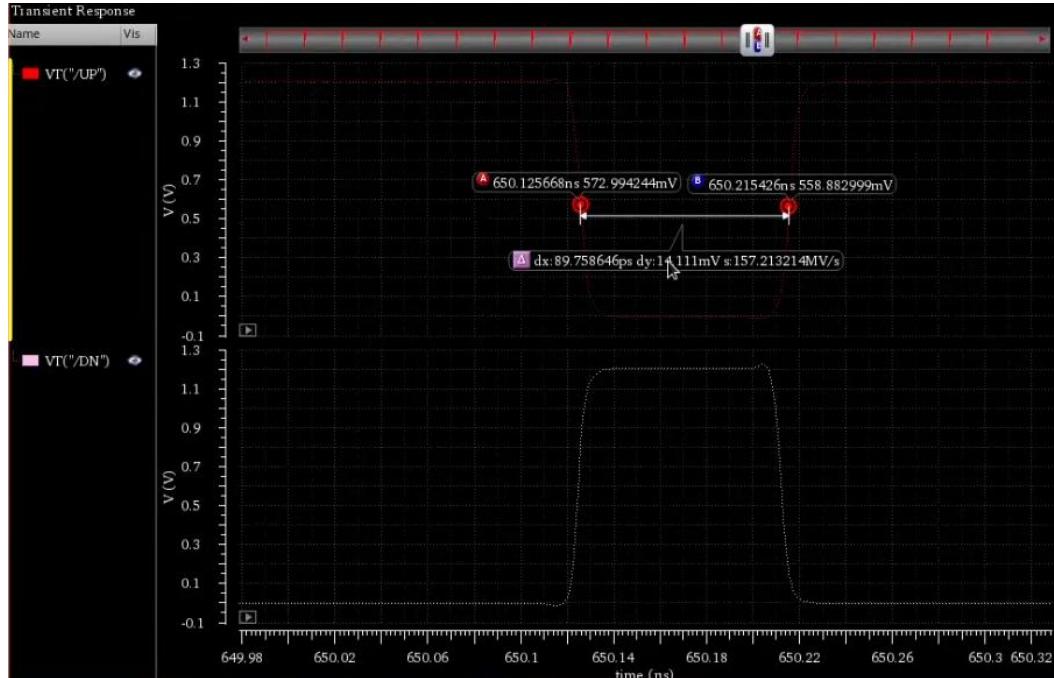
As REF and FB are in the same frequency and phase, CP mismatch =14.71nA(< 1%).



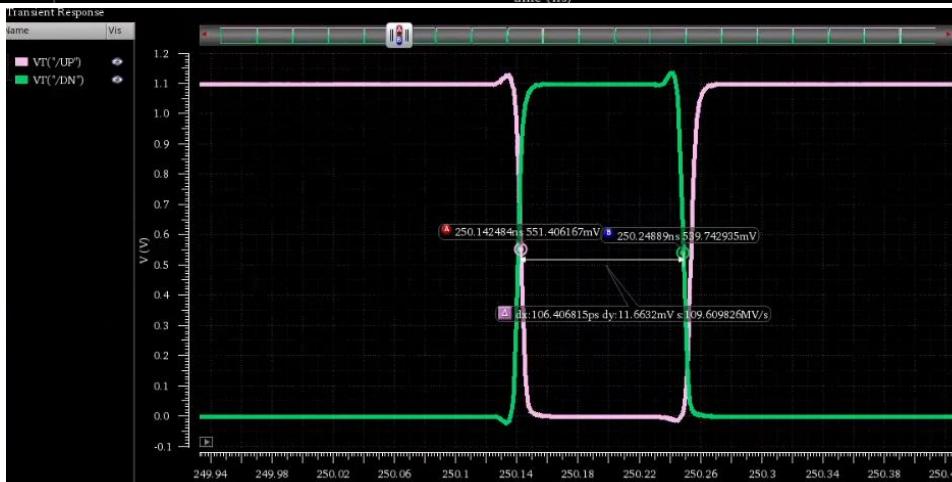
# PFD&CH\_Deadzone

As REF and FB are in the same frequency and phase

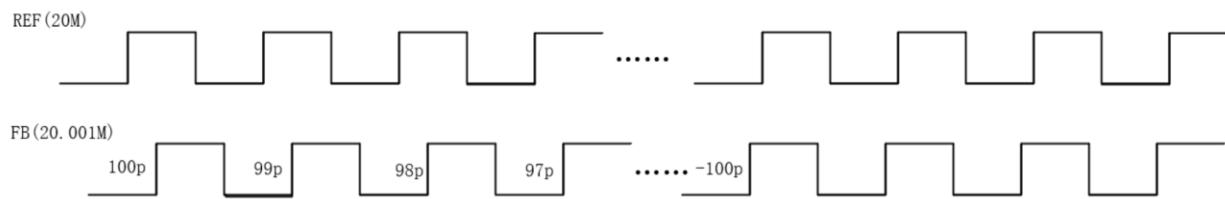
worse case: As FFHVHT, Deadzone = 89ps



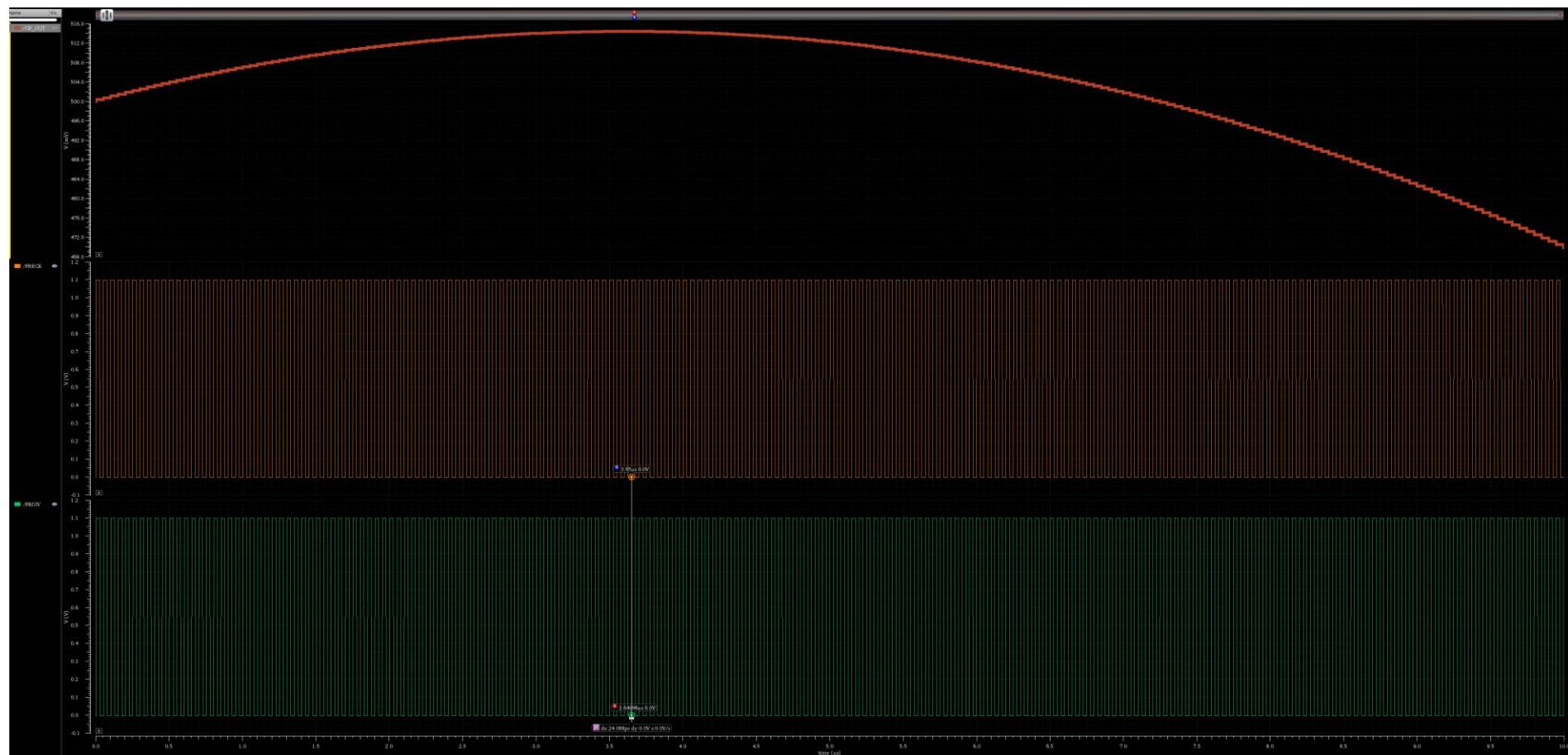
As TT, Deadzone = 106ps



# *PFD&CHP\_Phase error*



As Turning point of the curve(PLL Locked), Phase error = 24.1ps

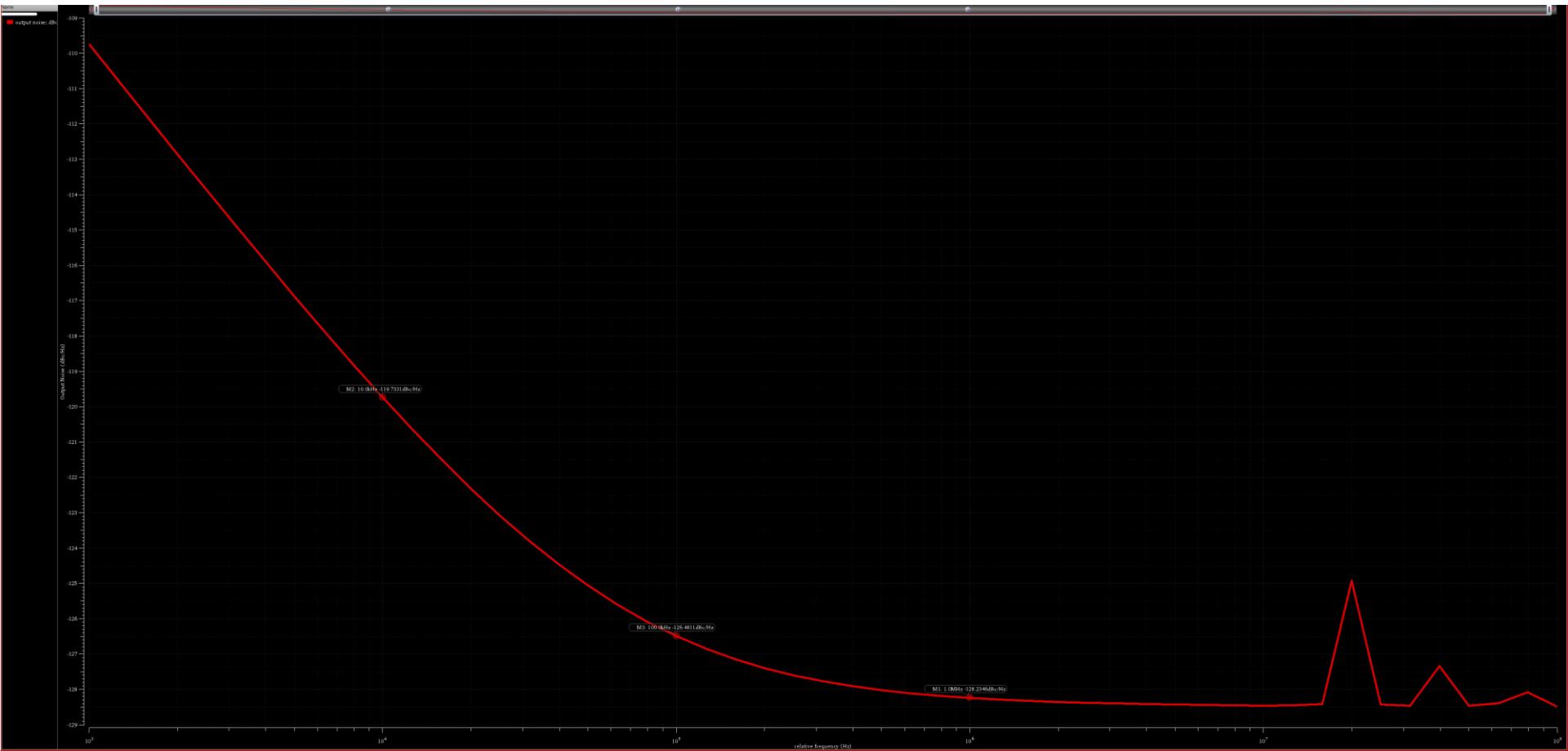


# *PFD&CP\_Phase Noise*

PN=-119dBc/Hz@10kHz

PN=-126dBc/Hz@100kHz

PN=-128dBc/Hz@1MHz



# Loop Filter Challenge

Issue: Large C in loop filiter would occupy too large area

My solution: I) Cap multiplication: Dual Path LPF

II) Layout: Mos cap & MoM cap overlap

$$\frac{V_c(s)}{I_{cp}(s)} = \frac{1}{sC_2} + \frac{B}{sC_1 + 1/R_1} = \frac{1 + sR_1(C_1 + BC_2)}{sC_2(1 + sR_1C_1)}.$$

$$\omega_Z = \frac{1}{R_1(C_1 + BC_2)}$$

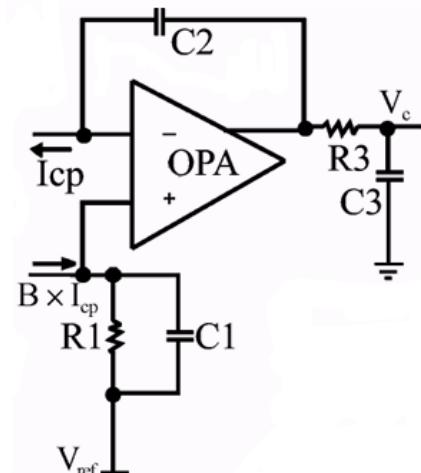
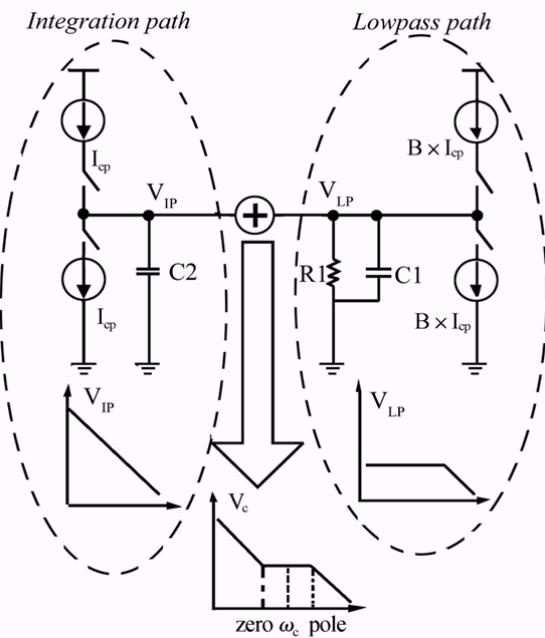
Compare with passive RC:

$$\frac{V_c(s)}{I_{cp}(s)} = \frac{1}{sC_2 + \frac{1}{R_1 + 1/sC_1}} = \frac{1 + sR_1C_1}{s(C_1 + C_2)\left(1 + \frac{sR_1C_1C_2}{C_1 + C_2}\right)}.$$

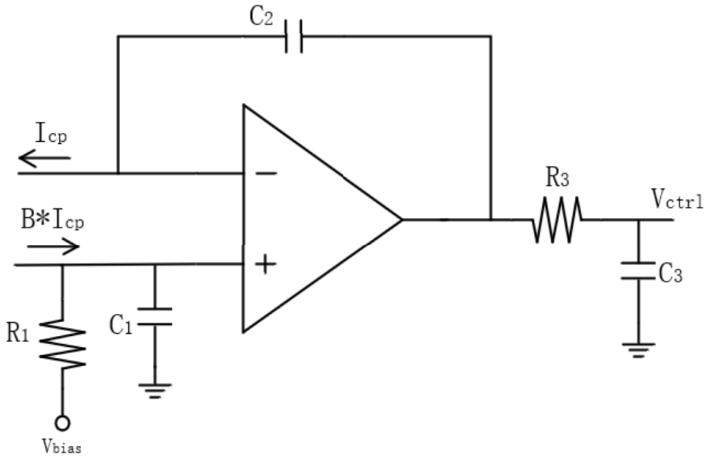
$$\omega_{Z'} = \frac{1}{R_1C_1'}$$

If B=10, make  $\omega_Z = \omega_{Z'}$ ,  $R_1(C_1 + 10C_2) = R_1C_1'$

$\Rightarrow$  Effectively reduce  $C_1$  Value to  $1/10 C_1'$



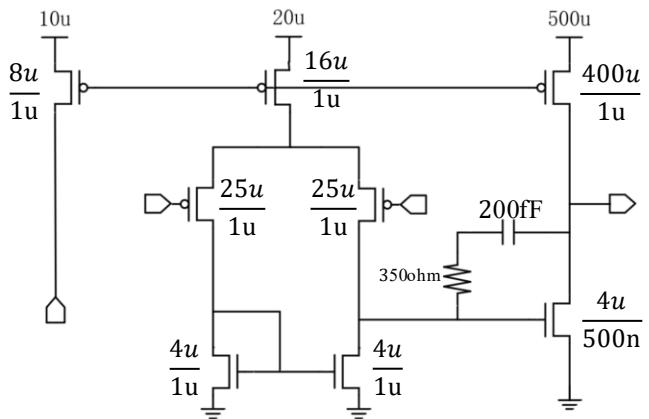
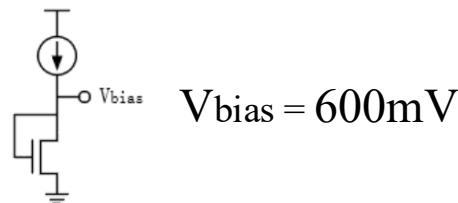
# Dual-Path LPF Implement



I set :  $R_1 = 45\text{k ohm}$

$C_1 = 119\text{fF}$

$C_2 = 704\text{fF}$



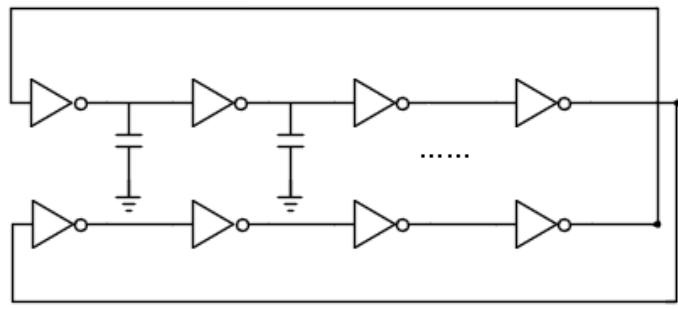
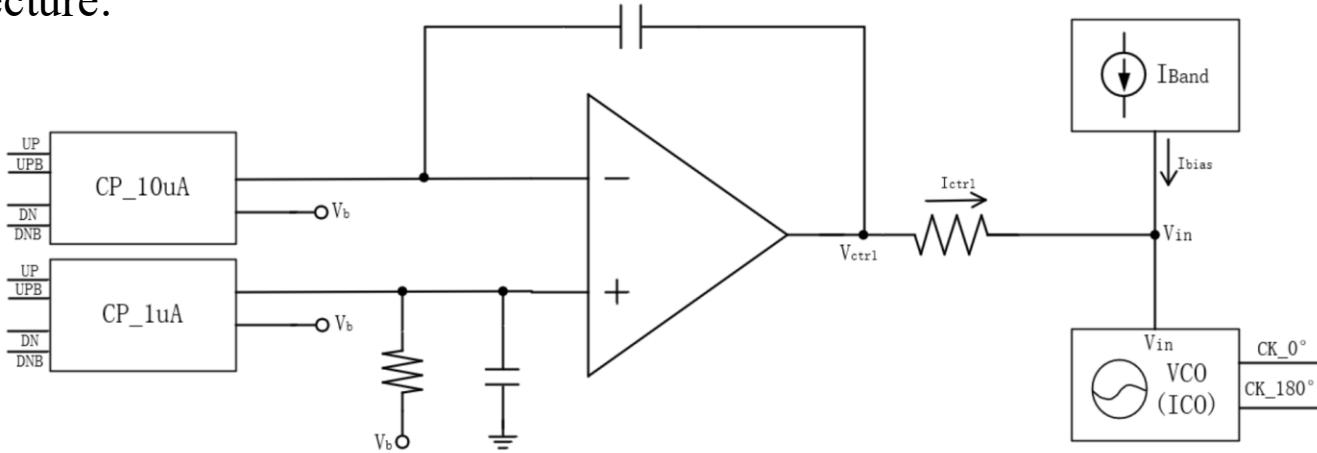
Op-amp Design spec:

- 1) DC Gain > 40dB.
- 2) BW > 50MHz.
- 3) Output Stage current:  $-2*I_{CP} \sim +2*I_{CP}$ .
- 4) Low Noise

the LPF op-amp stabilizes the CP output voltage by Vbias, simplifying CP design

# VCO/ICO

Architecture:



For Ring Oscillator,

The performance of a ring oscillator is affected by bias current and supply voltage.

$$f_0 = \frac{1}{2N\tau_{\text{delay}}}, \quad \tau_{\text{delay}} = \tau_0 + \frac{C}{I}$$

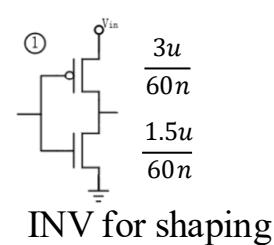
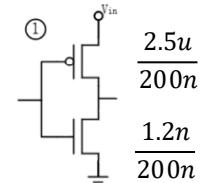
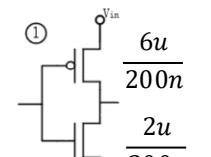
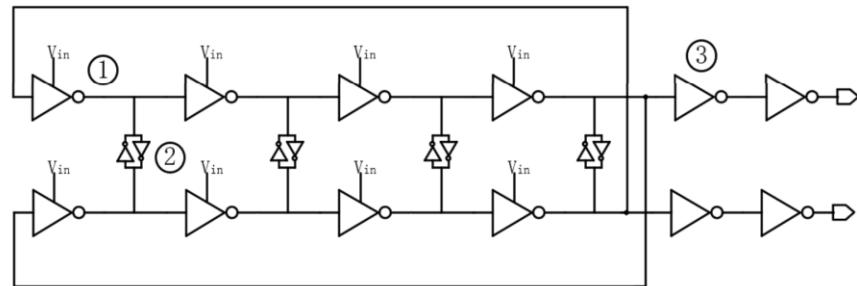
$$K_{\text{ICO}} = \frac{\partial f}{\partial I} = \frac{C}{2N(C + I * \tau_0)^2}$$

Power  $\leftrightarrow$  Phase Noise  $\leftrightarrow K_{\text{ICO}}$

# *Ring OSC & IBand Implement*

## VCO:

According to the Barkhausen Criterion, Adopted a 4-stage pseudo-differential ring oscillator to meet the half-rate output requirement for 0 and 180 phases.

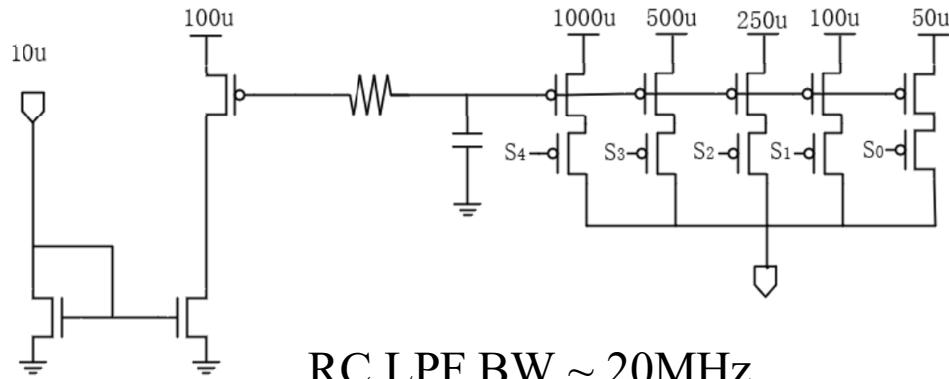


Issue: Even-stage ring oscillators suffer from startup issues

My Solution: Adding Latch to break the stable state and initiate oscillation.

$$\text{Sizing the latch: } \left(\frac{W}{L}\right)_{\text{INV}} = 2 \sim 3 \times \left(\frac{W}{L}\right)_{\text{Latch}}$$

## IBand:



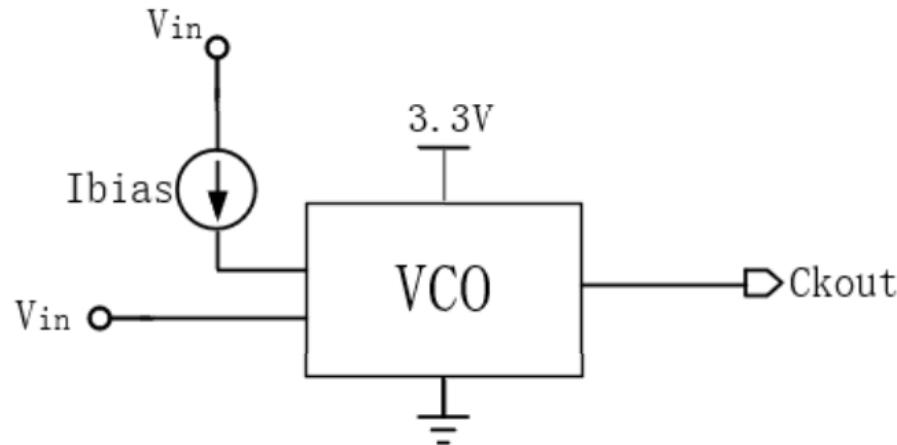
The I-band provides low-noise current to the VCO to improve phase noise.

And Reducing the loop filter bandwidth further improves phase noise.

# *Ring OSC*

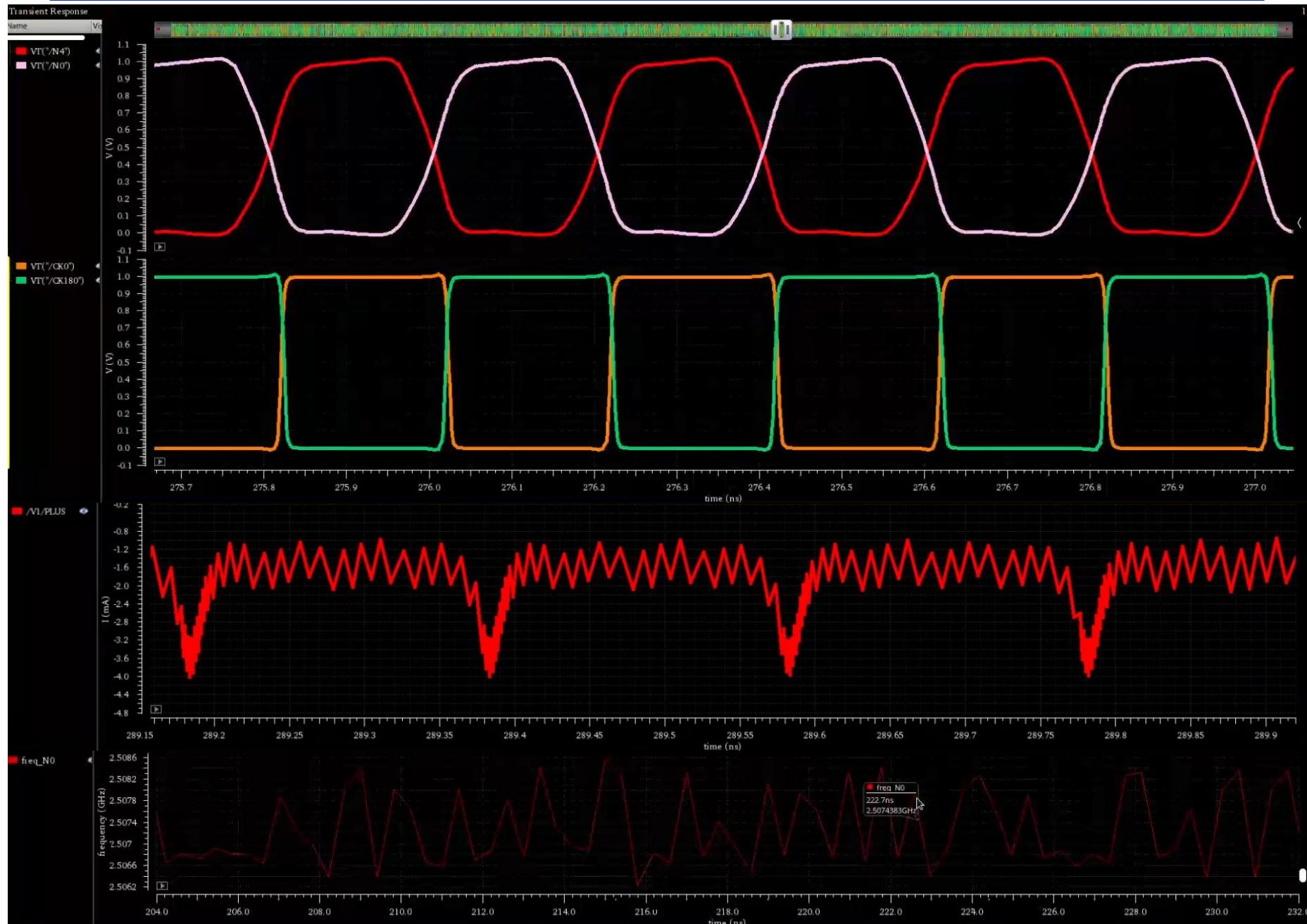
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Test Bench:



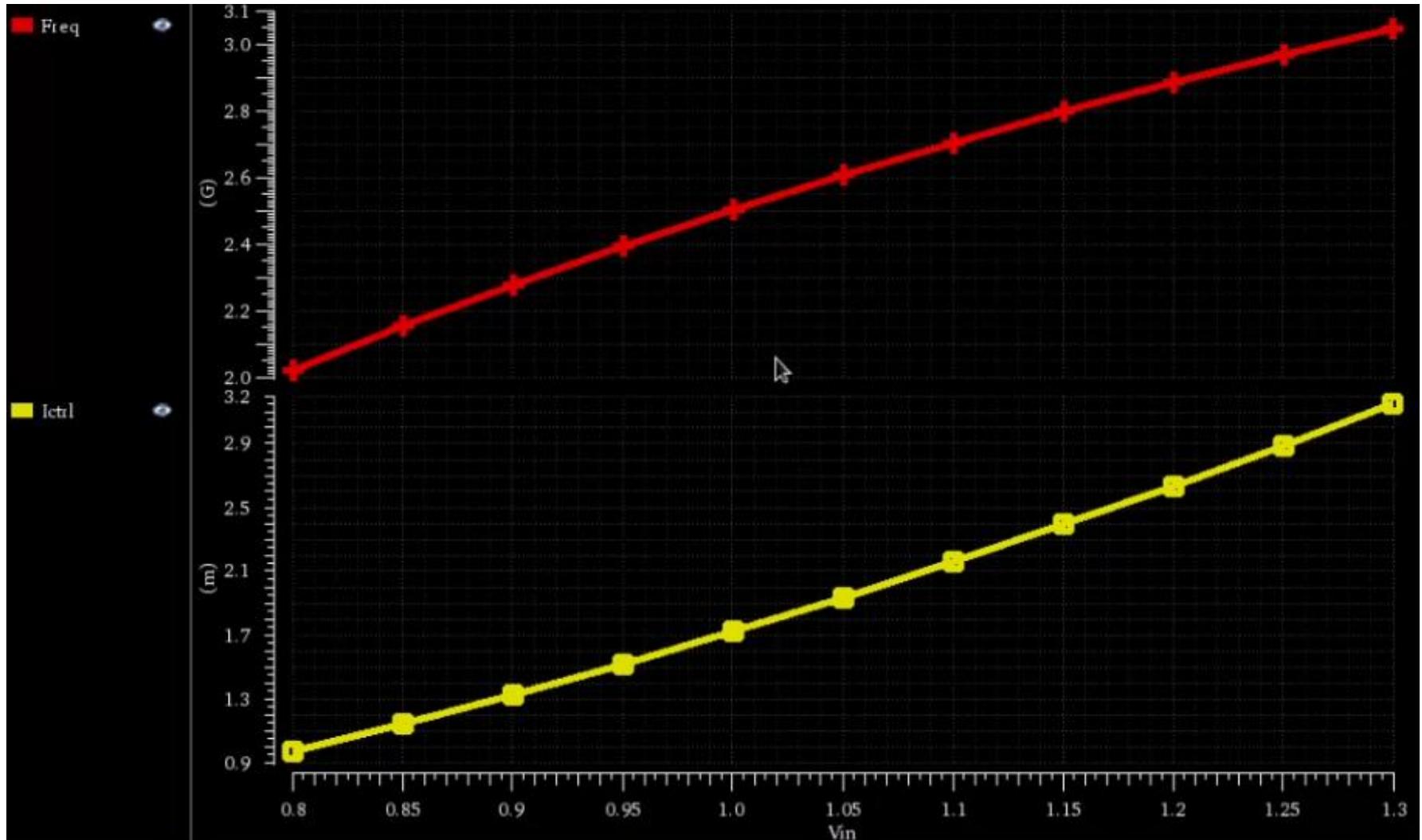
- Simulation Check List:
1. VCO/ICO frequency tuning range---2500MHz
  2. ICO/VCO small signal gain( $K_{ICO}/ K_{VCO}$ )
  3. Phase Noise (PSS+Pnoise)
  4. Start-up

# Ring OSC\_Waveform



# *Ring OSC\_Tuning Range*

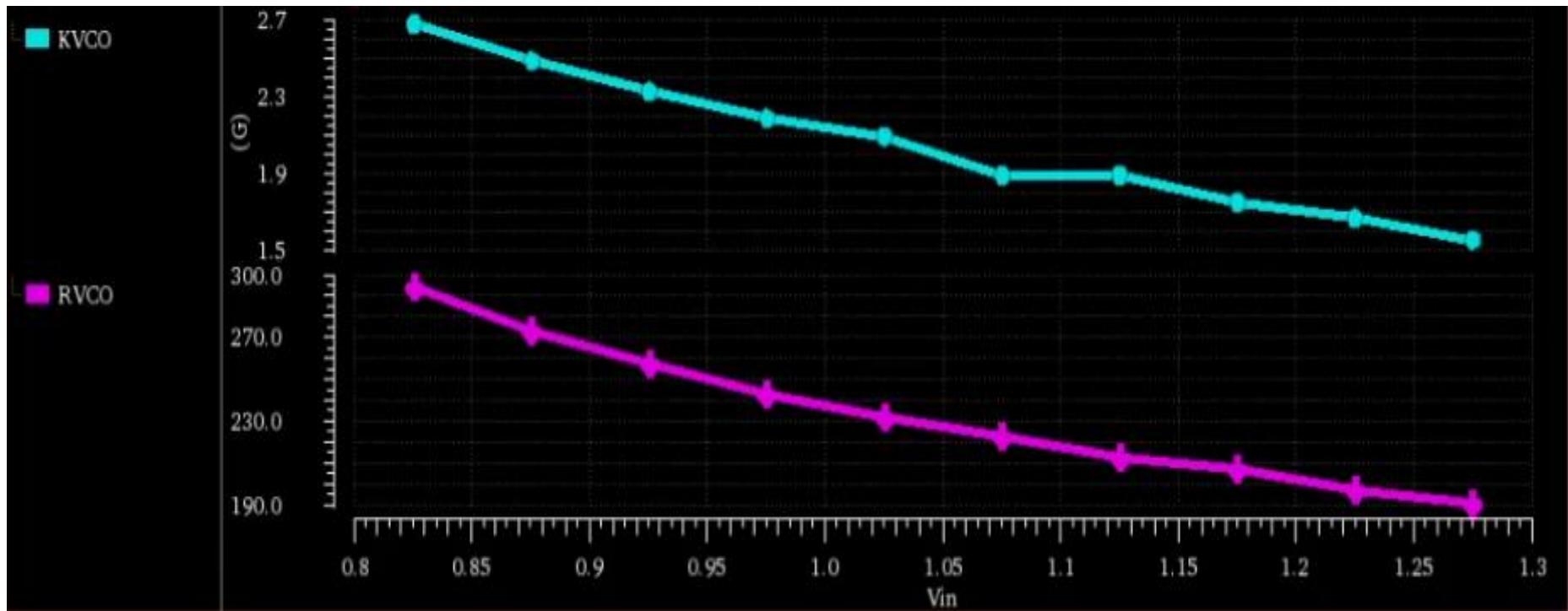
As Freq=2.5GHz, Vctrl=996mV, Ictrl=1.716mA



# *Ring OSC\_ K<sub>VCO</sub> / R<sub>VCO</sub>*

As Freq=2.5GHz, Vctrl=996mV, Kvco=2.1526G, Rvco=239ohm

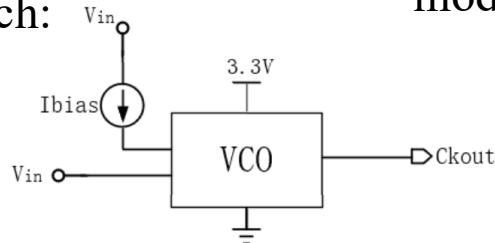
$$K_{ICO} = K_{VCO} \cdot R_{VCO}, K_{ICO} = 514.4714 \text{ G}$$



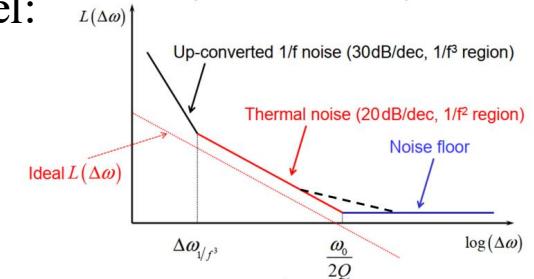
# Ring OSC\_Phase Noise

PSS+Pnoise

Test Bench:

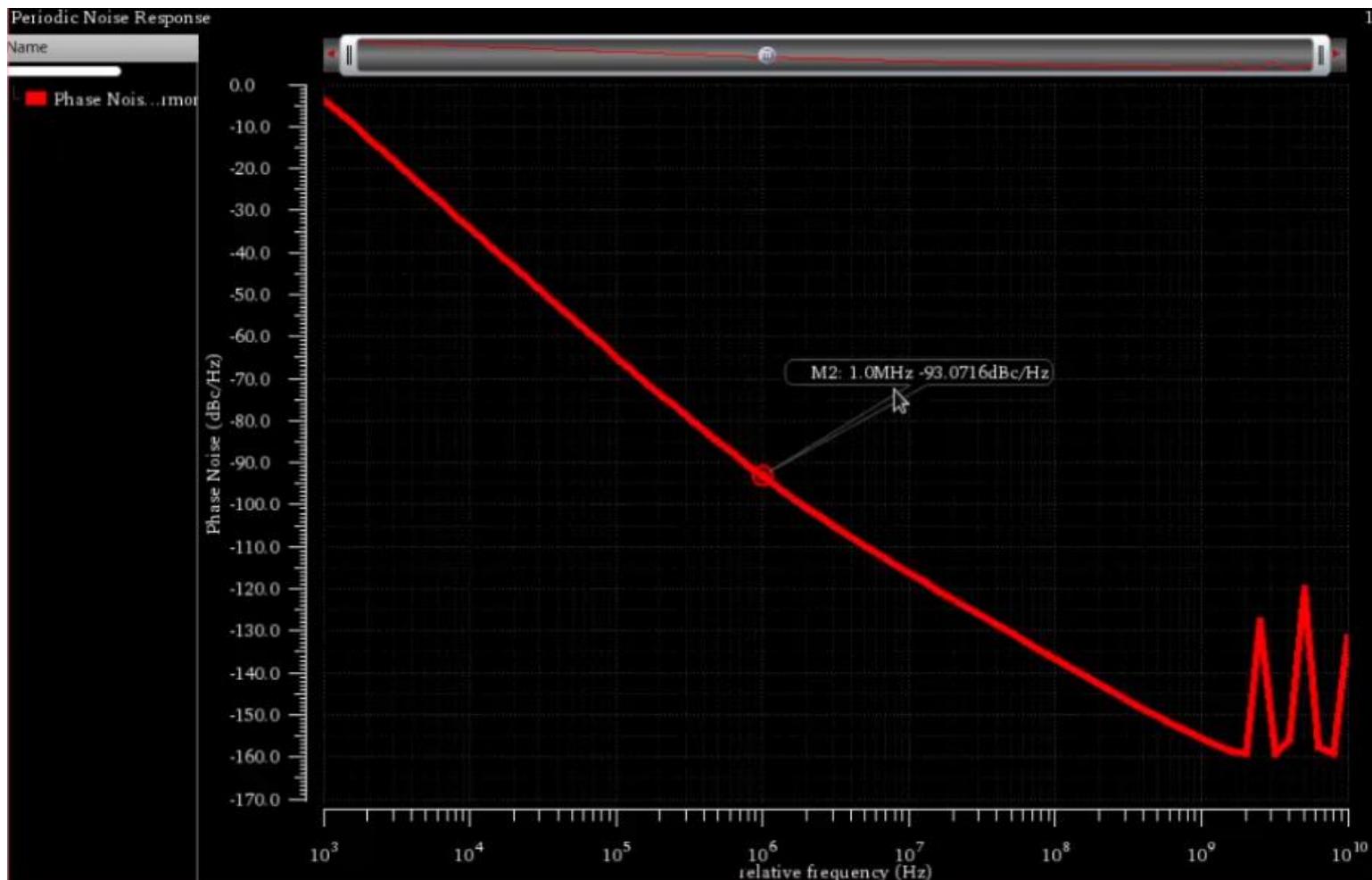


model:



PSS: convergence @ 2.509GHz

PN=-93dBc/Hz@1MHz

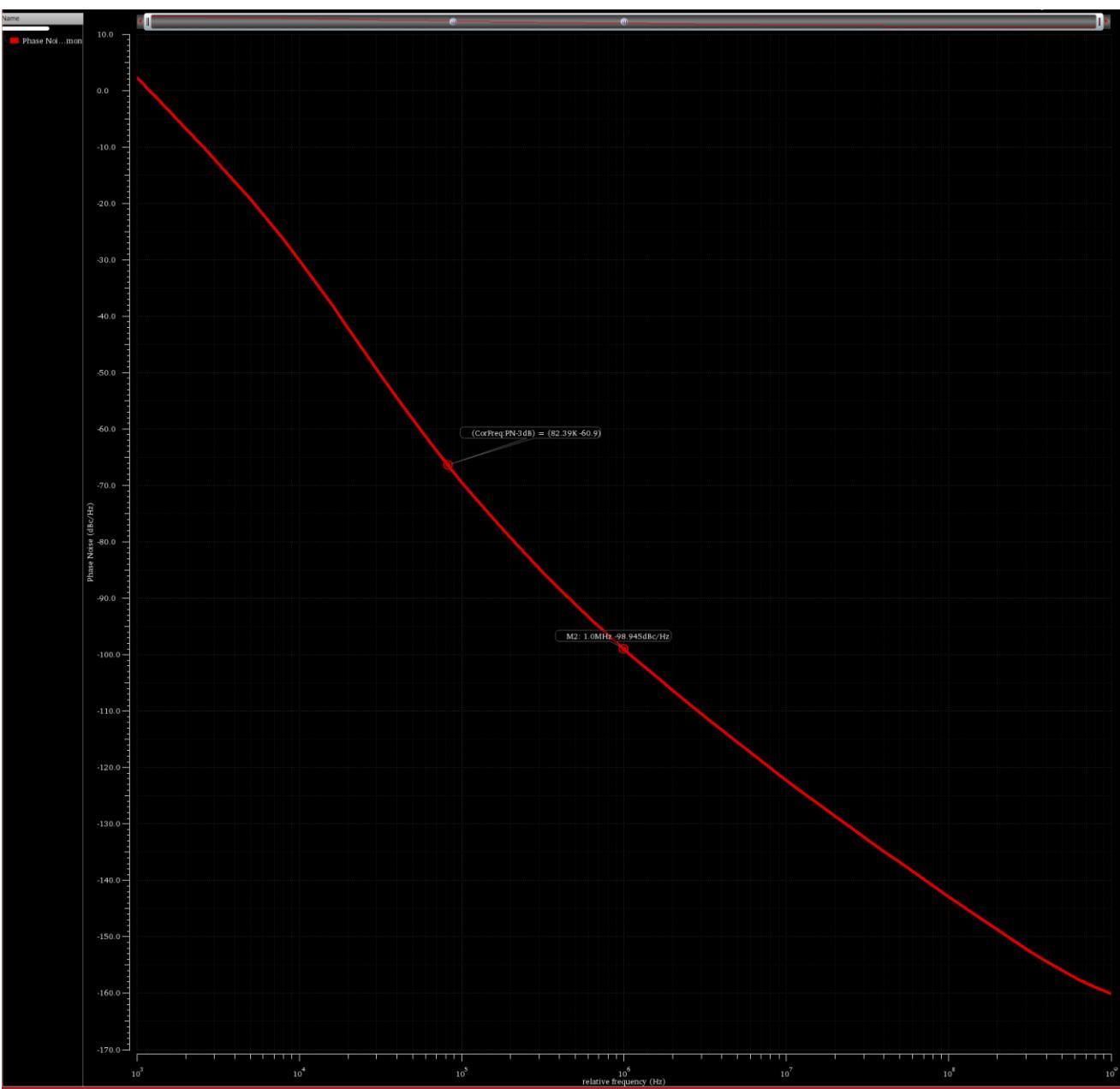
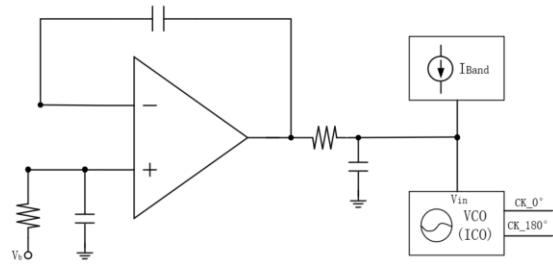


# *LPF&VCO&IBand\_Phase Noise*

PSS: convergence @ 2.526GHz

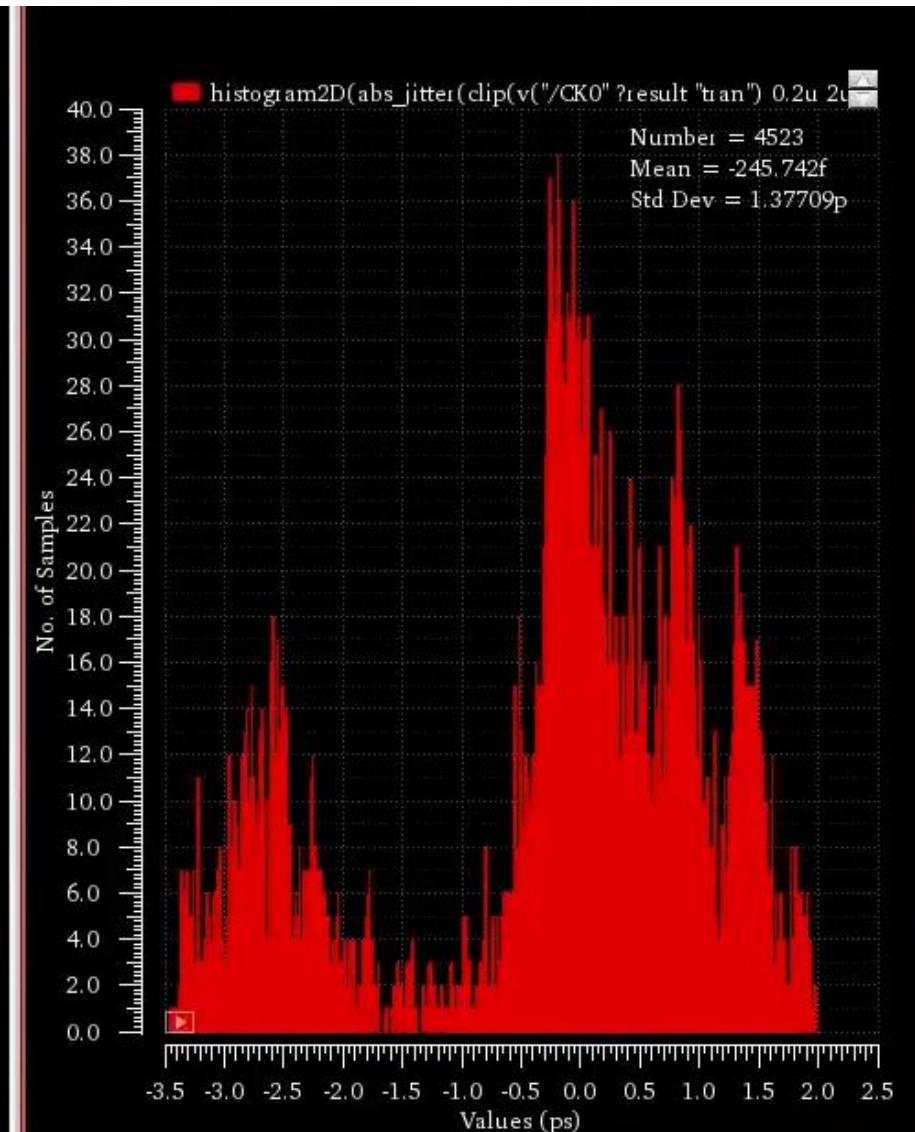
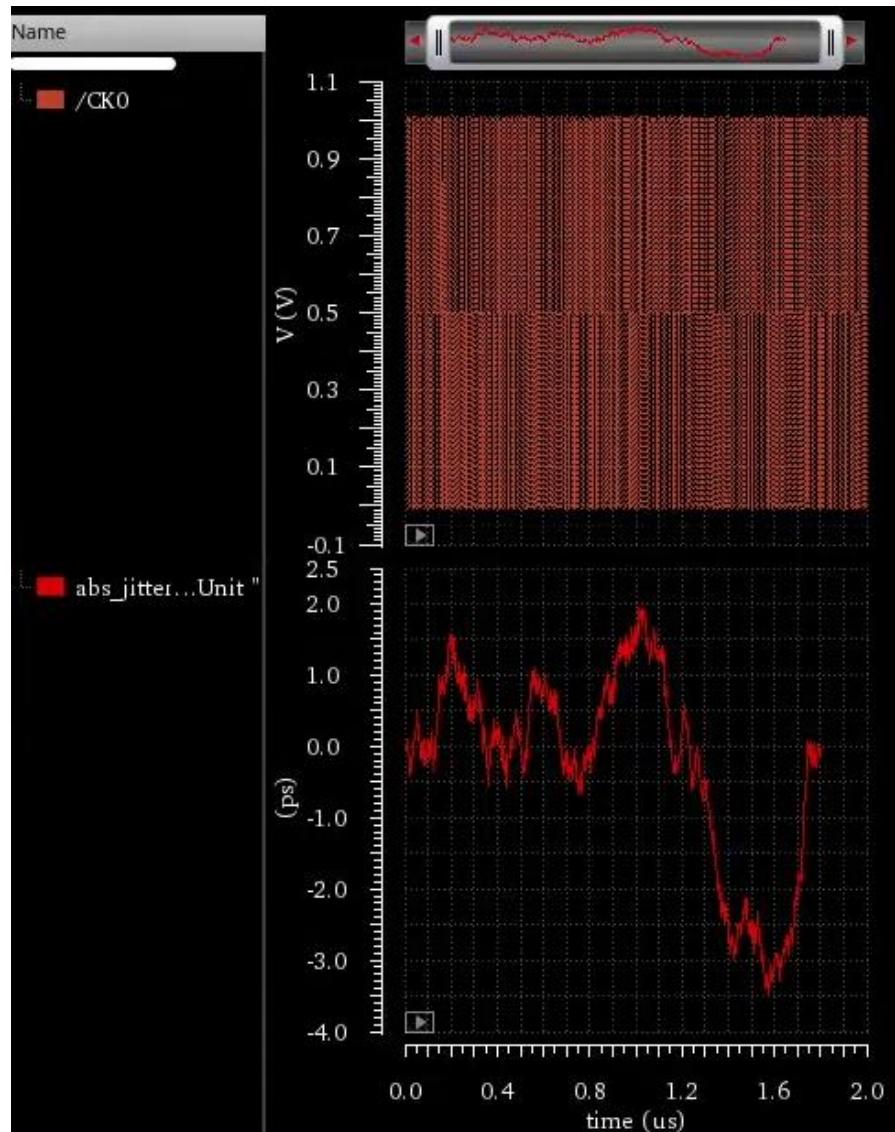
PN=-98.9dBc/Hz@1MHz

Test Bench:



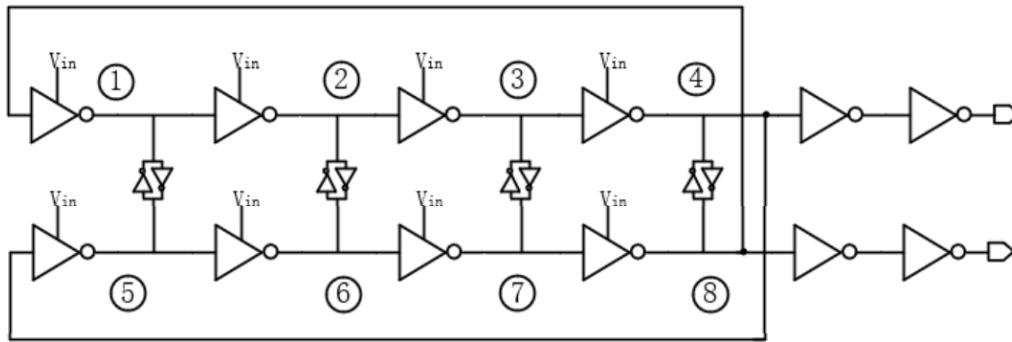
# *Ring OSC\_jitter*

Tran + Calculator abs jitter



# *Ring OSC\_Start-up*

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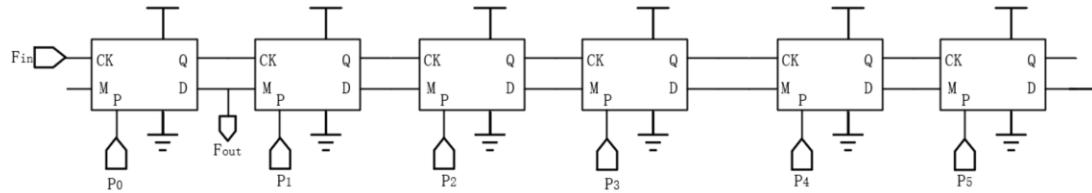
Initial condition set: 00000000,  
11111111,  
01010101,  
10101010, etc.

To ensure reliable VCO start-up under all operating conditions.

# Divider&PostDIV

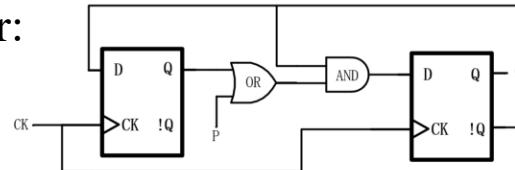
The Divider is built by cascading 6 stages dual-modulus divider.

Adopts an asynchronous connection to cut power, at the cost of jitter accumulation.

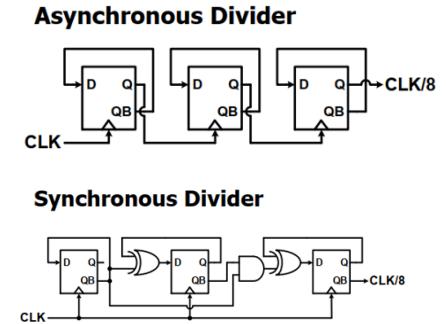
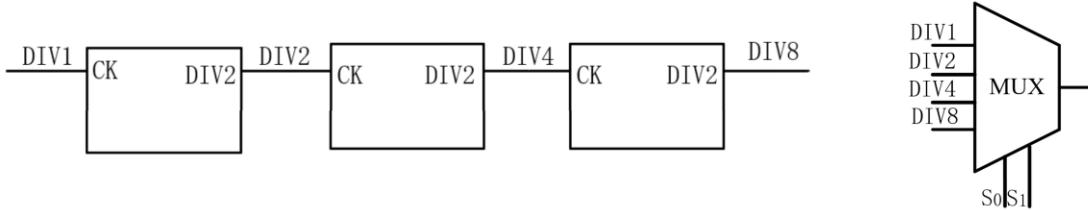


$$6\text{bit: } N = 64 + 32*P_5 + 16*P_4 + 8*P_3 + 4*P_2 + 2*P_1 + P_0$$

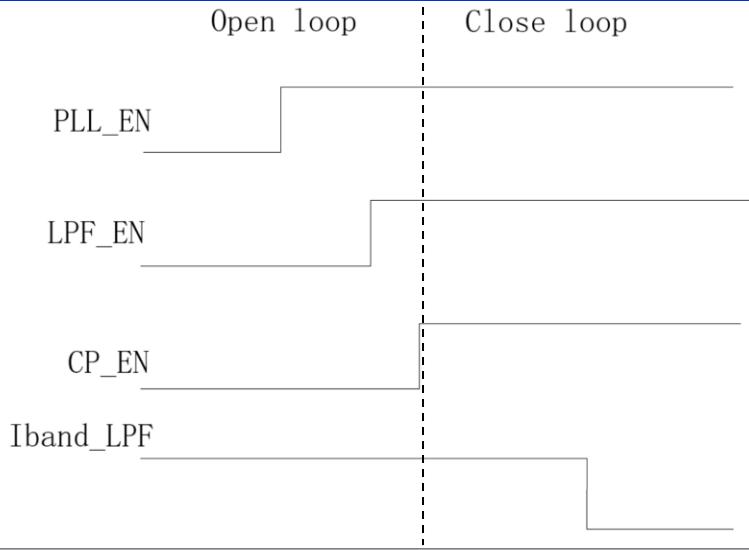
ex. 2/3 dual-modulus Divider:



PostDIV provides four selectable output frequencies,  
and reduces the phase noise of lower-frequency output frequencies.

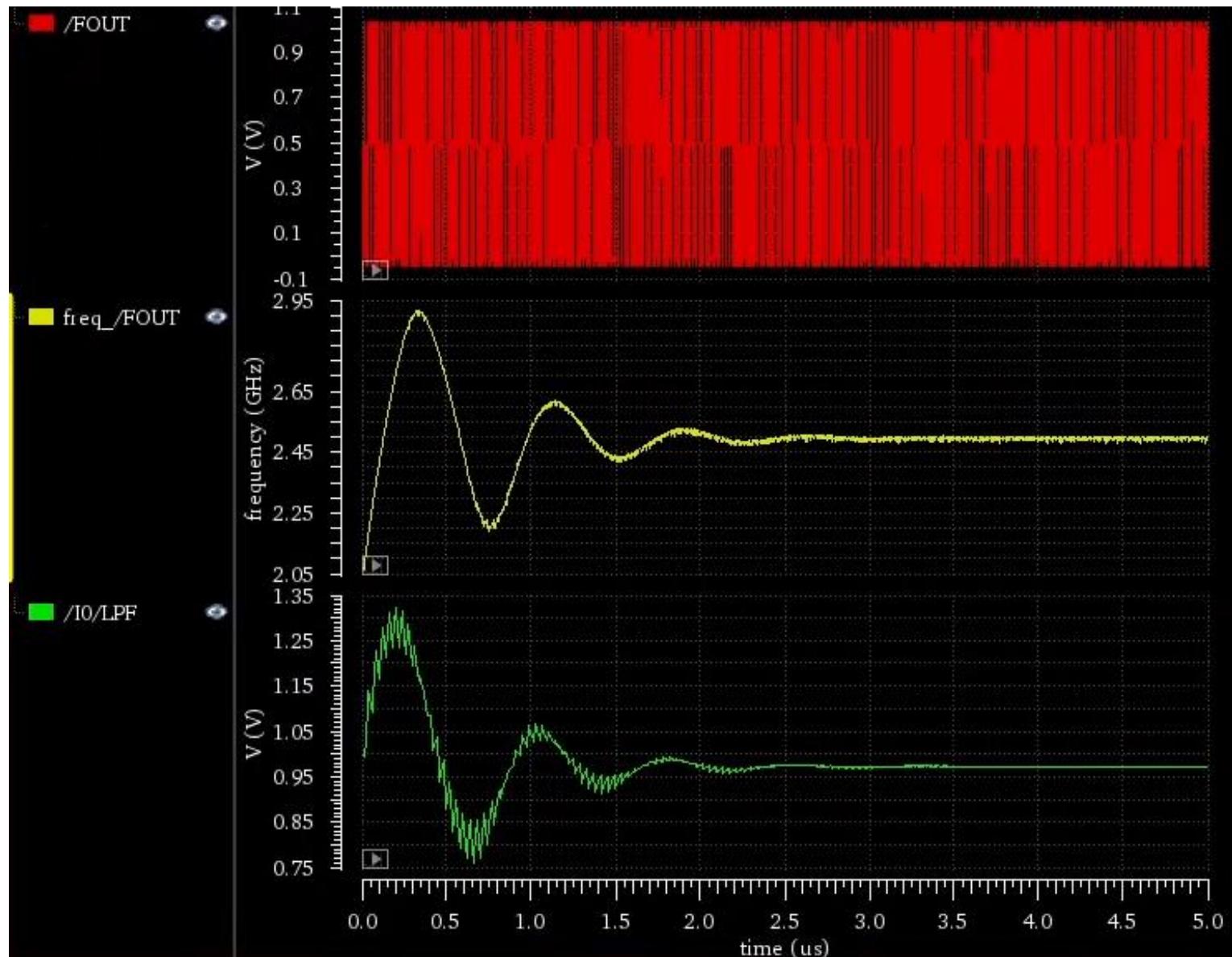


# *TOP Check\_PLL\_EN Sequence*



# *TOP Check\_PLL\_ Output Frequency*

AS PLL Locked, Output Frequency = 2.50GHz, settle time 4us



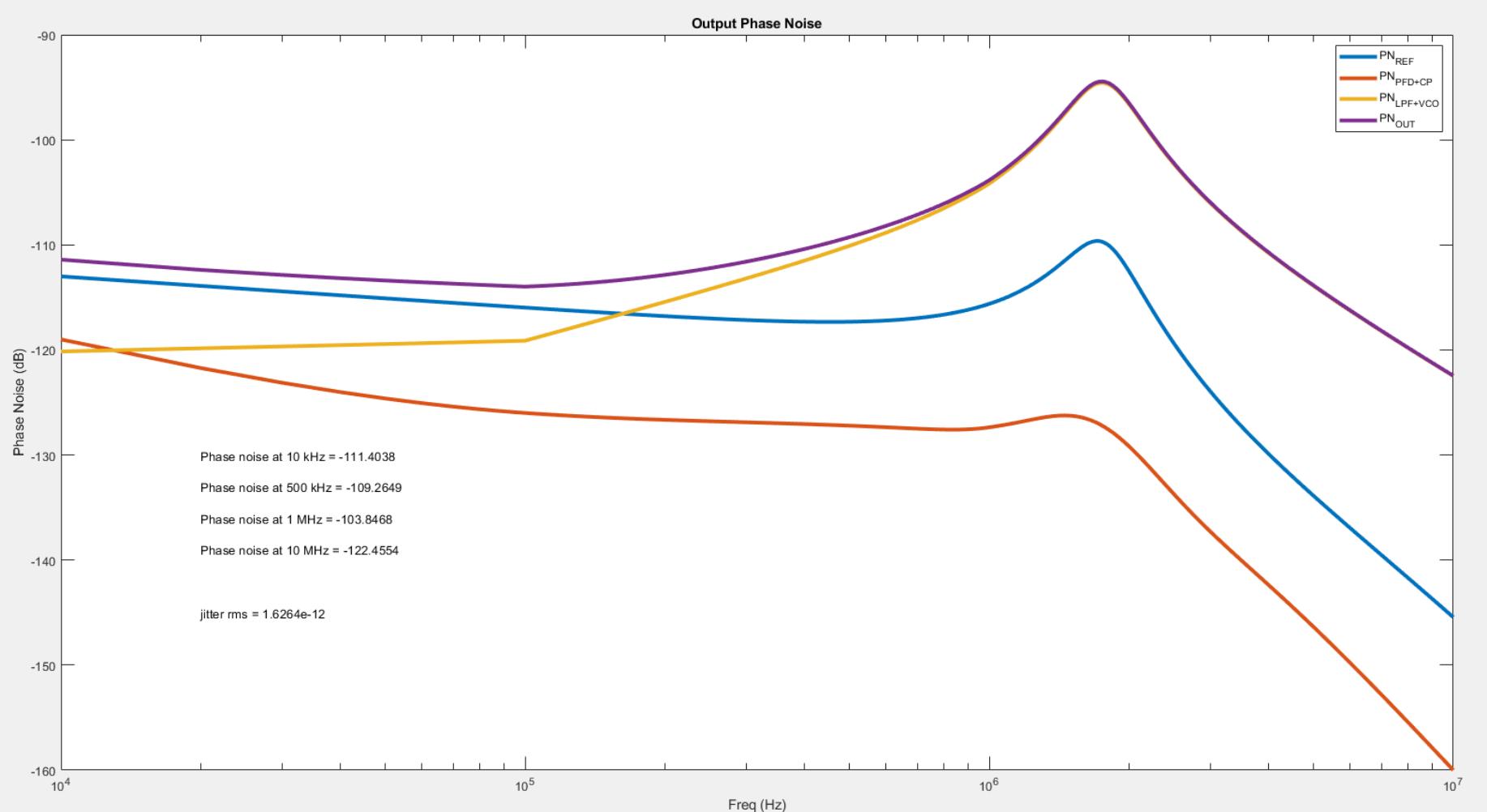
# *TOP Check\_PLL\_Phase Noise to jitter*

MATLAB to sum PN and convert to jitter.

PLL Phase Noise = -103.8dB@1MHz

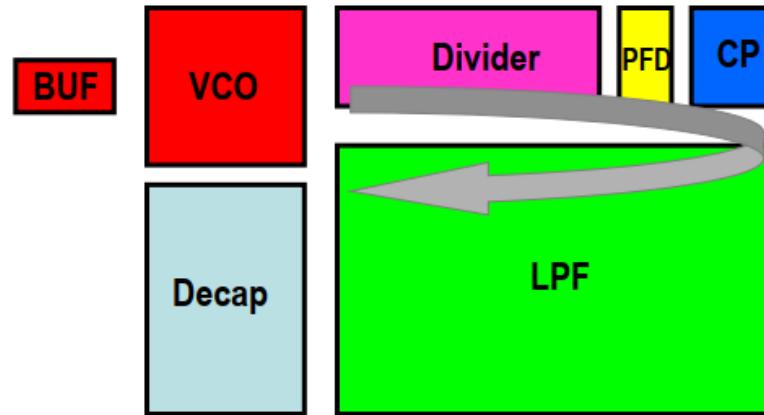
PLL Phase Noise = -127.9dB@10MHz

Jitter Rms= 1.63ps



# *FloorPlan*

- 1) Floorplanned cells along the signal flow, keep modules rectangular for easier integration;
- 2) Isolated analog and digital sections by decoupling capacitors to reduce noise, and minimized digital area;
- 3) Ensured full symmetry for VCO ring cells/routing with metal ring shielding;
- 4) Maintained symmetrical, equal-length routing from PFD to CP to ensure simultaneous signal arrival;
- 5) Applied common-centroid matching for differential pairs in CP and LPF op-amps to reduce mismatch;
- 6) Implemented mesh Power/Ground routing within modules;
- 7) tree-style Power/Ground routing on the top metal to lower parasitic resistance;
- 8) Completed layout, performed DRC/LVS checks, and extracted parasitic parameters;



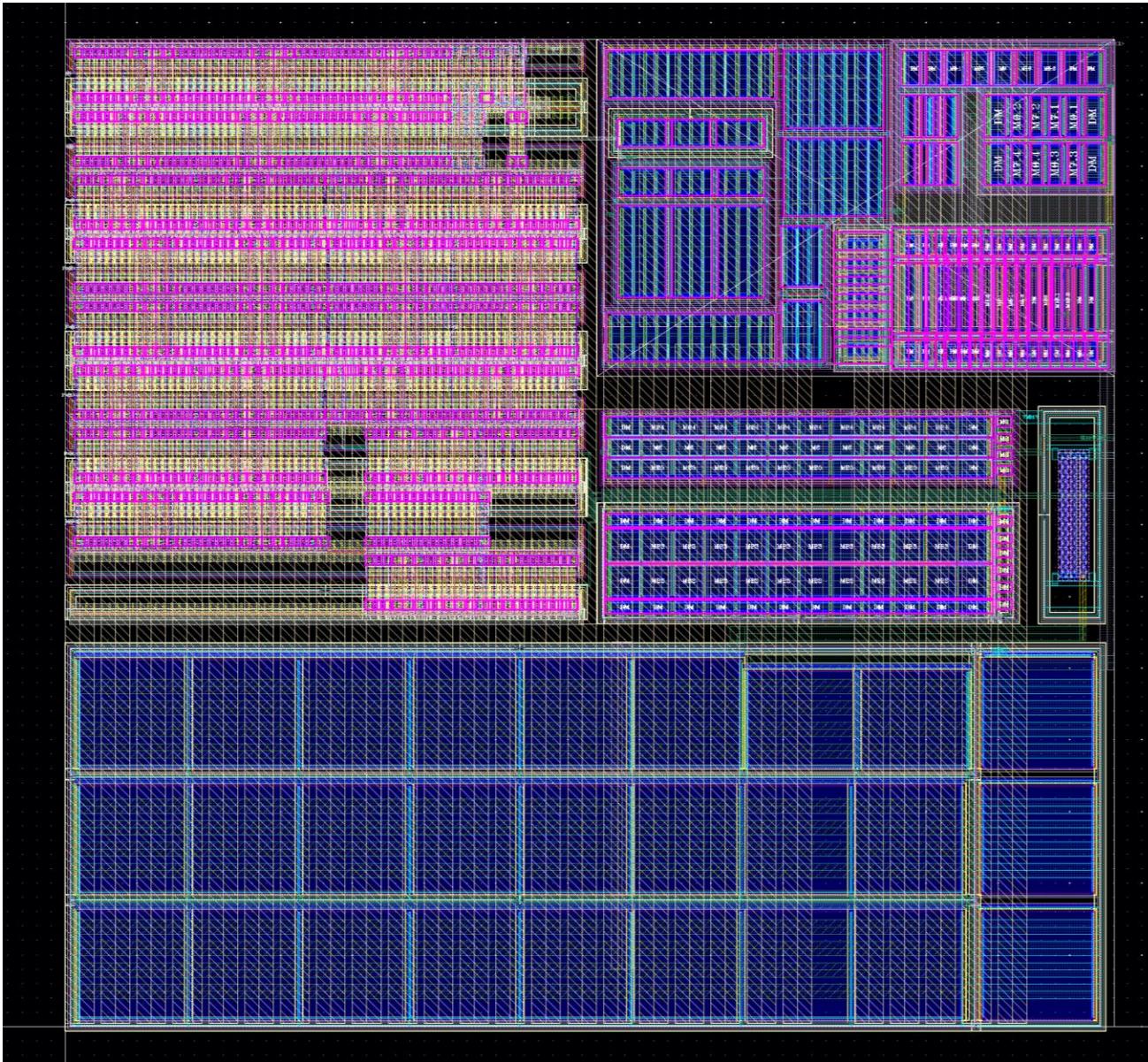
- **Signal flow:**

**VCO → Divider → PFD → CP → LPF → VCO**

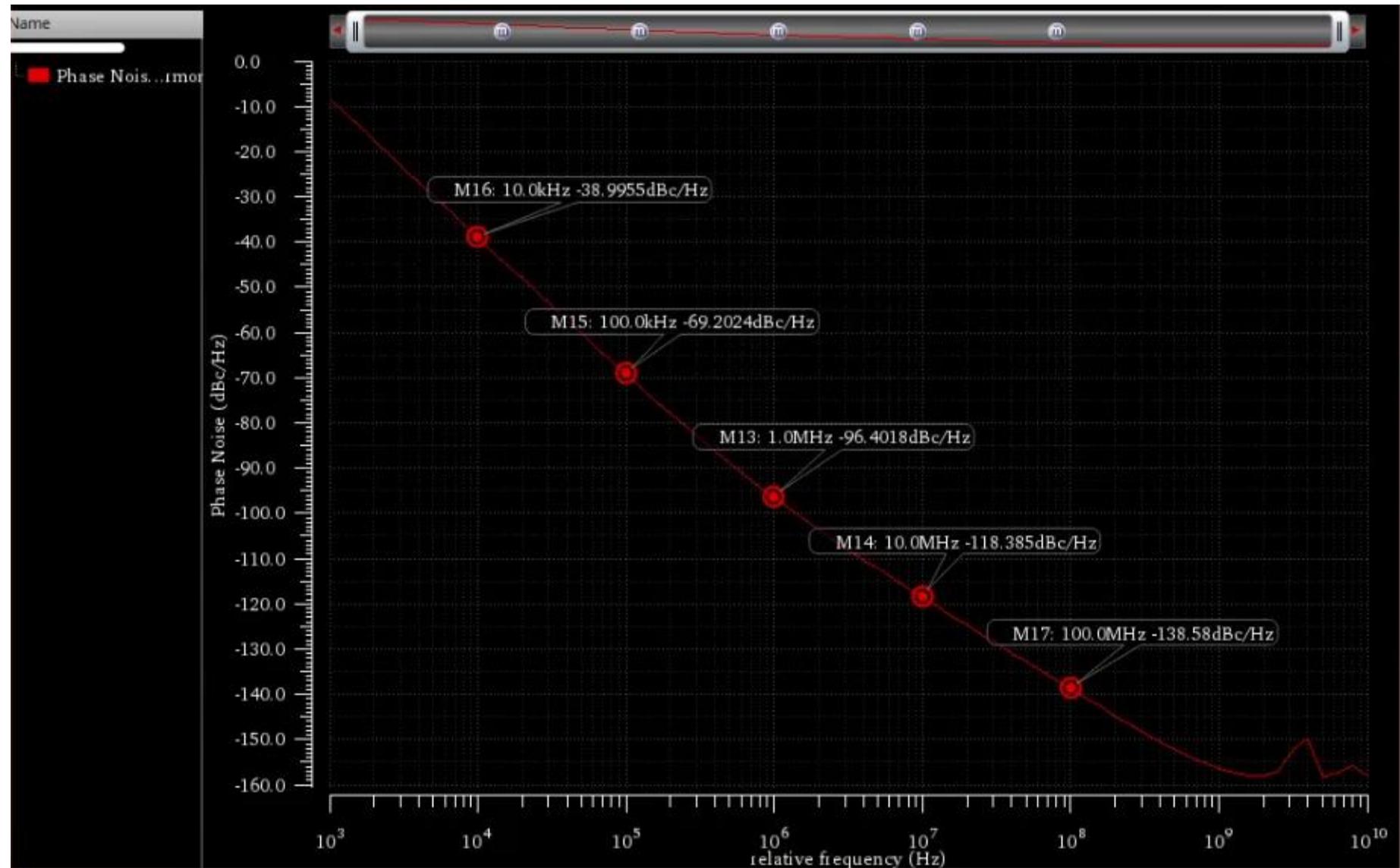
High freq.    High to low

Low freq.

# *PLL Layout Overall*

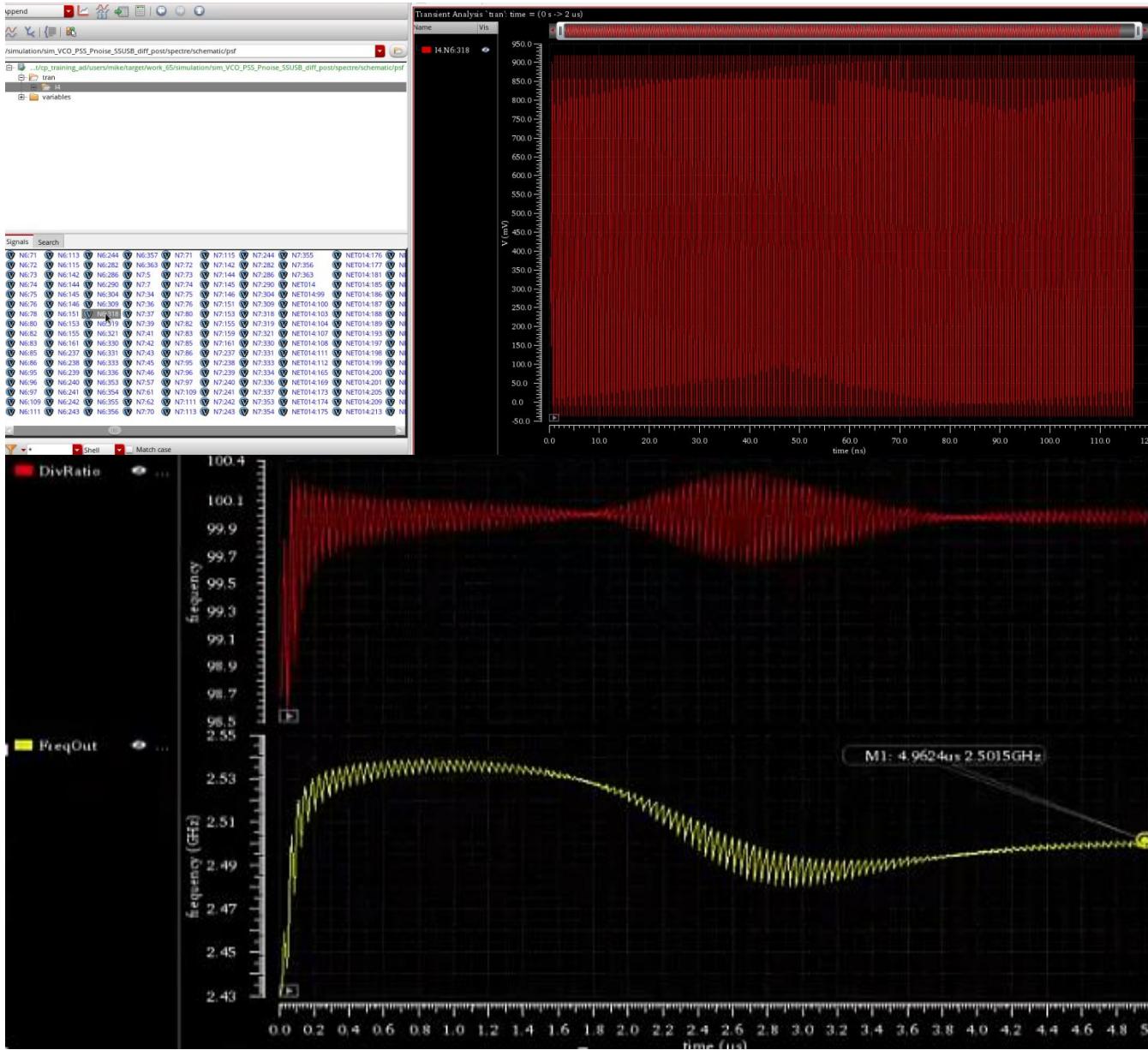


# *Post-sim\_VCO\_Phase Noise*



# *Post-sim\_PLL\_Output freq*

AS PLL Locked, Output Frequency = 2.50GHz, settle time 5us

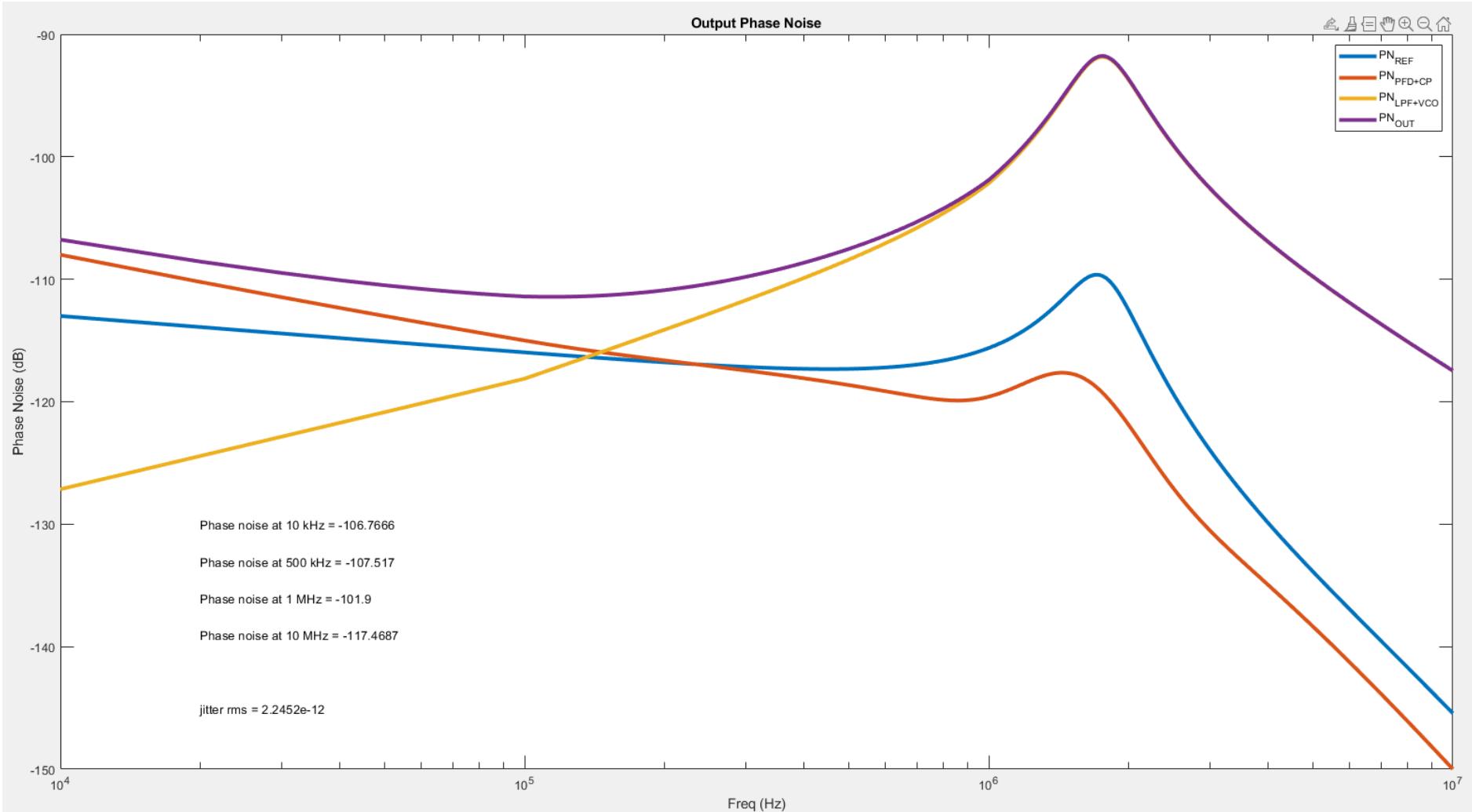


# *Post-sim\_PLL\_Phase Noise to jitter*

PLL Phase Noise = -101.9dB@1MHz

PLL Phase Noise = -116.9dB@10MHz

Jitter Rms= 2.25ps

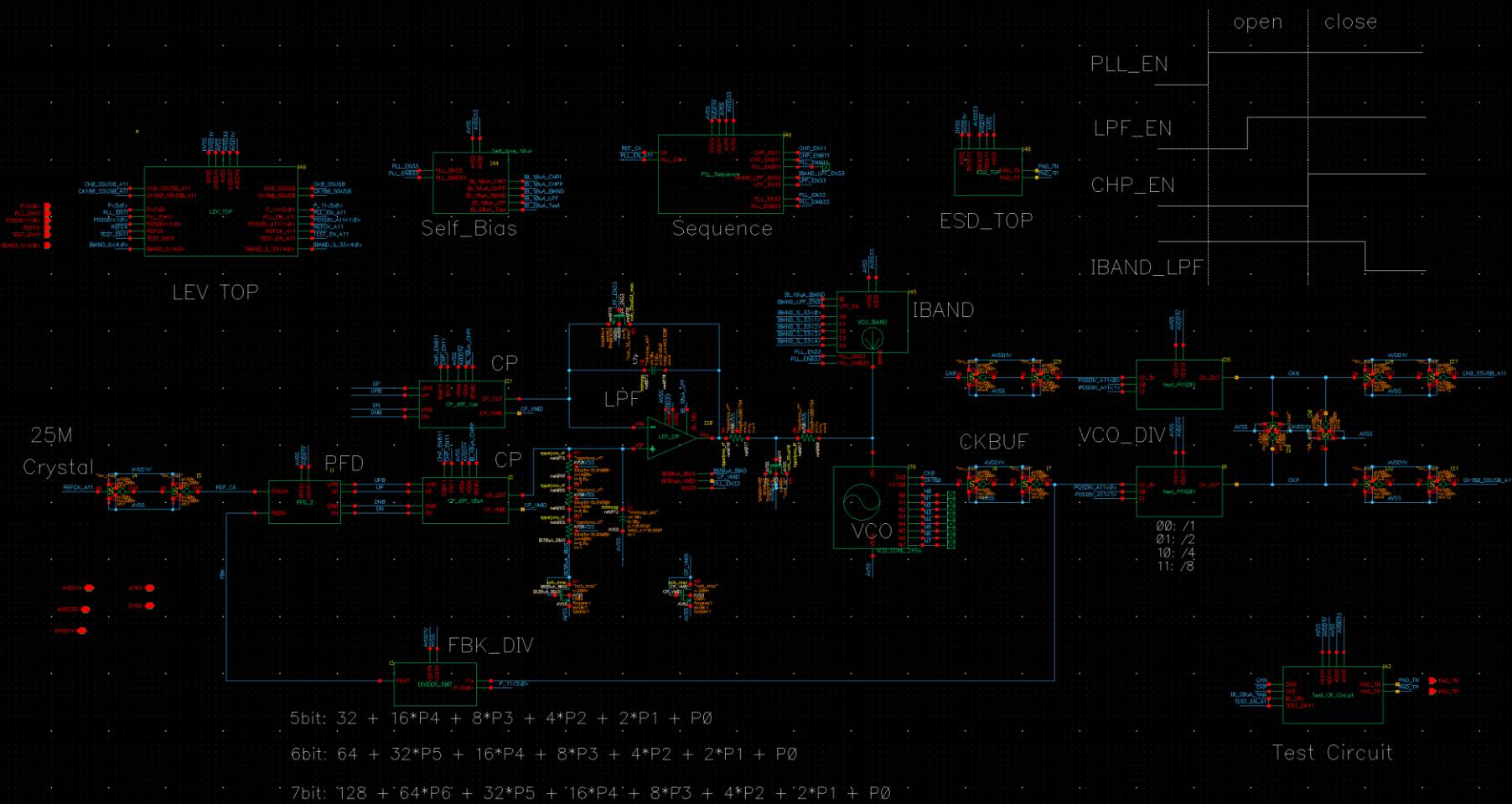


# References

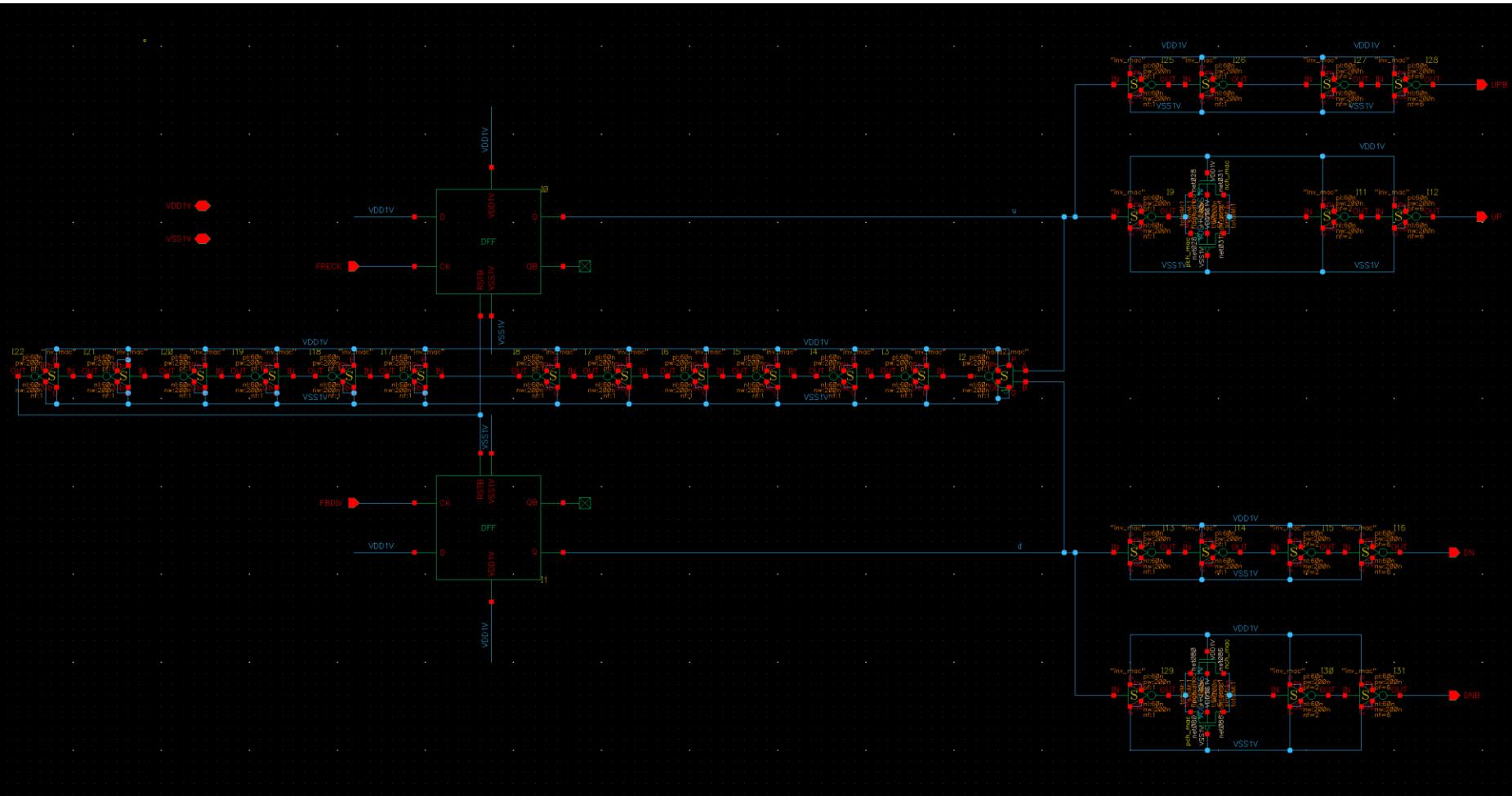
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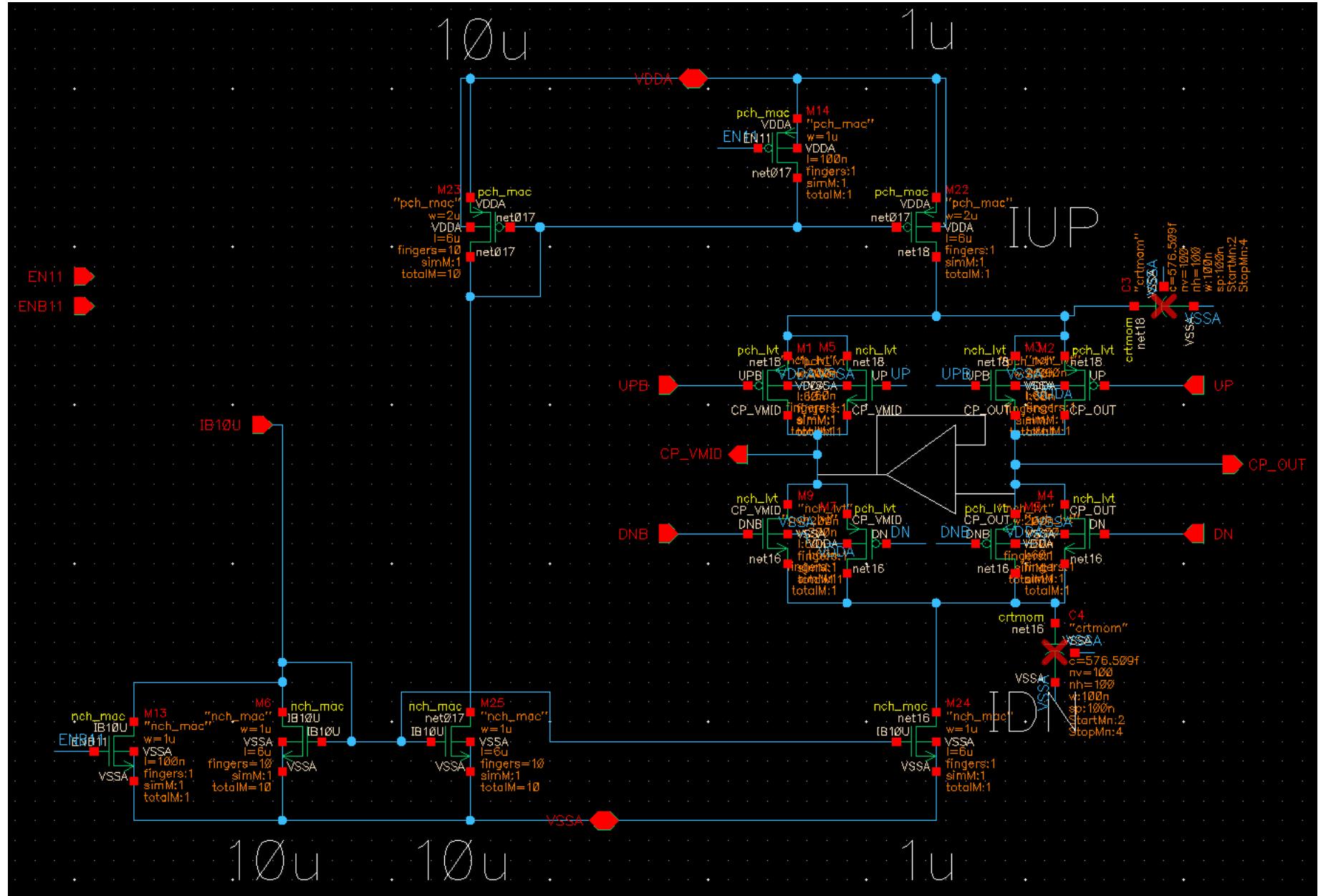
# Appendix: Sch Overview



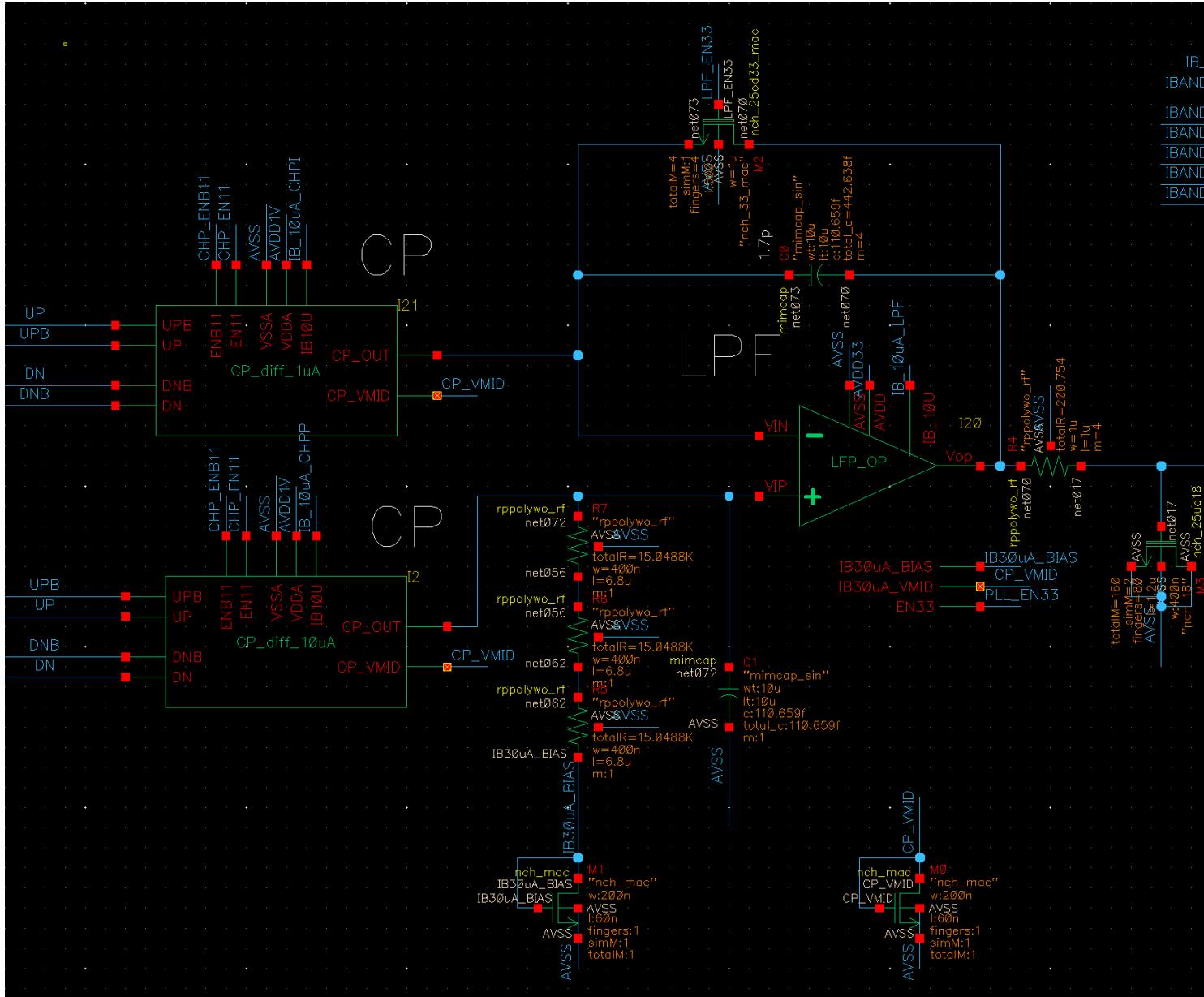
# Appendix: PFD Circuit



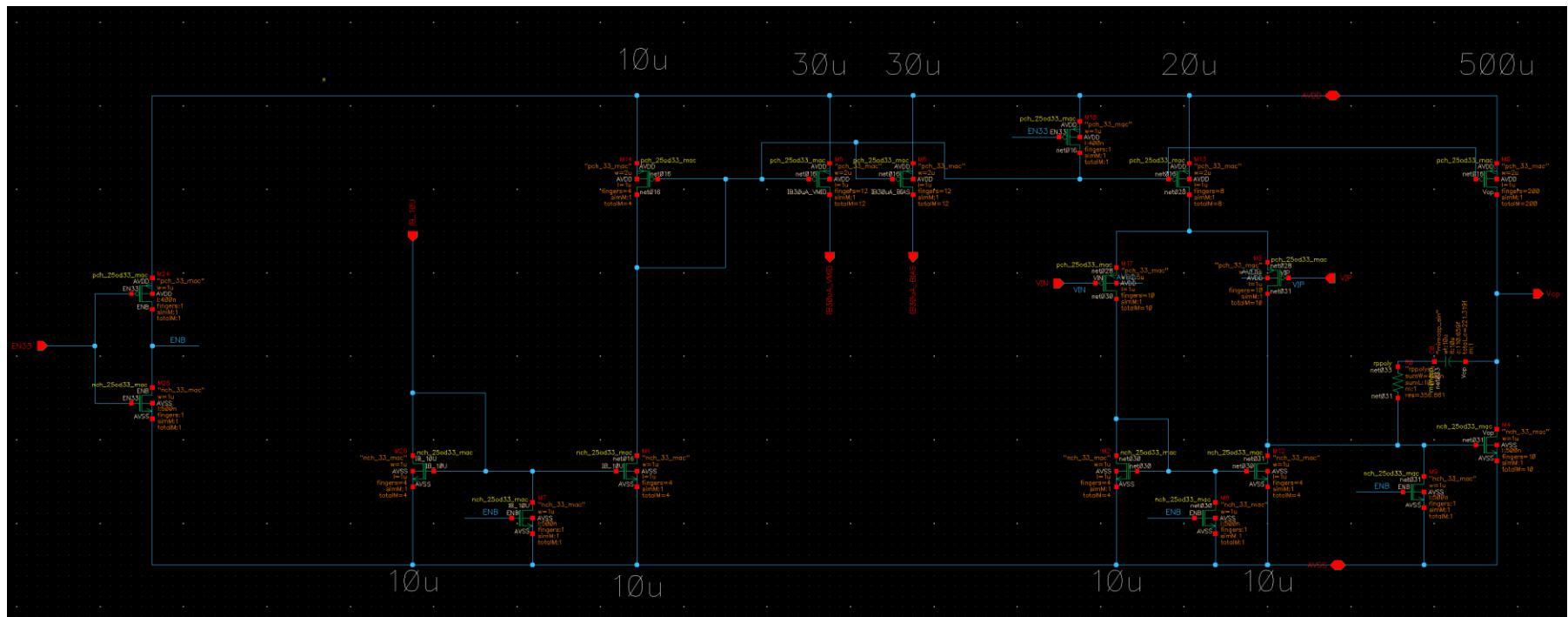
## *Appendix: CHP Circuit*



# *Appendix: Dual-Path LPF*

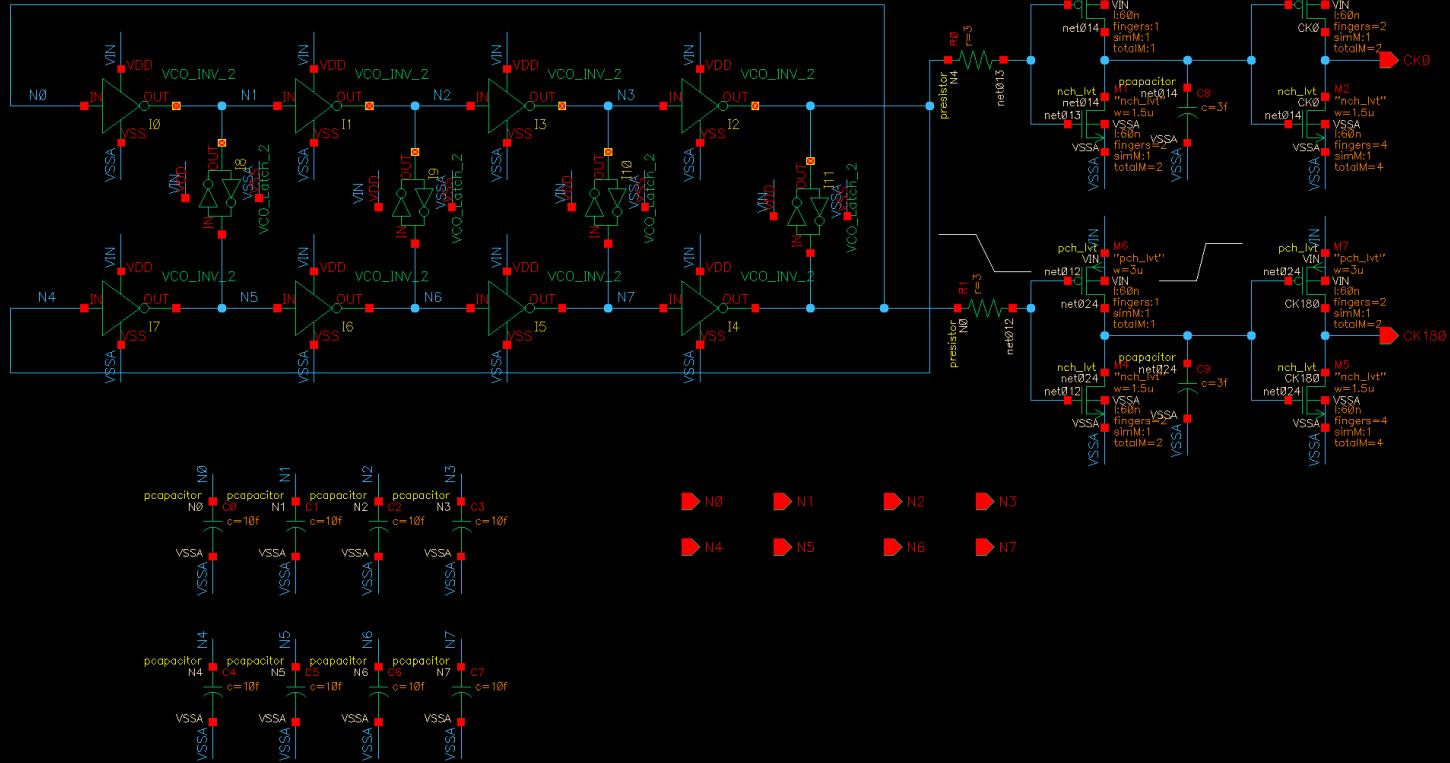


# Appendix: Dual-Path OPA



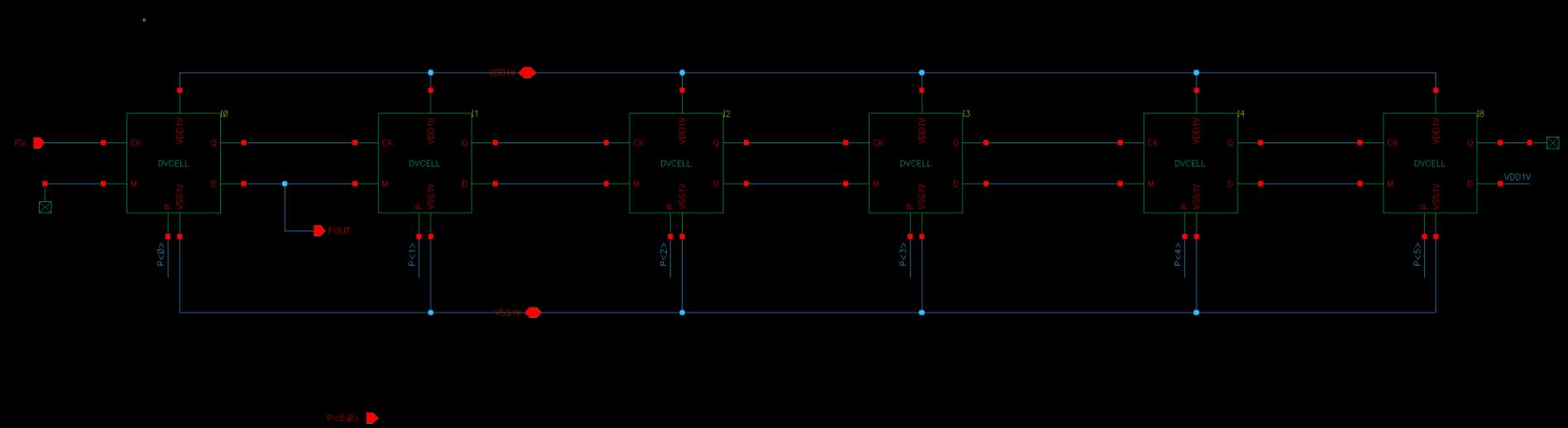
# Appendix: Ring Osc

VIN  
VSSA



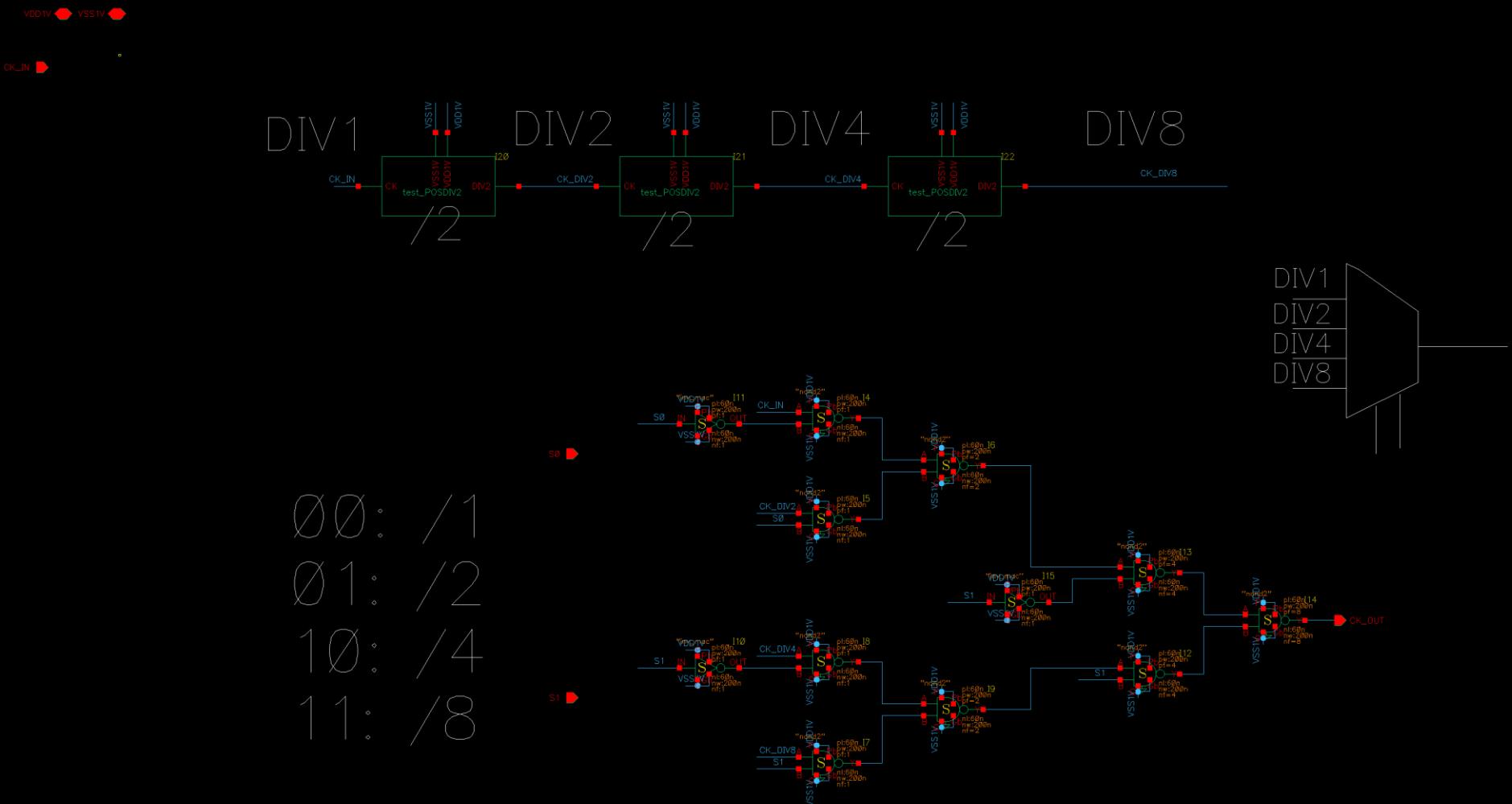
## *Appendix: IBand*

# Appendix: Divider

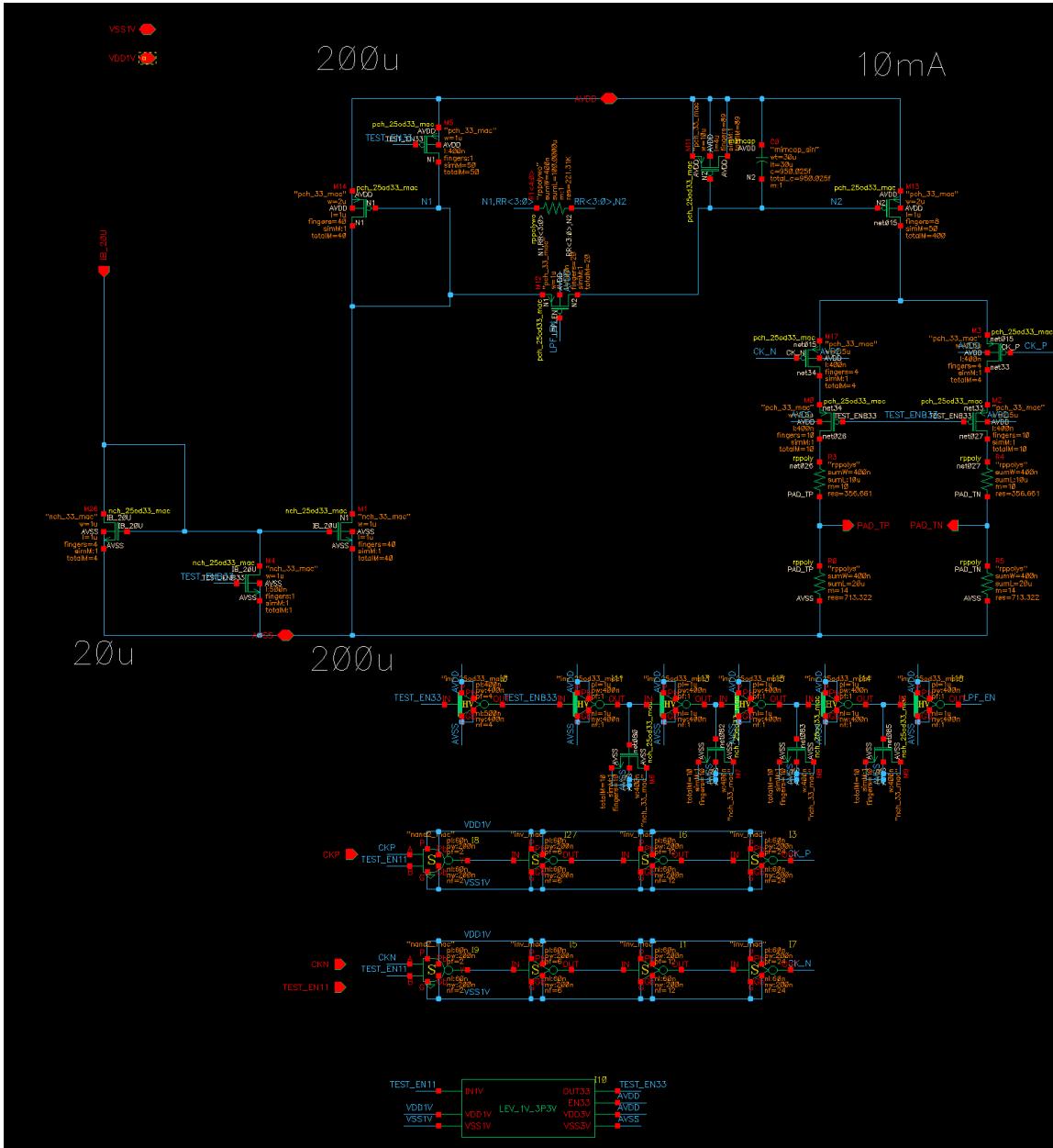


# *Appendix: 2/3 dual modulus Divider*

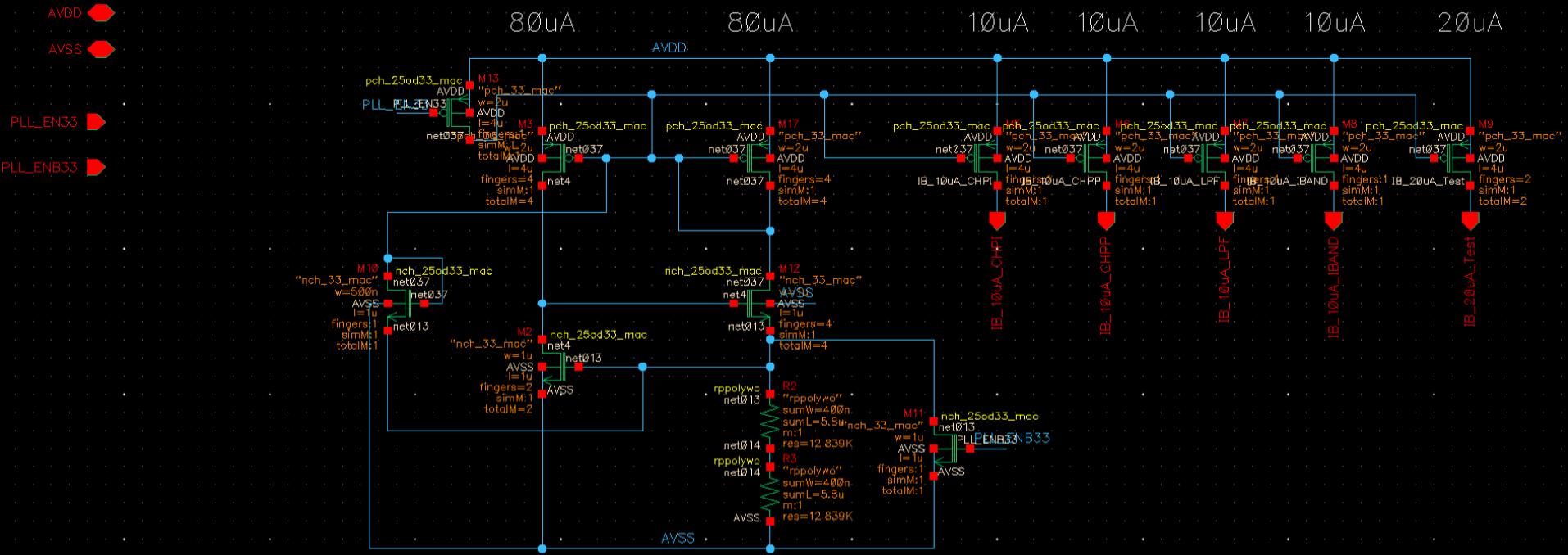
# Appendix: Post\_DIV



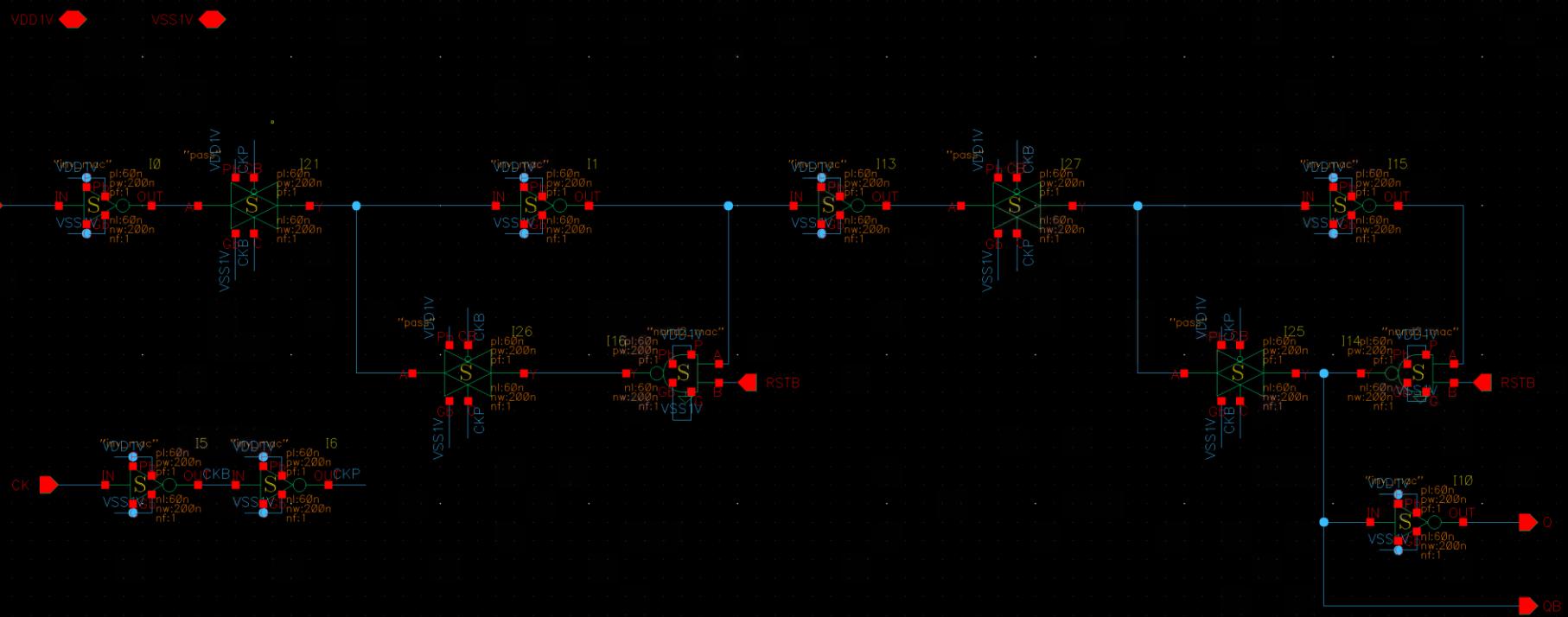
# Appendix: Test circuit\_CML



# Appendix: Self-Bias\_VGS/R



# Appendix: DFF



# Appendix: ESD

ESD: Diode + Clamp circuit

