EE230-02 RFIC II
Fall 2018

Lecture 19: Frequency Synthesizers

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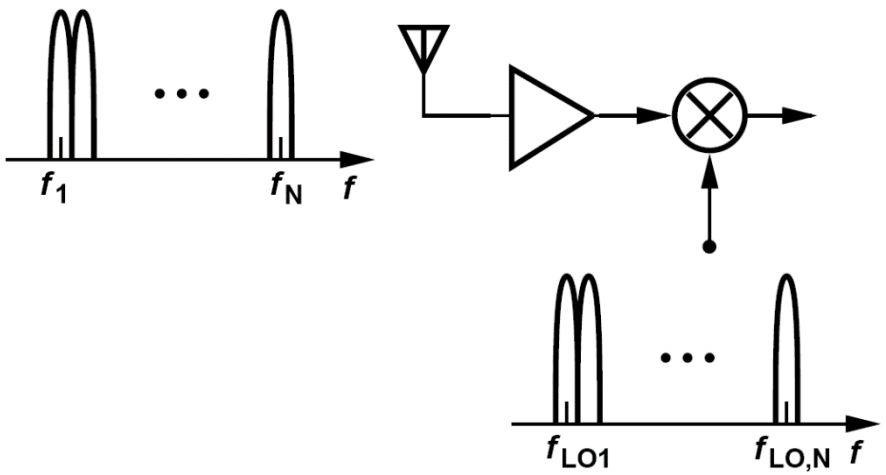
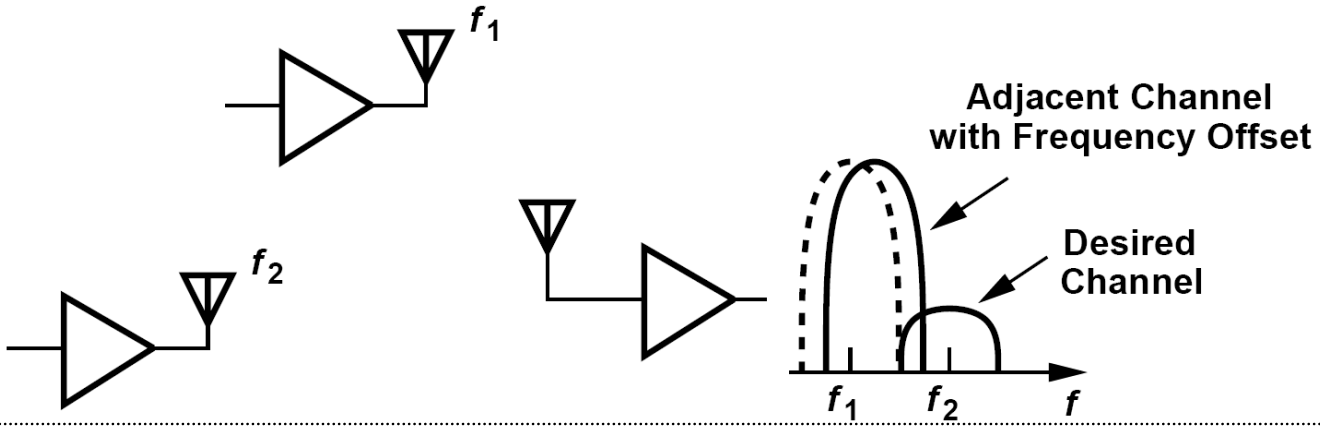
ENG-259

General Consideration of Frequency Synthesizer



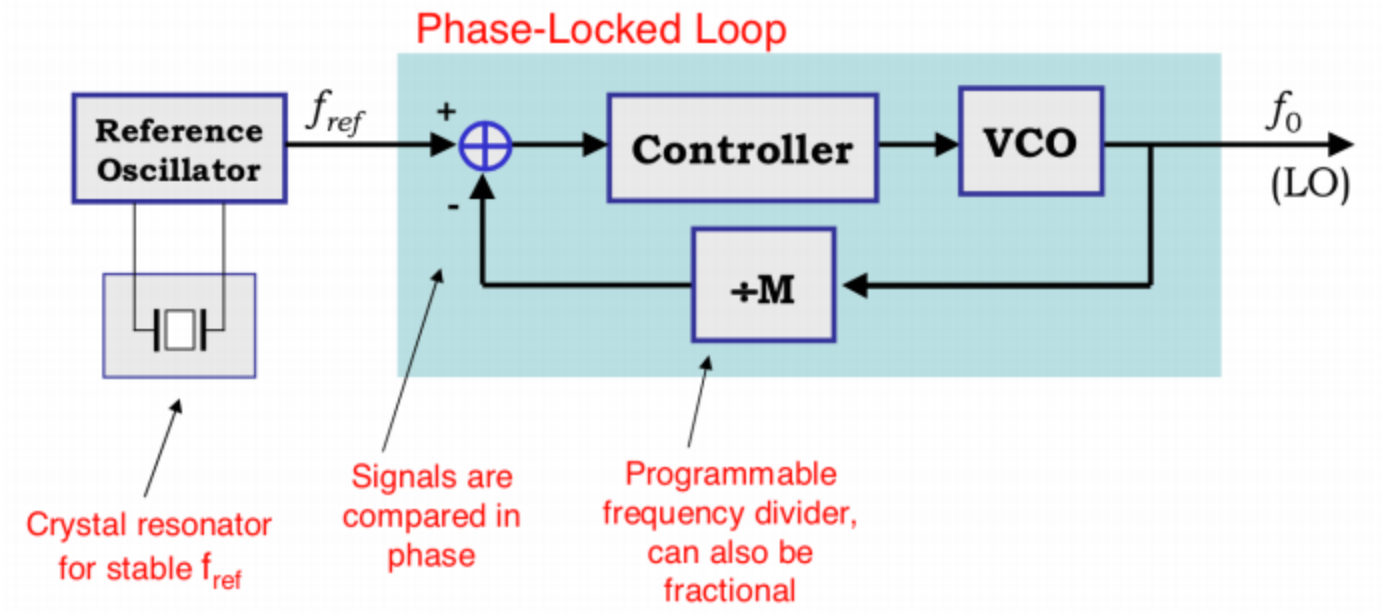
- The synthesizer performs the precise setting of LO frequency



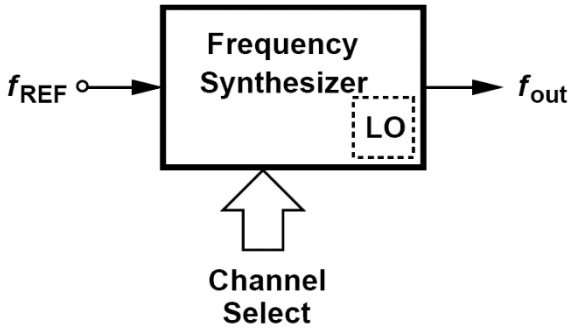
- A slight shift leads to significant spillage of a high-power interferer in to a desired channel

Integer-N Synthesizer

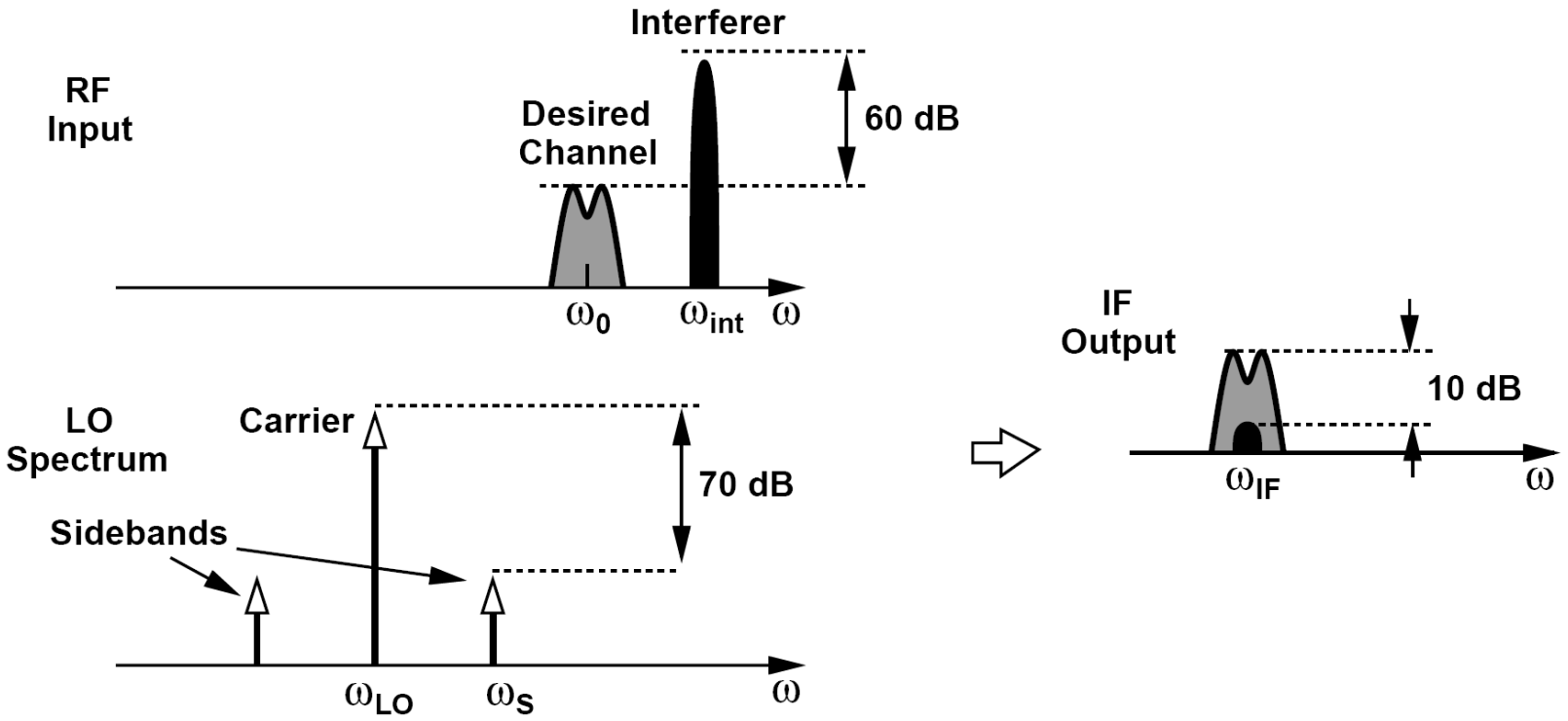
- Integer-N synthesizers: output frequency is an integer multiple of the reference frequency.
- If N increases by 1, then f_o increases by f_{REF} => the minimum channel spacing is equal to the reference frequency.



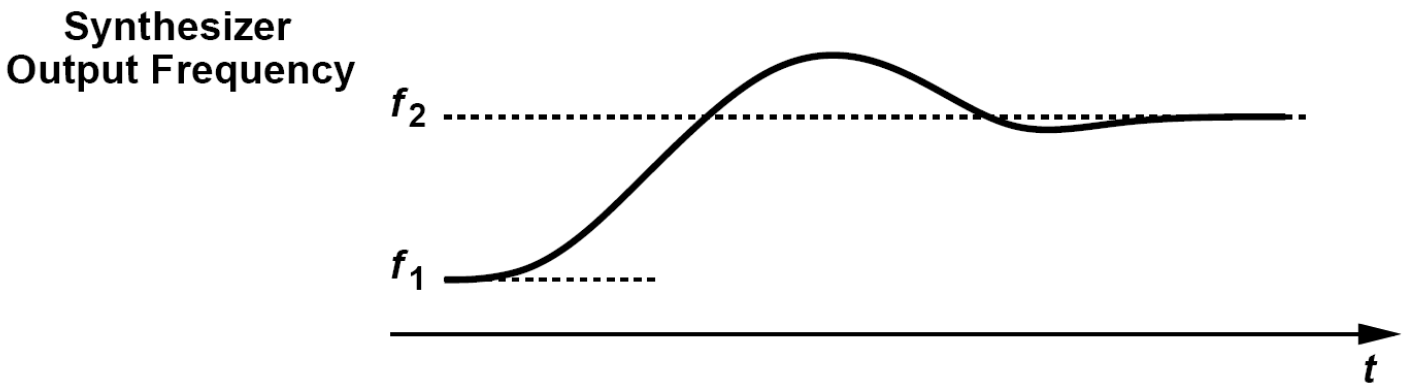
Reciprocal Mixing



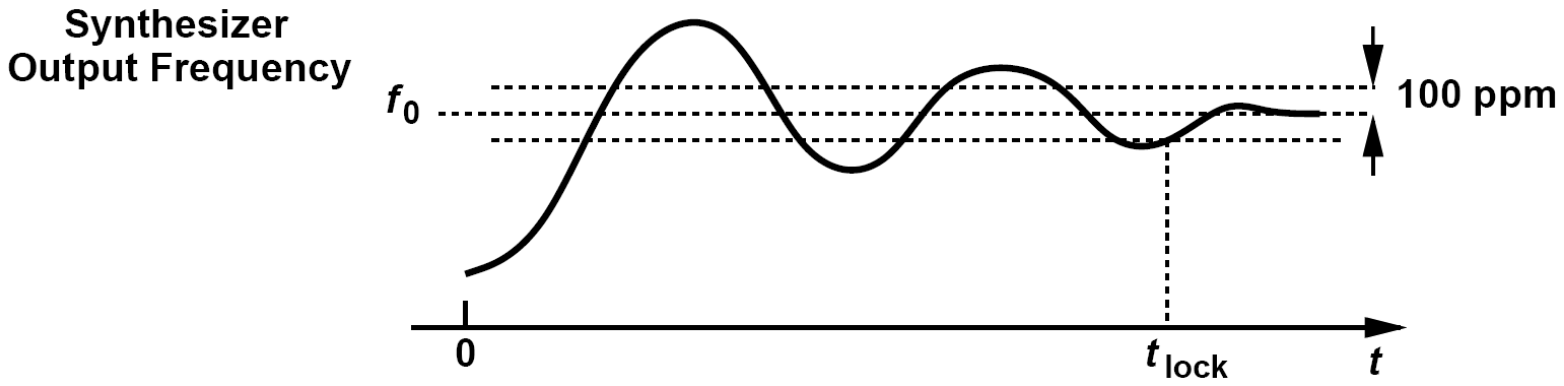
- The output frequency is generated as a multiple of a precise reference.
- Sidebands: upon downconversion mixing, the desired channel is convolved with the carrier and the interferer with the sideband



Lock Time

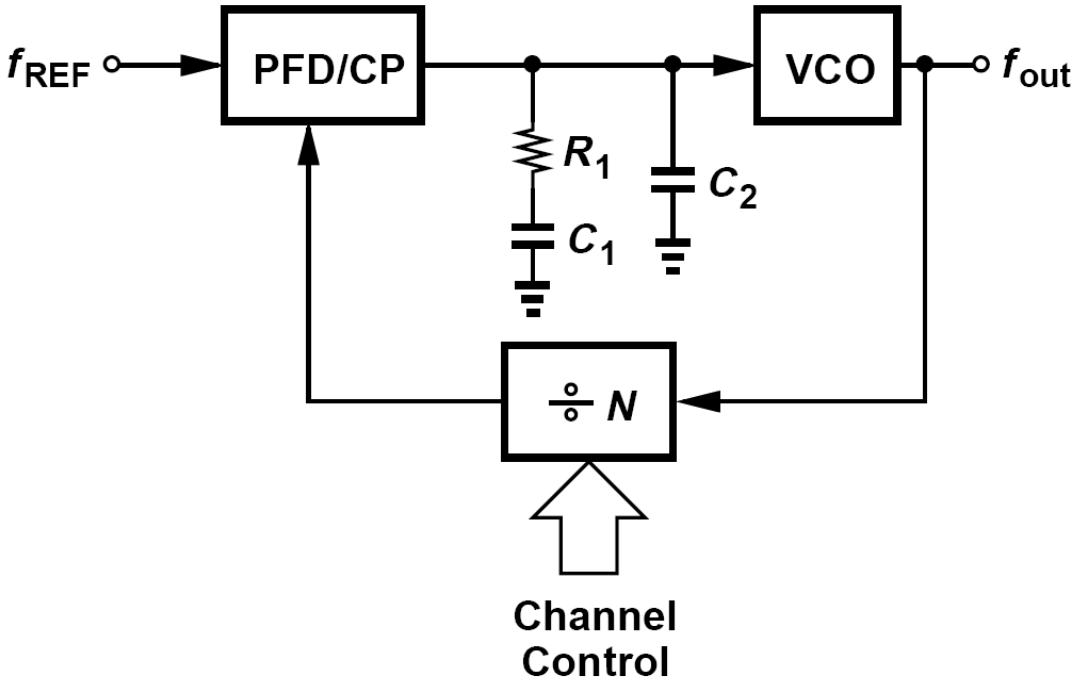


- Lock time directly subtracts from the time available for communication



- The lock time is typically specified as the time required for the output frequency to reach within a certain margin around its final value

Basic Integer-N Synthesizer



- Integer-*N* synthesizer produces an output frequency that is an integer multiple of the reference frequency.
- The choice of f_{REF}: it must be equal to the desired channel spacing and it must be the greatest common divisor of f_1 and f_2.

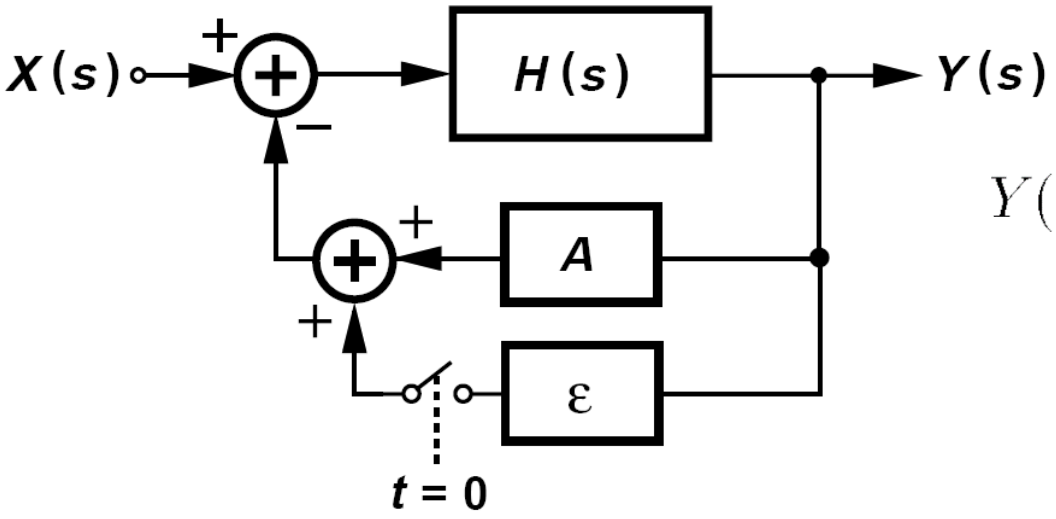
Reference Frequency and Divide Ratio

What is the required reference frequency and range of divide ratios for an integer-*N* synthesizer designed for a Direct Conversion Bluetooth receiver?

The LO range extends from the center of the first channel, 2400.5 MHz, to that of the last, 2479.5 MHz.

Thus, even though the channel spacing is 1 MHz, f_{REF} must be chosen equal to 500 kHz. Consequently, N_1 = 4801 and N_2 = 4959.

Settling Behavior: Channel Switching



$$Y(s) = \frac{H(s)}{1+(A+\epsilon)H(s)}X(s)$$

$$\approx \frac{H(s)}{1+AH(s)} \cdot \frac{1}{1+\epsilon/A}X(s)$$

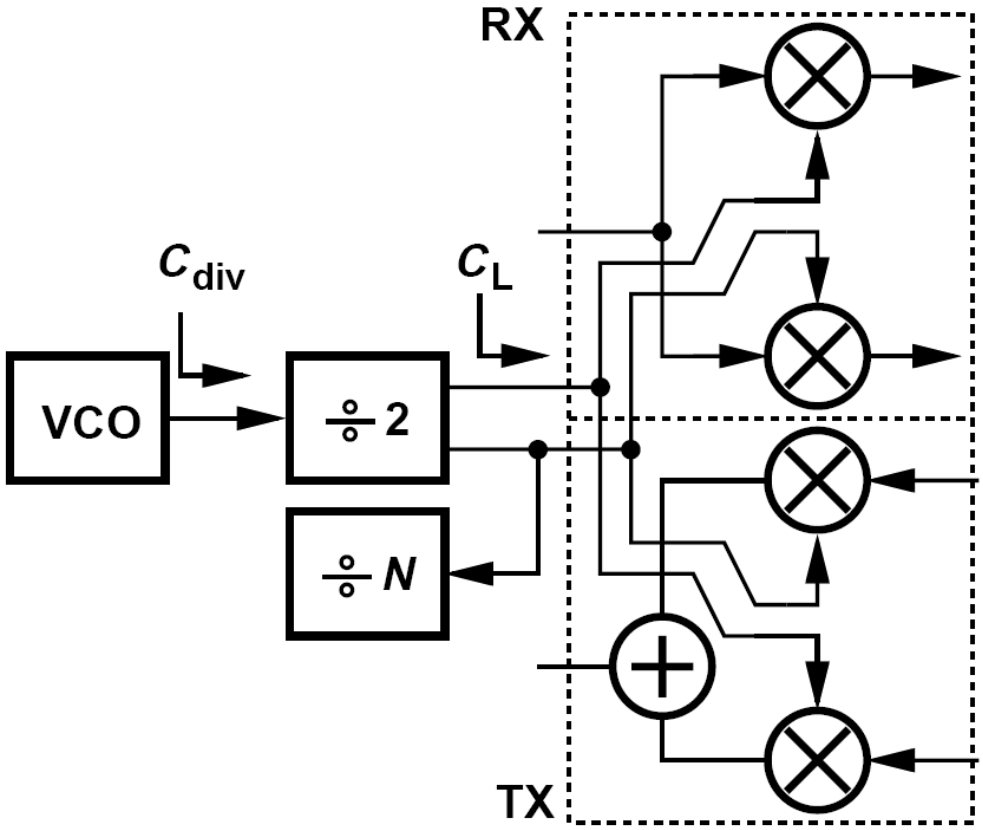
$$\approx \frac{H(s)}{1+AH(s)}\left(1-\frac{\epsilon}{A}\right)X(s)$$

We can view multiplication by (1 –ε/A) as a step function from f_0 to $f_0(1 - \varepsilon/A)$, i.e., a frequency jump of $-(\varepsilon/A)f_0$.

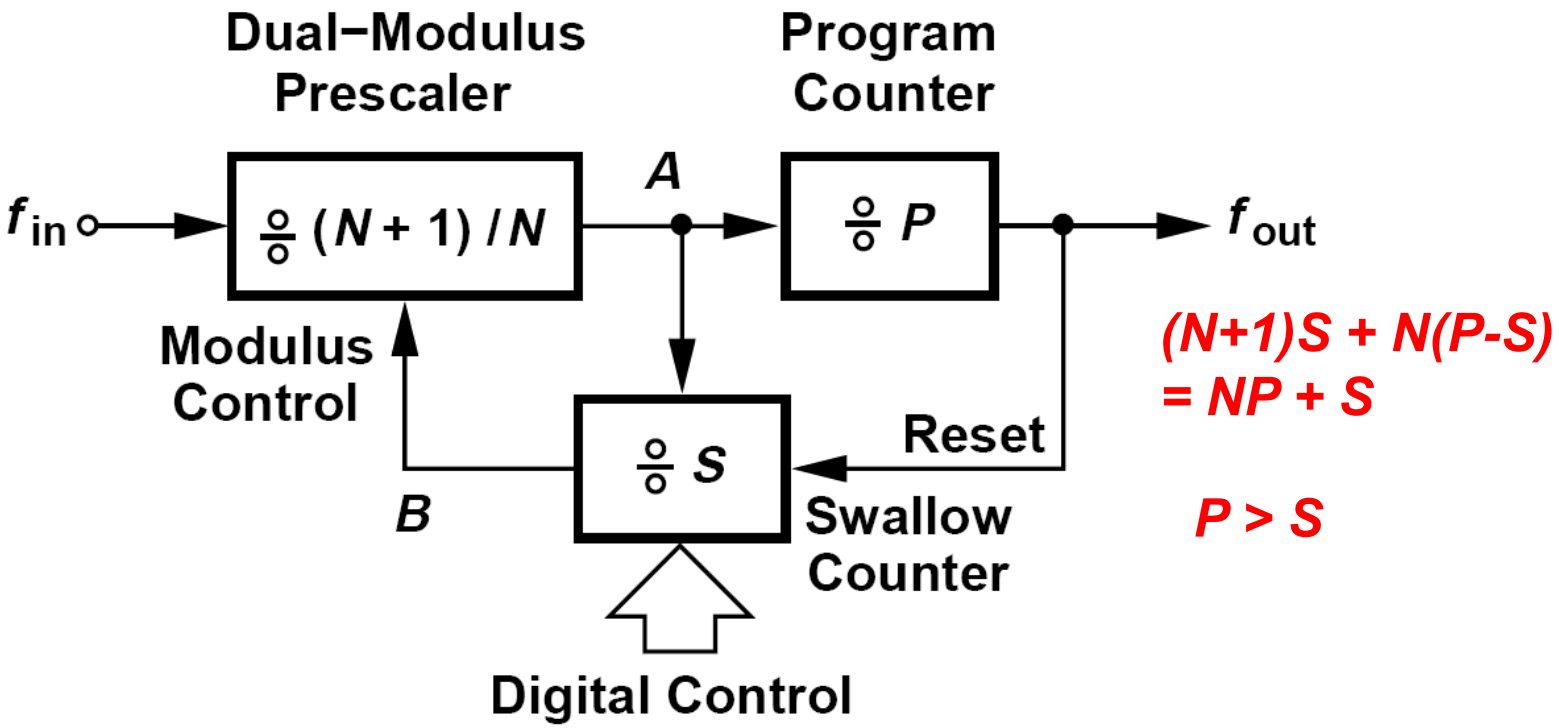
- **When the divide ratio changes, the loop responds as if an input frequency step were applied**

Divider Design: Requirements

- The divider modulus, *N*, must change in unity steps
- The first stage of the divider must operates as fast as the VCO
- VCO must drive the divider input capacitance
- The divider must consume low power, preferably less than the VCO



Pulse Swallow Divider

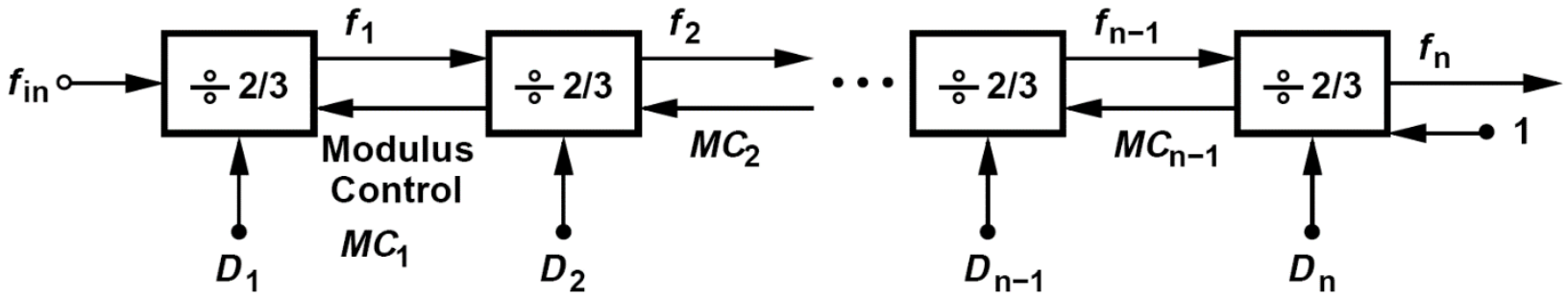


- Sensing the high-frequency input, the Prescaler proves the most challenging of the three building blocks.

Modular Divider Realizing Multiple Divider Ratios

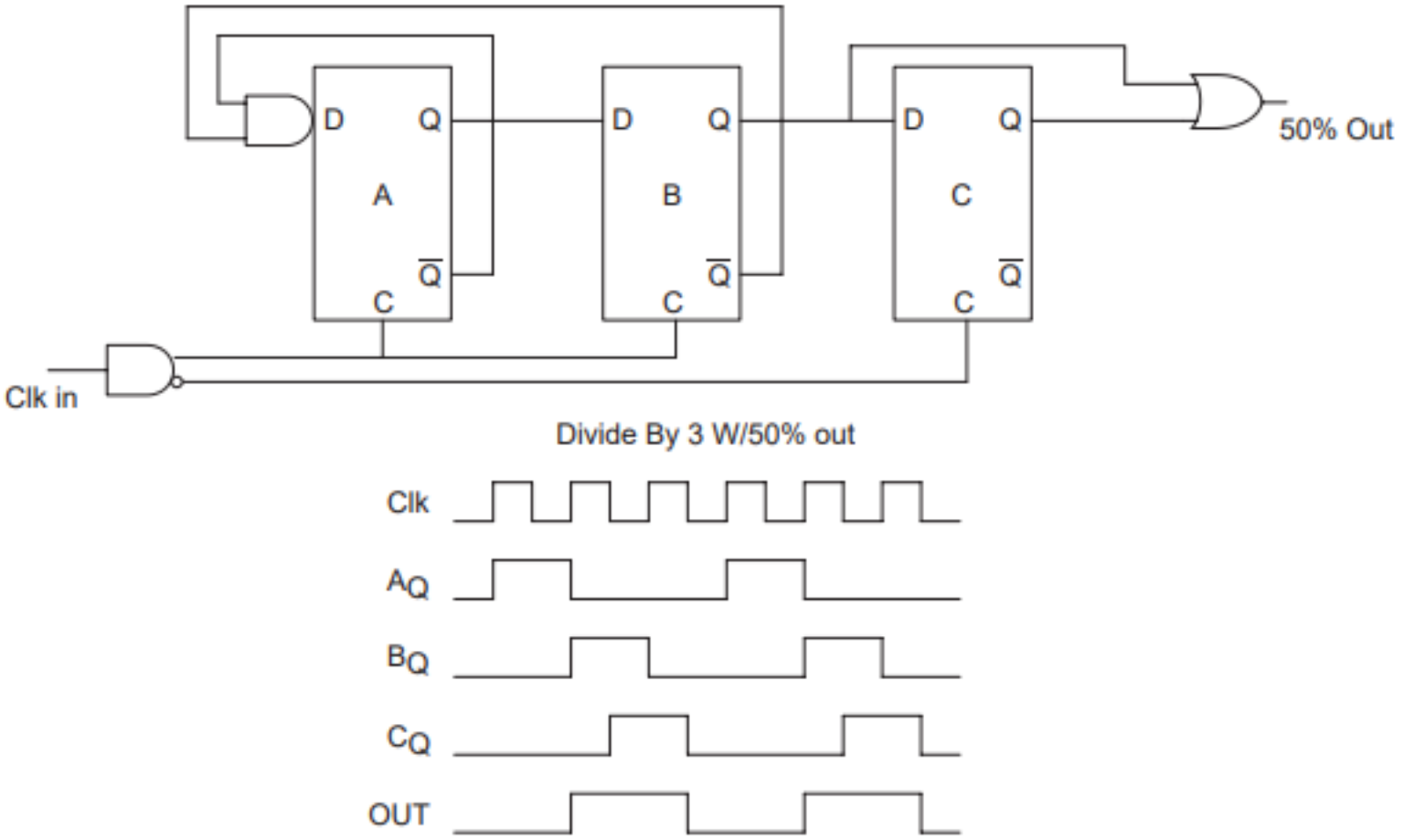
- Use ÷2/3 stages in a modular form so as to reduce the design complexity.
- Each ÷2/3 block receives a modulus control from the next stage.
- The digital inputs set the overall divide ratio according to:

$$N = 2^n + D_n 2^{n-1} + D_{n-1} 2^{n-2} + \cdots + 2D_2 + D_1$$

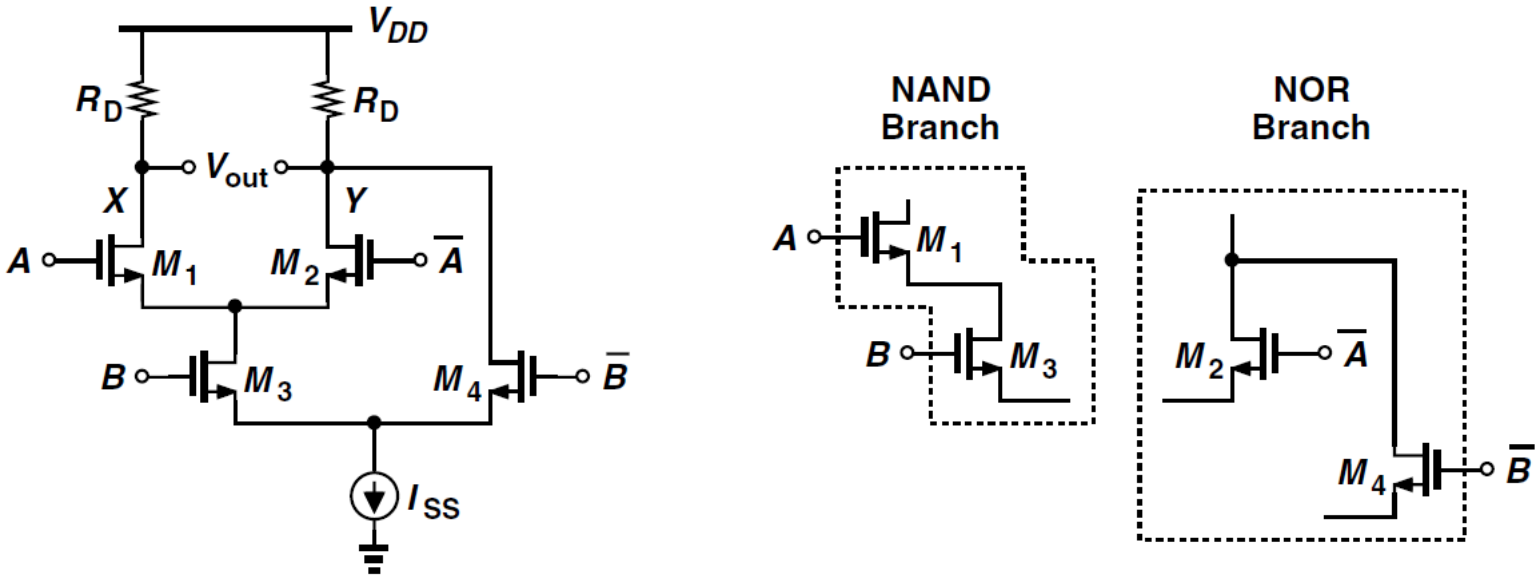


C. S. Vaucher et al., "A Family of Low-Power Truly Modular Programmable Dividers in Standard 0.35-µm CMOS Technology," IEEE J. of Solid-State Circuits, vol. 35, pp. 1039–1045, July 2000.

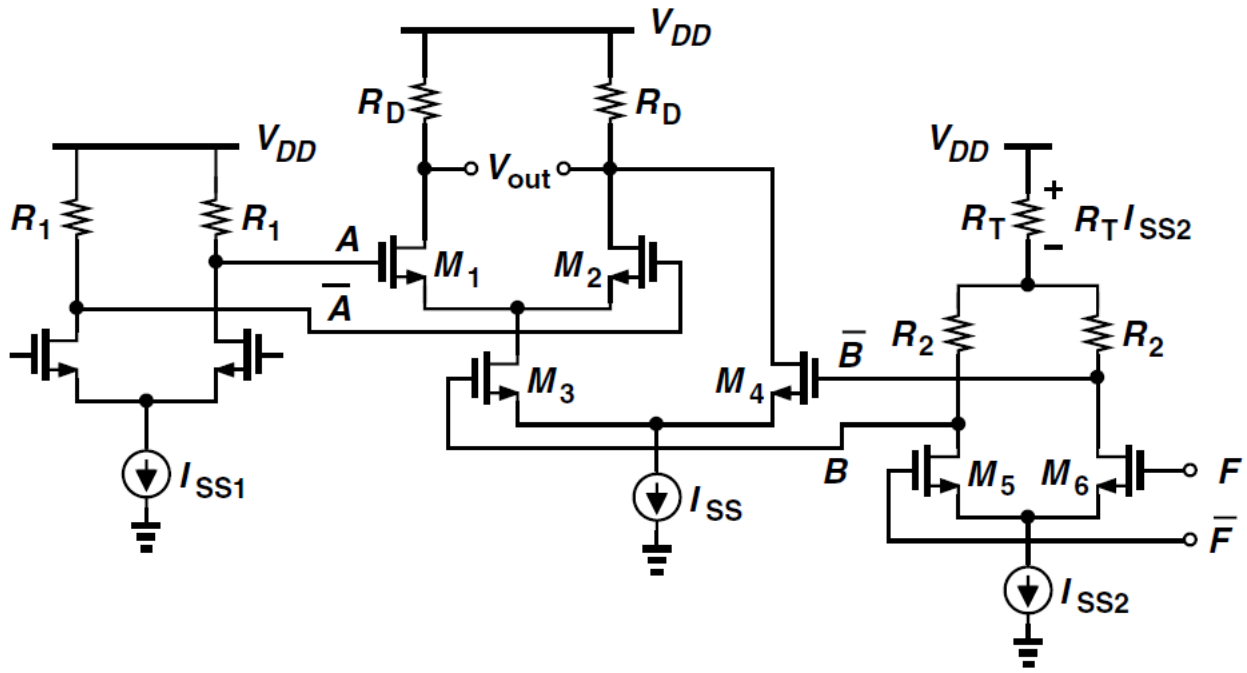
Divide by 3


D
Q
A
Q
C
D
Q
B
Q
C
D
Q
C
Q
C
50% Out
Clk in
Divide By 3 W/50% out
Clk
AQ
BQ
CQ
OUT

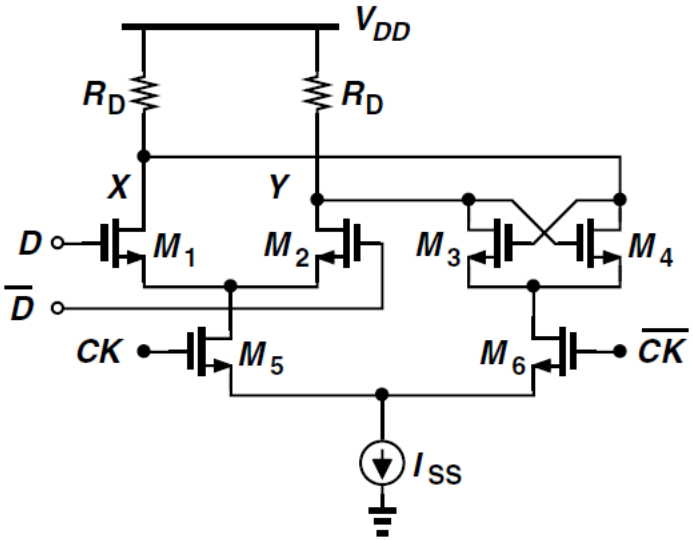
CML Circuit

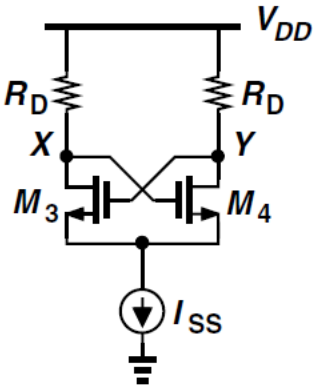

V_{DD}
R_D
R_D
V_{out}
X
Y
A
M_1
M_2
$\overline{A}$
B
M_3
M_4
$\overline{B}$
I_{SS}
NAND Branch
A
M_1
B
M_3
NOR Branch
M_2
$\overline{A}$
M_4
$\overline{B}$

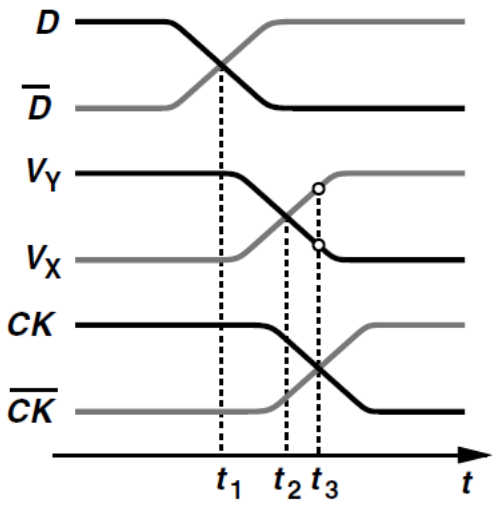
CML Circuit


V_{DD}
R_D
R_D
V_{DD}
V_{out}
V_{DD}
R_1
R_1
A
M_1
M_2
$\overline{A}$
R_T
$R_T I_{SS2}$
R_2
R_2
$\overline{B}$
M_3
M_4
B
M_5
M_6
F
$\overline{F}$
I_{SS1}
I_{SS}
I_{SS2}

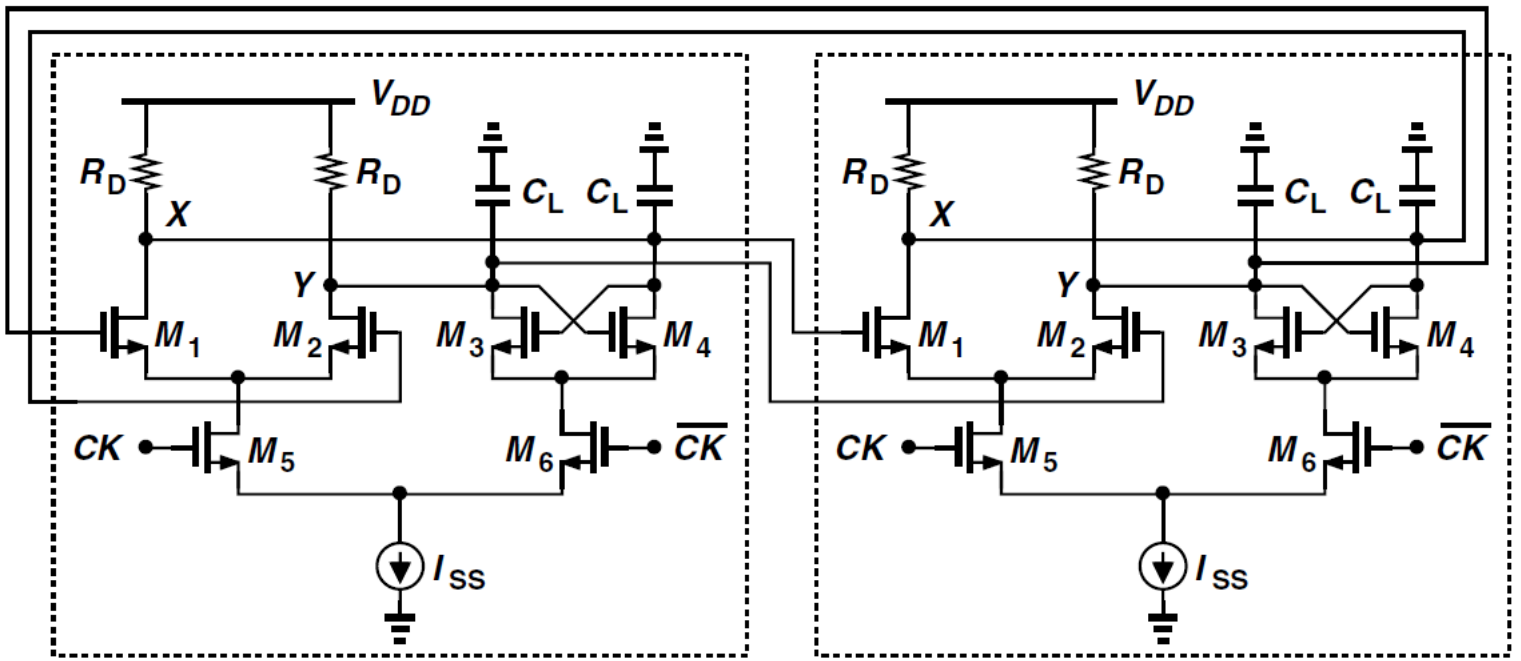
CML Latch


V_{DD}
R_D
R_D
X
Y
D
M_1
M_2
M_3
M_4
$\overline{D}$
CK
M_5
M_6
$\overline{CK}$
I_{SS}

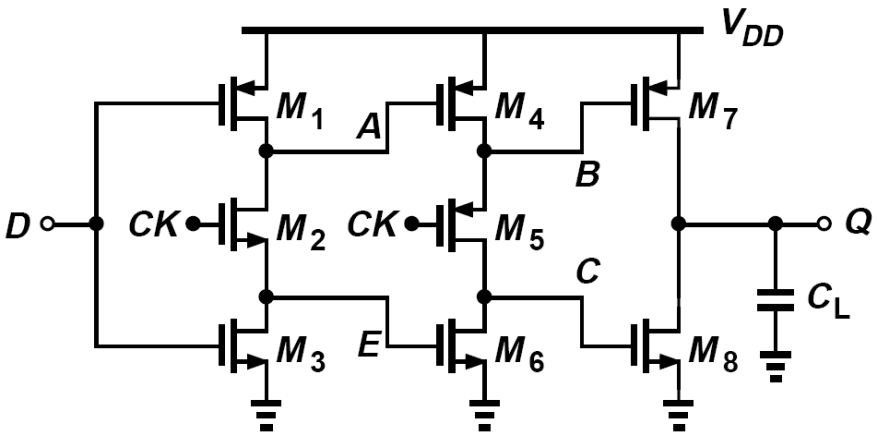

V_{DD}
R_D
R_D
X
Y
M_3
M_4
I_{SS}

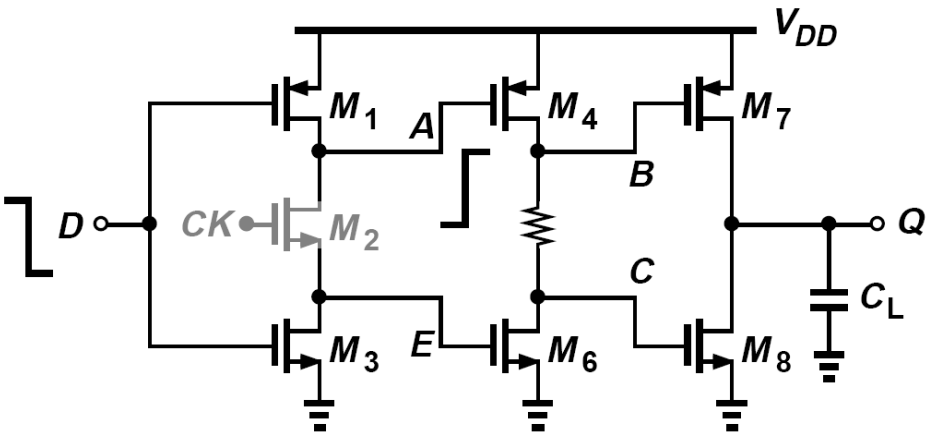

D
$\overline{D}$
V_Y
V_X
CK
$\overline{CK}$
t_1
t_2
t_3
t

CML Divide by 2



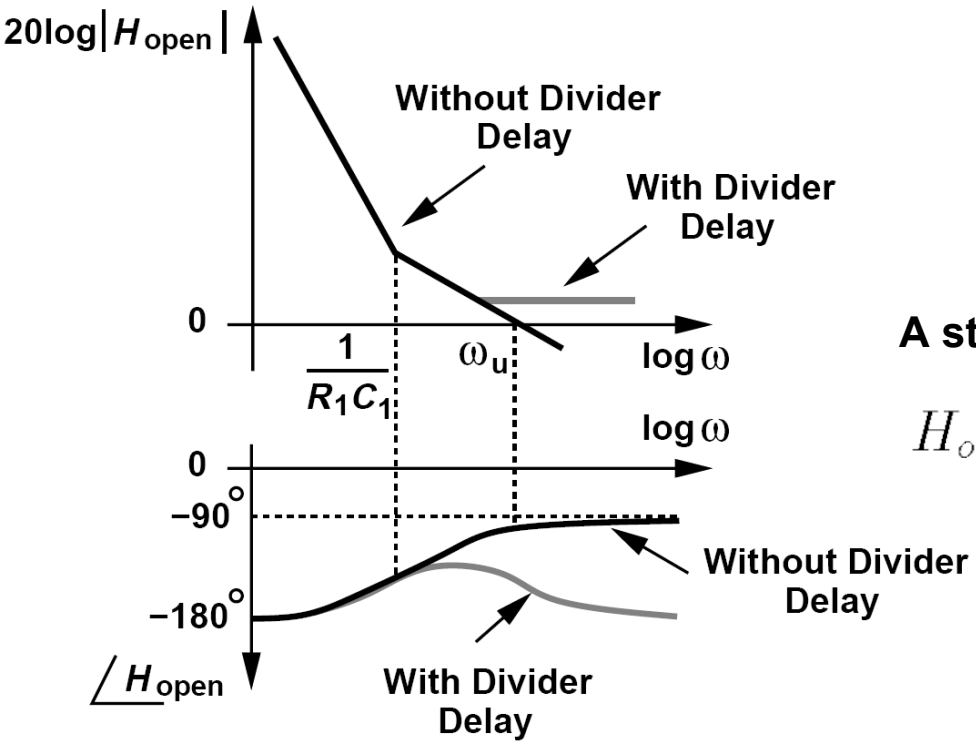
True Single Phase Clocking





- When *CK* is high, the first stage operates as an inverter, impressing $\overline{D}$ at *A* and *E*. When *CK* goes low, the first stage is disabled and the second stage becomes transparent, writing $\overline{A}$ at *B* and *C* and hence making *Q* equal to *A*. The logical high at *E* and the logical low at *B* are degraded but the levels at *A* and *C* ensure proper operation of the circuit.

Divider Delay and Phase Noise: Effect of Divider Delay



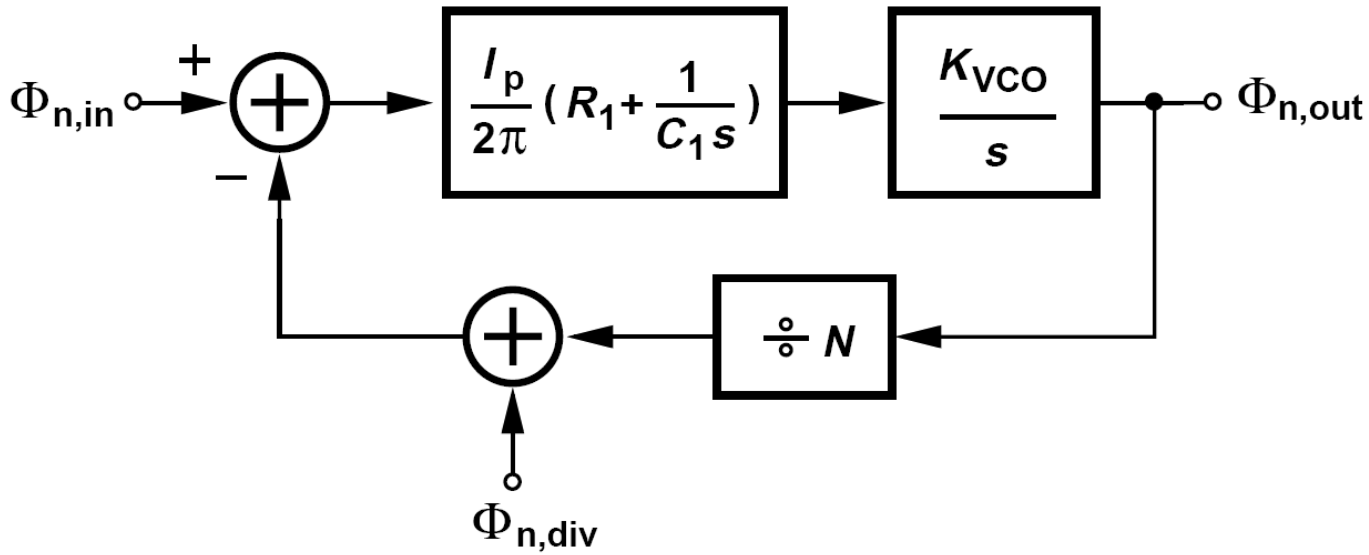
A stage with a constant delay of ΔT

$$H_{open}(s) = \frac{I_P}{2\pi}\left(R_P + \frac{1}{C_1 s}\right)\frac{K_{VCO}}{NS}e^{-\Delta T \cdot s}.$$

- **The zero has two undesirable effects: it flattens the gain, pushing the gain crossover frequency to higher values (in principle, infinity), and it bends the phase profile downward.**

This zero must remain well above the original unity-gain bandwidth of the loop:

Effect of Divider Phase Noise



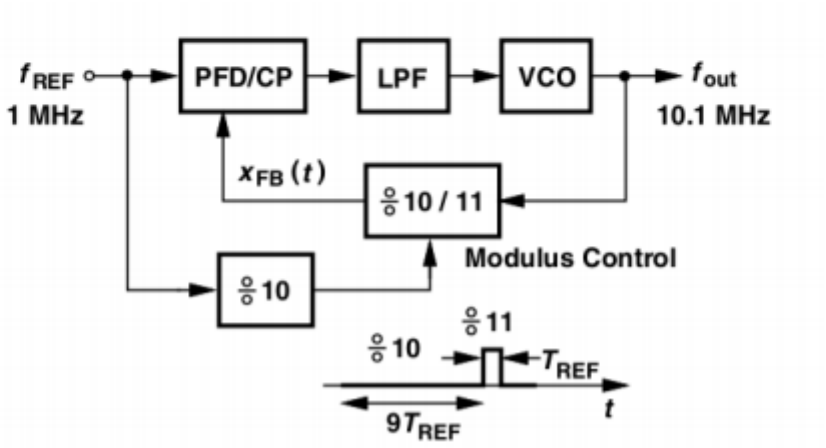
- The output phase noise of the divider directly adds to the input phase noise, experiencing the same low-pass response as it propagates to ϕ_{out}. In other words, $\phi_{n,div}$ is also multiplied by a factor of N within the loop bandwidth.

For the divider to contribute negligible phase noise, we must have

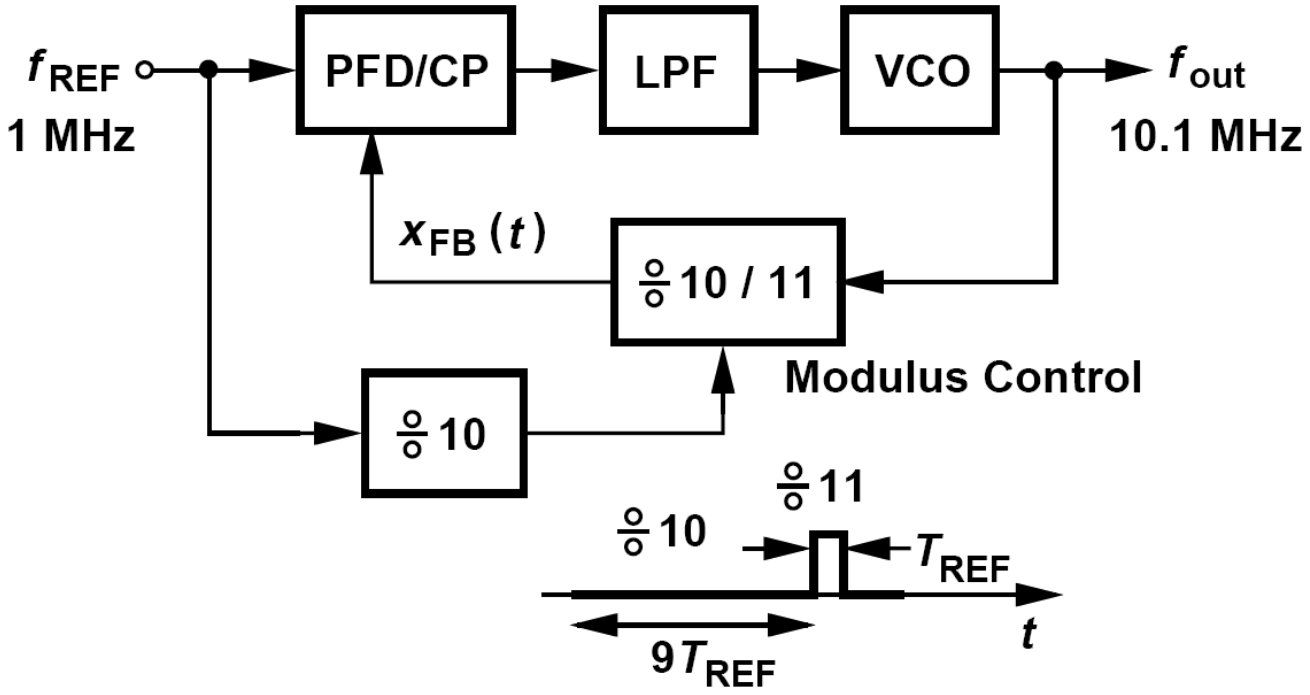
$$\phi_{n,div} \ll \phi_{n,in}$$

Fractional-N Synthesizer

- What happens if the divider divides by N for half of the time and by N+1 for the other half?
- The "average" modulus of the divider is now equal to [N + (N +1)]/2 = N + 0.5.
- If the PLL below divides by 10, 90% of the time, and 11, 10% of the time, f_{out} = 10.1 MHz.
- Arbitrary frequency steps can be provided with a fractional-n synthesizer!

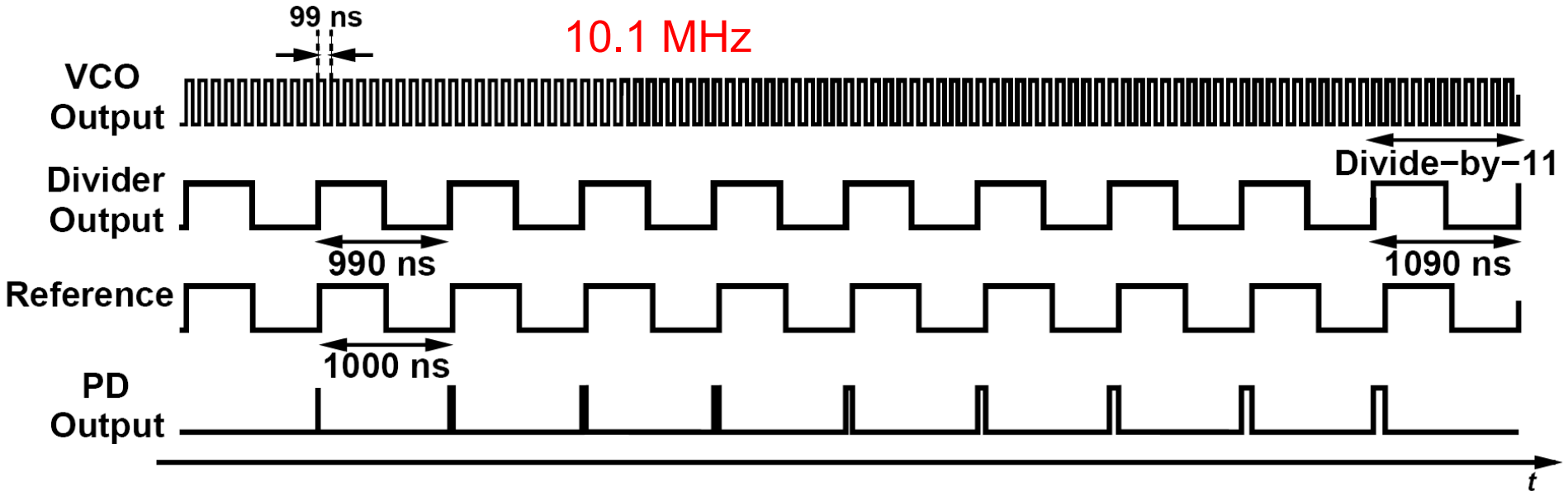


Basic Concepts: Example of Fractional-N Loop



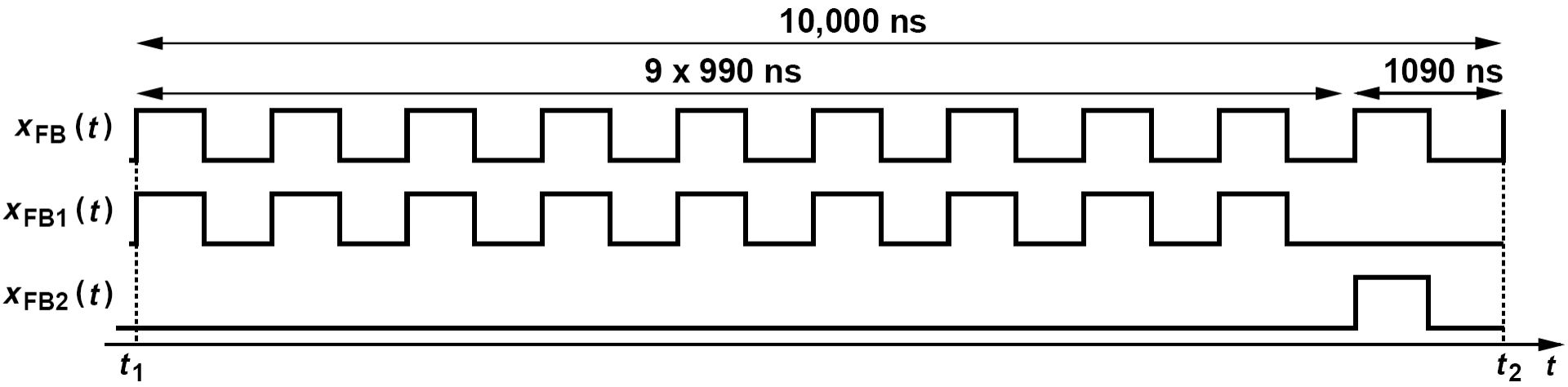
- **We expect to obtain other fractional ratios between *N* and *N+1* by simply changing the percentage of the time during which the divider divides by *N* or *N+1***

Fraction Spurs



- In above example, VCO is modulated at a rate of 0.1MHz and producing sidebands at ±0.1MHz×*n* around 10.1MHz, where n denotes the harmonic number. These sidebands are called *fractional spurs*.
- For a nominal output frequency of $(N+\alpha)f_{REF}$, the LPF output exhibits a repetitive waveform with a period of $1/(\alpha f_{REF})$

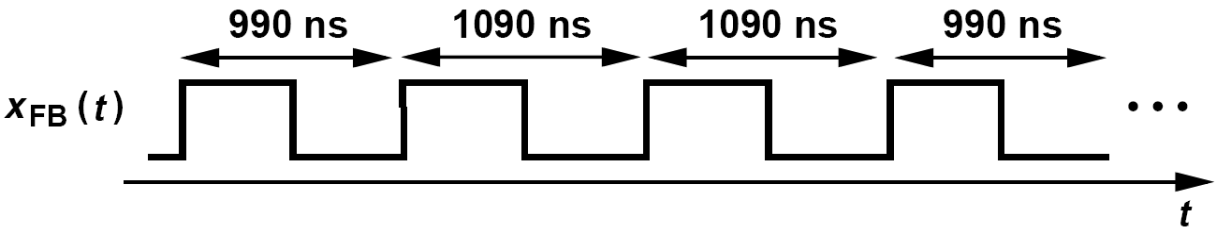
Fraction Spurs: Another Perspective

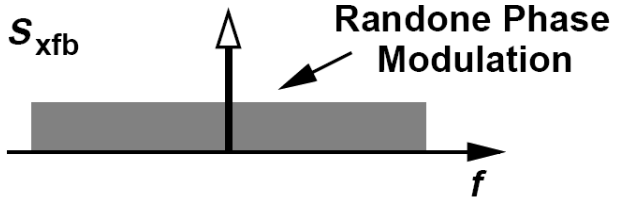


- The overall feedback signal, $x_{FB}(t)$ can be written as the sum of two waveforms, each of which repeat every 10,000 ns. The first waveform consists of nine periods of 990 ns and a "dead" time of 1090 ns, while the second is simply a pulse of width 1090/2 ns. Since each waveform repeats every 10,000 ns, its Fourier series consists of only harmonics at 0.1 MHz, 0.2 MHz, etc.
- The sidebands can be considered FM (and AM) components, leading to periodic phase modulation:

$$x_{FB}(t) \approx A\cos[\omega_{REF}t + \phi(t)]$$

Randomization and Noise Shaping: Modulus Randomization





$x_{FB}(t)$ exhibits a random sequence of 990-ns and 1090-ns periods

$x_{FB}(t)$ now contains random phase modulation:

$$x_{FB}(t) = A\cos[\omega_{REF}t + \phi_n(t)]$$

The modulus breaks the periodicity in the loop behavior, converting the deterministic sidebands to *noise*

The instantaneous frequency of the feedback signal is therefore expressed as:

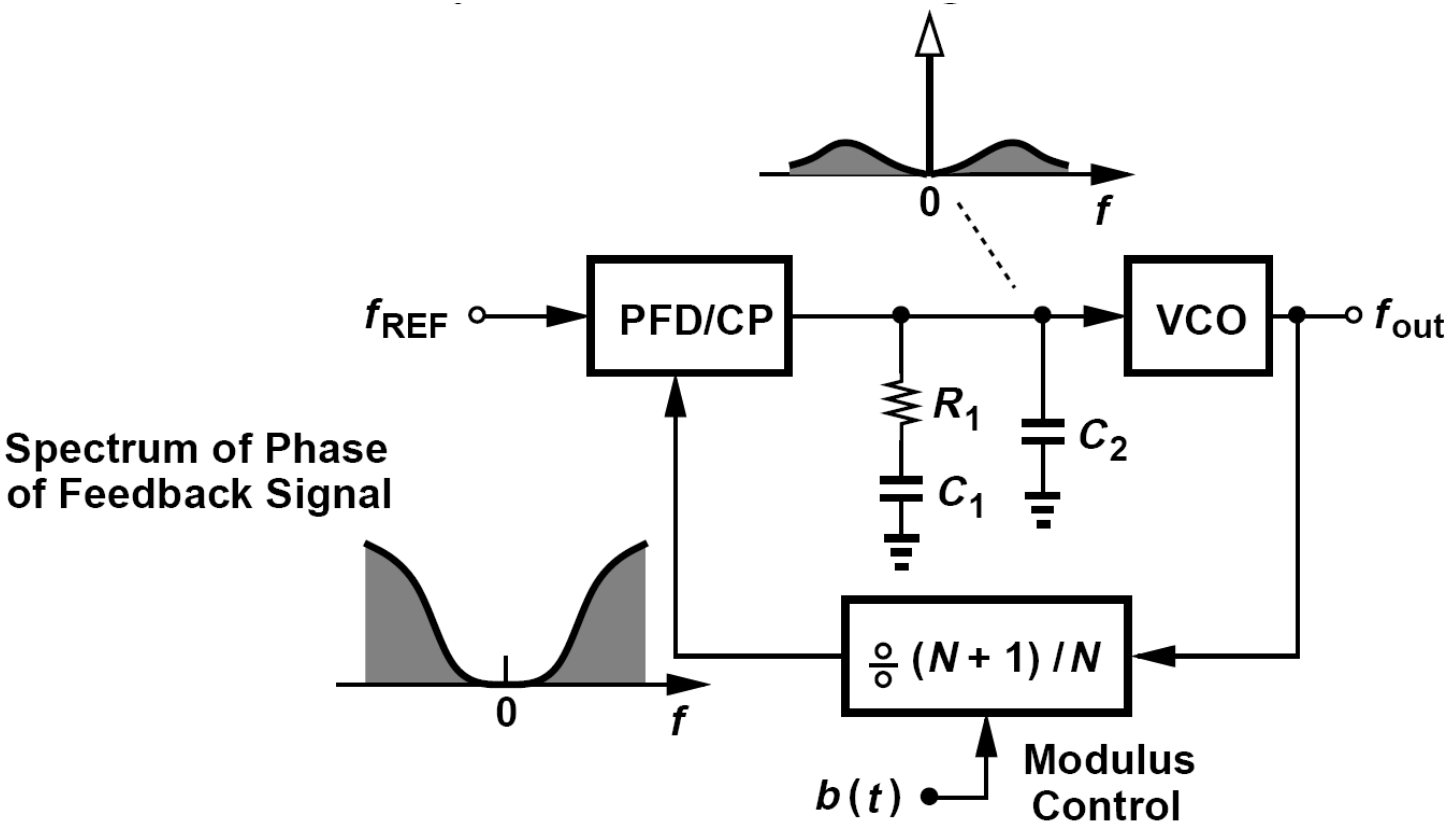
$$f_{FB}(t) = \frac{f_{out}}{N + b(t)}$$

where b(t) randomly assumes a value of 0 or 1 and has an average value of α

In terms of its mean and another random variable with a zero mean:

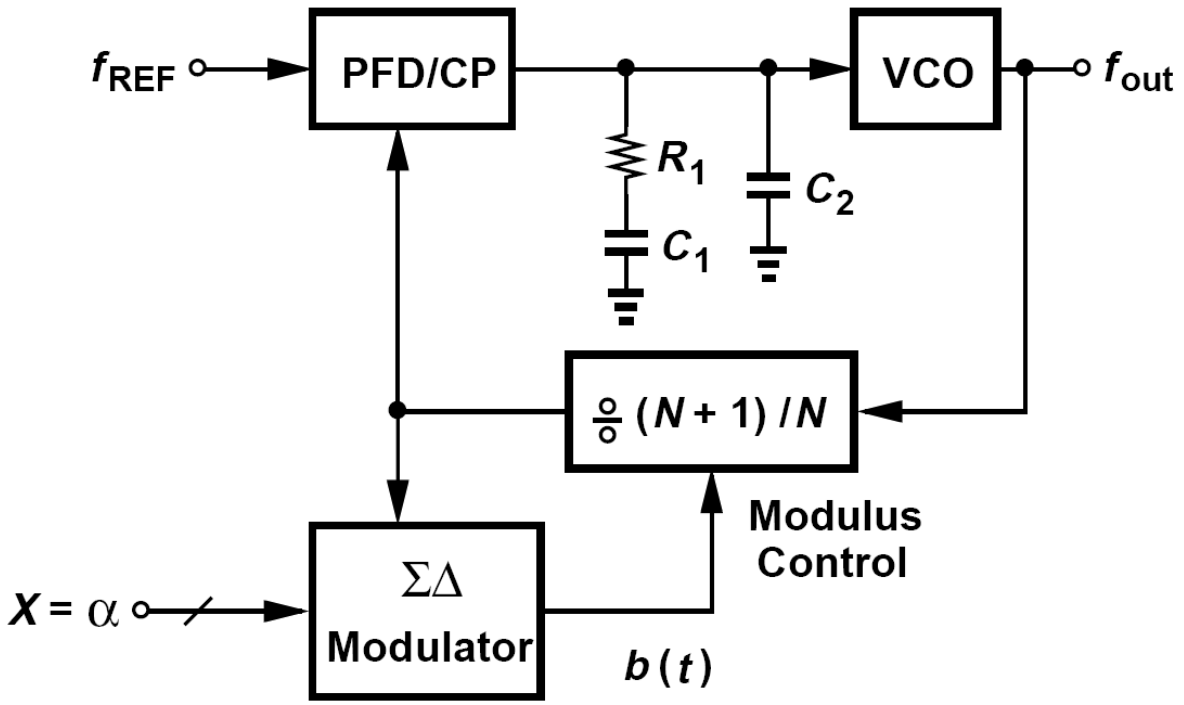
$$b(t) = \alpha + q(t)$$

Basic Noise Shaping: Randomization Resulting in High-Pass Phase Noise Spectrum



- We wish to generate a random binary sequence, *b(t)*, that switches the divider modulus between *N* and *N+1* such that (1) the average value of the sequence is *α*, and (2) the noise of the sequence exhibits a high-pass spectrum.

Summary: Fractional-N Synthesizer Developed Thus Far



- Shown above is a basic fractional-*N* loop using a Σ-Δ modulator to randomize the divide ratio.
- Clocked by the feedback signal, the Σ-Δ modulator toggles the divide ratio between *N* and *N+1* so that the average is equal to *N+α*