EE230-02 RFIC II
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Lecture 16: Phase-Locked Loops

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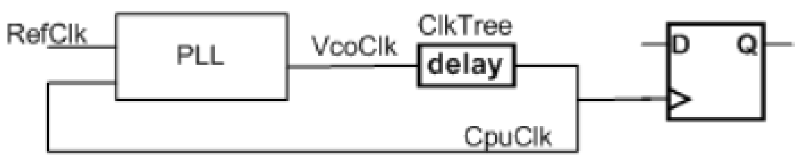
How Are PLL's used?

- Frequency Synthesis (e.g. generating a 1 GHz clock from a 100 MHz reference in a CPU)

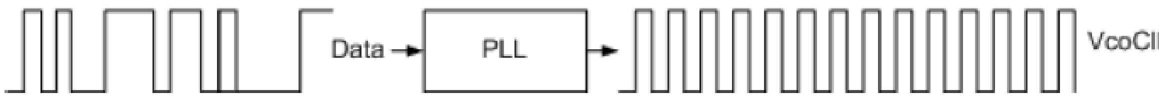
- Skew Cancellation (e.g. phase-aligning an internal clock to the I/O clock) (May use a DLL instead)



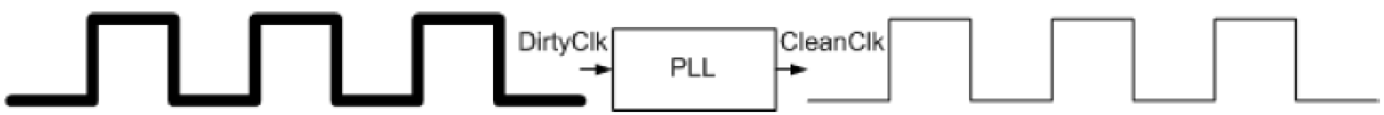
How Are PLL's used?

Serdes

- Extracting a clock from a random data stream (e.g. serial-link clock-data recovery)



- Reference Clean-Up (e.g. low-pass filter source-synchronous clock in high-speed I/O)



Has many HFC & LPF will clean it

What is a PLL?

- Negative feedback control system where f_{out} tracks f_{in} and rising edges of input clock align to rising edges of output clock
- Mathematical model of frequency synthesizer

$$V_{in}(t) \propto \sin\left(\overbrace{2\pi f_{in} t}^{\phi_{in}}\right) \longrightarrow \boxed{\text{Phase-Locked Loop}} \longrightarrow V_{out}(t) \propto \sin\left(\overbrace{2\pi N f_{in} t}^{\phi_{out}}\right)$$

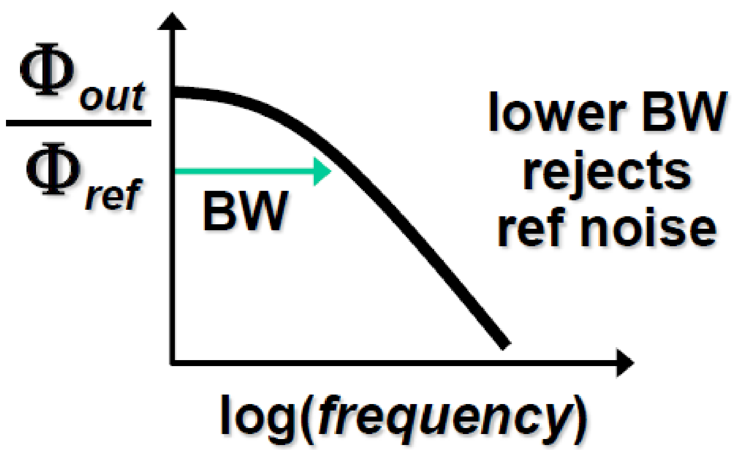
- **Phase = ∫ frequency**

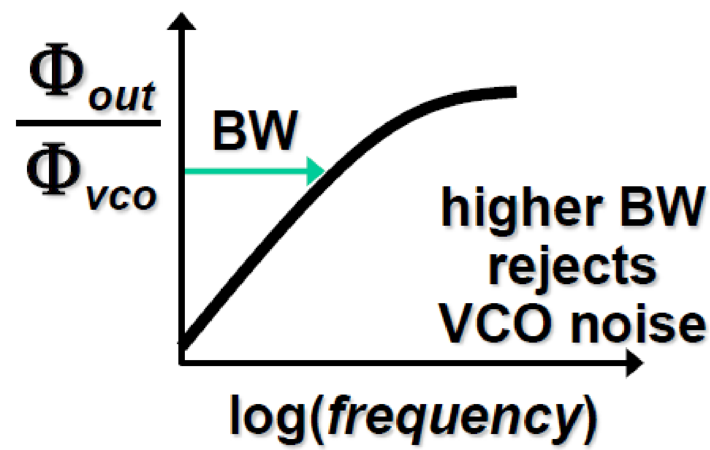
$$\phi(t) = 2\pi \int f(t)\, dt \;\leftrightarrow\; f(t) = \frac{1}{2\pi}\frac{d\phi(t)}{dt}$$

- **When phase-locked,** $\phi_{out} = N\phi_{in} \rightarrow f_{out} = N f_{in}$

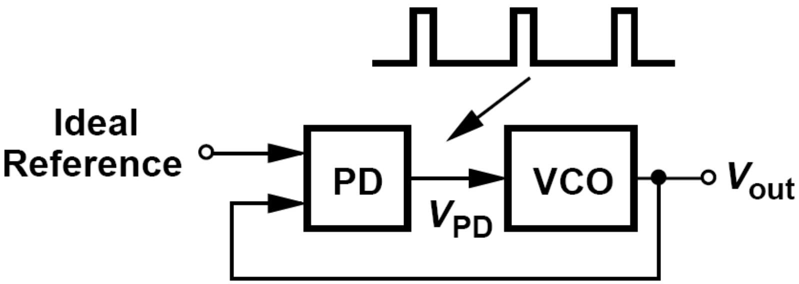
What does PLL Bandwidth means?

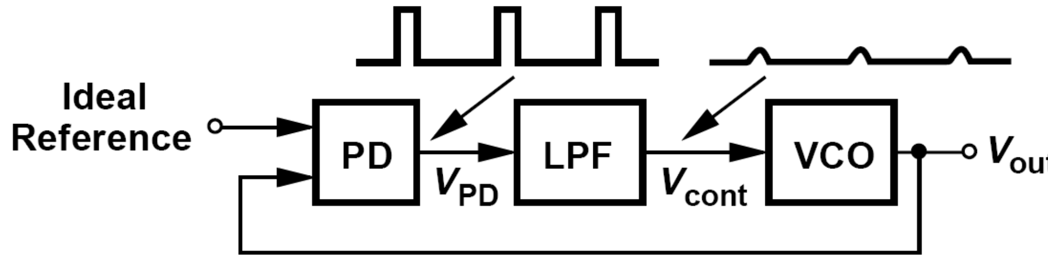
- PLL acts as a low-pass filter with respect to the reference modulation. High-frequency reference jitter is rejected
- Low-frequency reference modulation (e.g., spread-spectrum clocking) is passed to the VCO clock
- PLL acts as a high-pass filter with respect to VCO jitter
- "Bandwidth" is the modulation frequency at which the PLL begins to lose lock with the changing reference (-3dB)





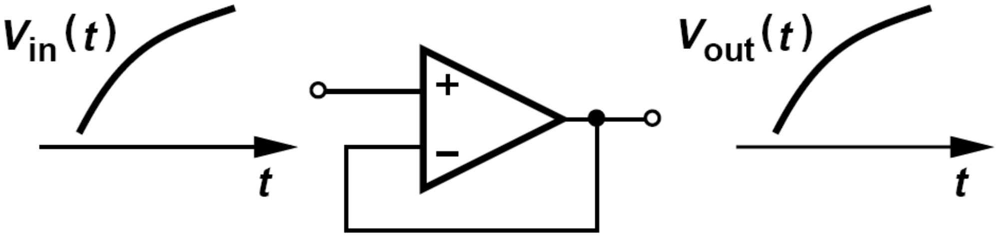
Simple Type-I PLL and Loop Filter

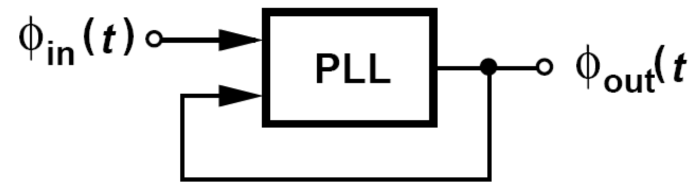




- Negative feedback loop: if the "loop gain" is sufficiently high, the circuit minimizes the input error. phase error but Type I have stability problems
- The PD produces repetitive pulses at its output, modulating the VCO frequency and generating large sidebands.
- Insert a low-pass filter between the PD and the VCO to suppress these pulses. ⟹ Smoth The signals

Simple PLL: Phase Locking





$$\phi_{out}(t) - \phi_{in}(t) = \text{constant}$$

$$\frac{d\phi_{out}}{dt} = \frac{d\phi_{in}}{dt}$$

- Loop is "locked" if $\phi_{out}(t)$-$\phi_{in}(t)$ is constant with time.
- Phase locking makes the input and output frequencies of the PLL exactly equal.

Example of Phase Error

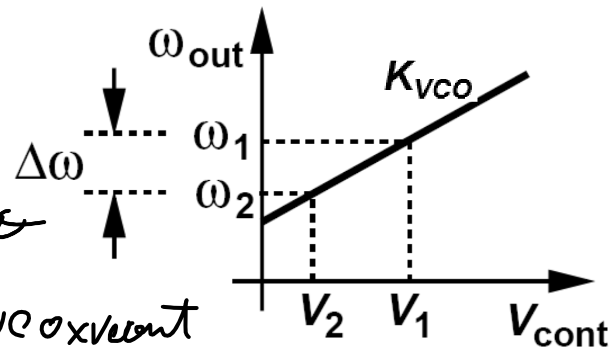
If the input frequency changes by $\Delta\omega$, how much is the change in the phase error? Assume the loop remains locked.

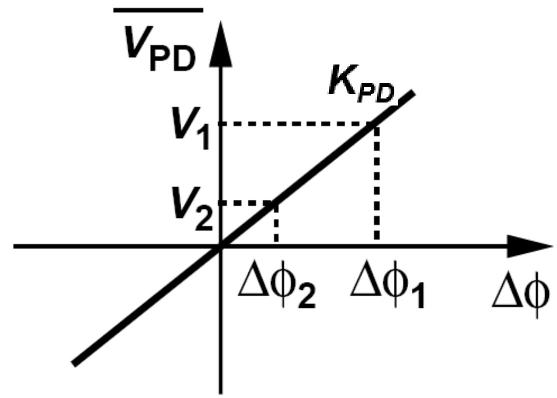
$\Delta\phi = \frac{V_{cont}}{K_{PD}}$

$\Delta\phi = \frac{\Delta\omega}{K_{PD} K_{VCO}}$

$\omega_{out} = \omega_{in} + K_{VCO} \times V_{cont}$

$\Delta\omega = K_{VCO} \times V_{cont}$

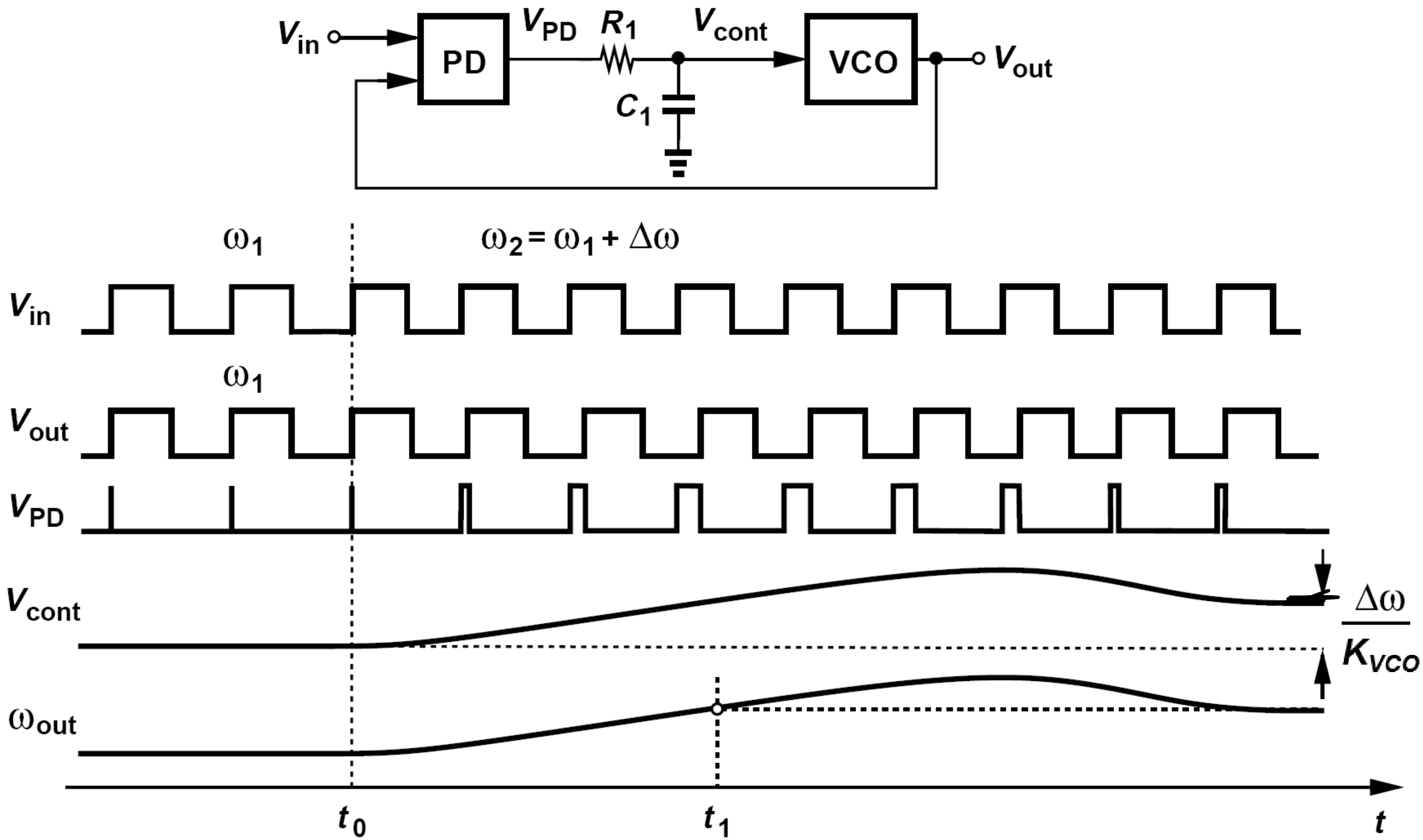




V_{cont} change = $\Delta\omega / K_{VCO}$ ➡ $$\Delta\phi_2 - \Delta\phi_1 = \frac{\Delta\omega}{K_{PD} K_{VCO}}$$

- Phase error varies with the frequency.
- To minimize this variation, $K_{PD}K_{VCO}$ must be maximized.
- $K_{PD}K_{VCO}$ is called the "loop gain".

Response of PLL to Input Frequency Step

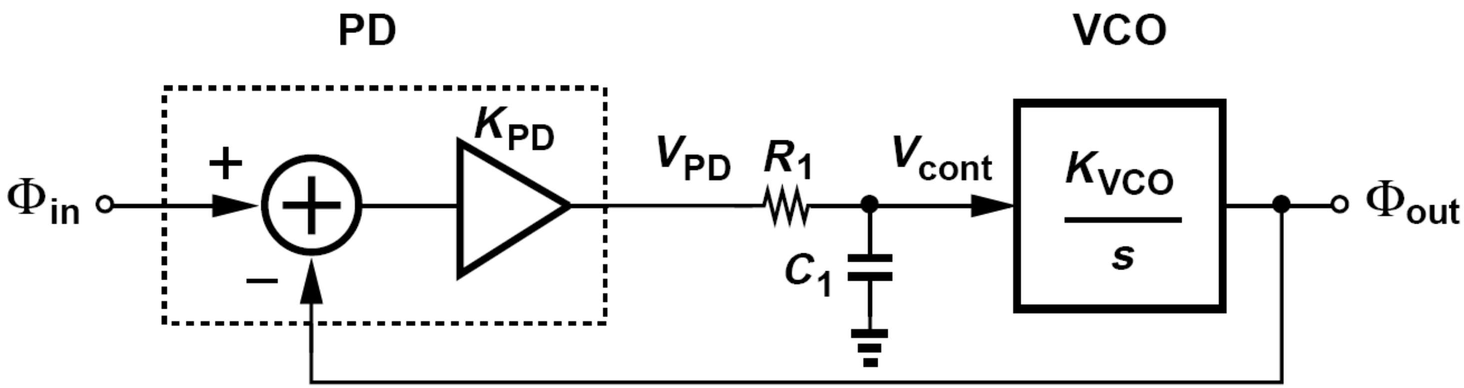


- The loop locks only after two conditions are satisfied:

(1) ω_{out} becomes equal to ω_{in}

(2) the difference between ϕ_{in} and ϕ_{out} settles to its proper value

Loop Dynamics: Phase Domain Model



Open-loop transfer function

$$[K_{PD}/(R_1C_1s + 1)](K_{VCO}/s)$$

Closed-loop transfer function

$$H(s) = \frac{\phi_{out}}{\phi_{in}}(s) = \frac{K_{PD}K_{VCO}}{R_1C_1s^2 + s + K_{PD}K_{VCO}}.$$

Damping Factor and Natural Frequency

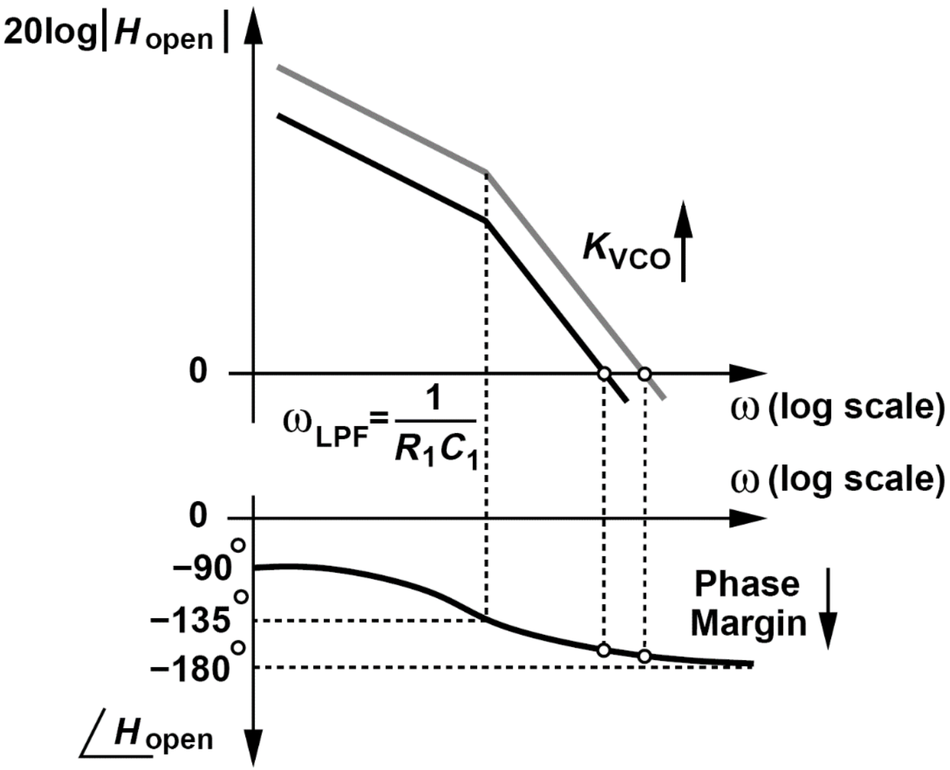
$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$$

$$\omega_n = \sqrt{K_{PD}K_{VCO}\omega_{LPF}}$$

- The damping factor is typically chosen to be $\sqrt{2}/2$ or larger so as to provide a well-behaved (critical damped or overdamped) response.
- $\omega_{LPF}=1/(R_1C_1)$

ζ is inversely proportional to K_{VCO}.



Behavior of the open-loop transfer function, H_{open}, for two different values of K_{VCO}

As K_{VCO} increases, the unity-gain frequency rises, thus reducing the phase margin (PM).

Drawbacks of Type-I PLL

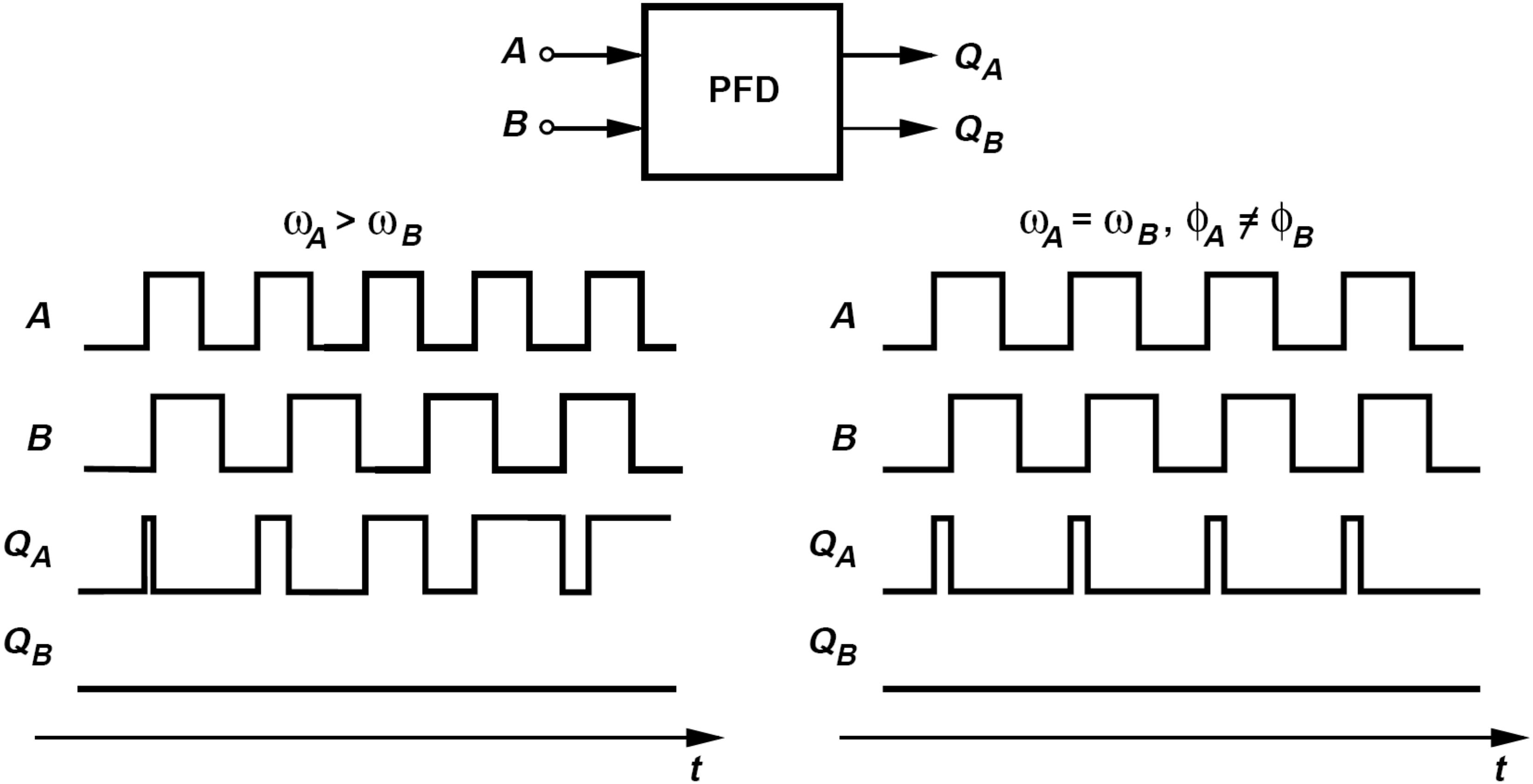
- Tight relation between the loop stability and the corner frequency of the low-pass filter. Ripple on the control line modulates the VCO frequency and must be suppressed by choosing a low value for ω_{LPF}, leading to a less stable loop

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$$

- Suffers from a limited “acquisition range”

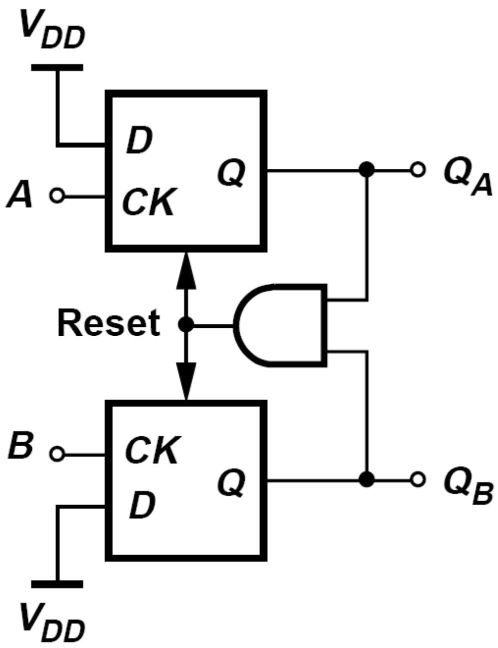
  If the VCO frequency and the input frequency are very different at the start-up, the loop may never “acquire” lock.

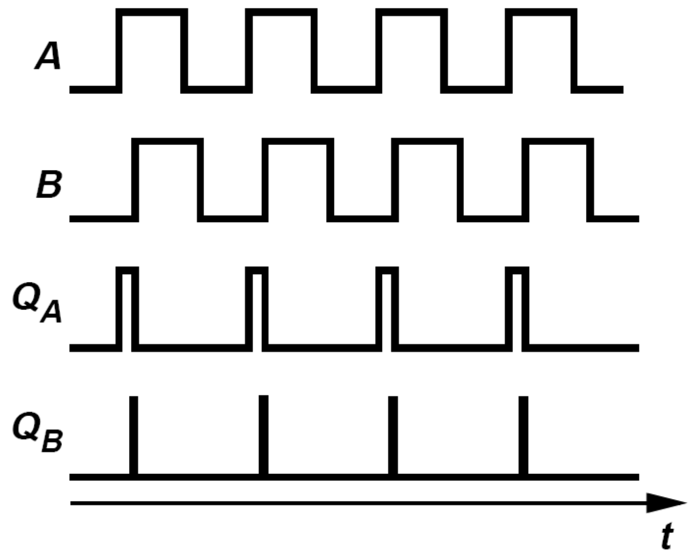
Type-II PLLs: Phase/Frequency Detectors



- A rising edge on *A* yields a rising edge on Q_A (if Q_A is low)
- A rising edge on *B* resets Q_A (if Q_A is high)
- The circuit is symmetric with respect to *A* and *B* (and Q_A and Q_B)

PFD: Logical Implementation





- Q_A and Q_B are simultaneously high for a duration given by the total delay through the AND gate and the reset path of the flipflops.