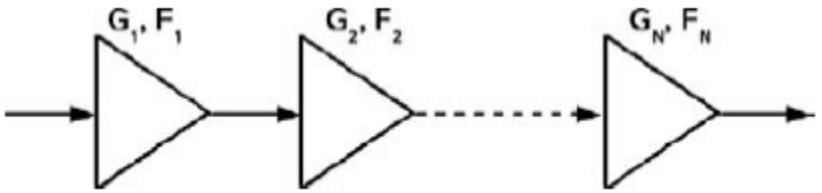
ELC4005: Selected Topics in Electronics I
EECS331: Advanced Topics in Electronics I

Lecture 5

Low Noise Amplifiers

LNA Figure of Merit



$$F = F_1 + \frac{F_2 - 1}{G_{a,1}} + \ldots + \frac{F_N - 1}{G_{a,1}G_{a,2}\ldots G_{a,N-1}}$$

- LNA should have a low NF along with adequate gain to suppress the noise of the subsequent Rx stages
- LNA figure of merit, defined by the ITRS roadmap:

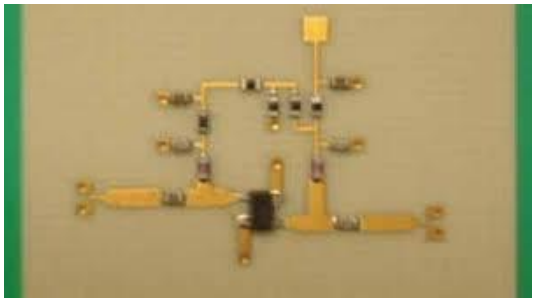
$$FOM_{LNA} = \frac{G \times IIP_3 \times f}{(F-1) \times P}$$

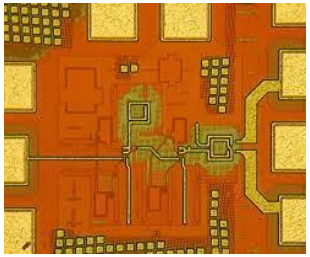
- Maximizing the FoM of the LNA implies simultaneously:
  - minimizing the noise factor
  - increasing the gain
  - maximizing linearity
  - minimizing power dissipation
  - reducing the input reflection coefficient

2011 ITRS Roadmap. www.itrs.net

LOW-NOISE DESIGN PHILOSOPHY

Discrete LNAs

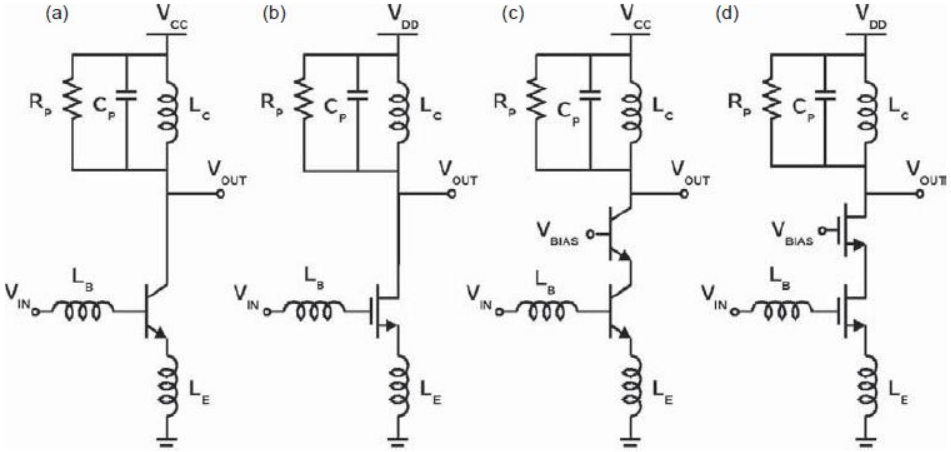


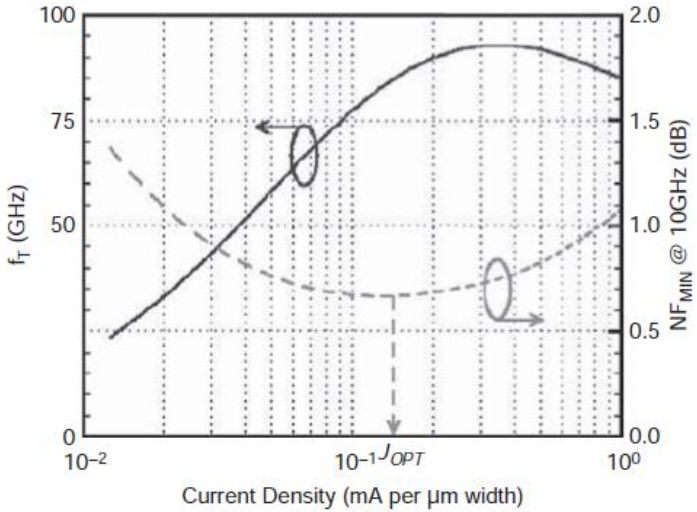


MMICs

- **Traditional LNA design (before monolithic microwave integrated circuits MMICs) :**
  - Used **external** passive matching networks to transform Z_s to Z_{OPT} of a discrete transistor
  - **Discrete** transistor was biased at J_{OPT} (minimum NF_{min})
  - In general, Re{Z_{OPT}} and Re{Z_{in}} of the transistor are not equal→ sub-optimal S_{11} and gain for the LNA in order to minimize its noise factor
  - Measured S-parameters of the transistor at the J_{OPT} & the noise circles were used for design
- Move to MMICs:
  - integrated matching circuits & more flexibility in transistor sizing & biasing
  - On-chip lossy passive matching components → New design methodology to reduce number/loss of passives **"Active matching"**

CS/CE with/without Cascode LNAs





- CS/CE topologies are the most widely used LNAs→ best NF & permit **simultaneous noise and input impedance matching**
- Cascode isolates output from input → extends BW & higher gain with low NF penalty
- Avoid active loads → increase noise & degrade linearity
- Fix transistor finger width W_f to get the desired R_g/F_{MAX}
- Sweep J_{DS} by changing the I_{DS} (or number of fingers N, $W=NxW_f$)
- Bias the transistors at the J_{OPT} of the topology → lowest NF_{MIN}

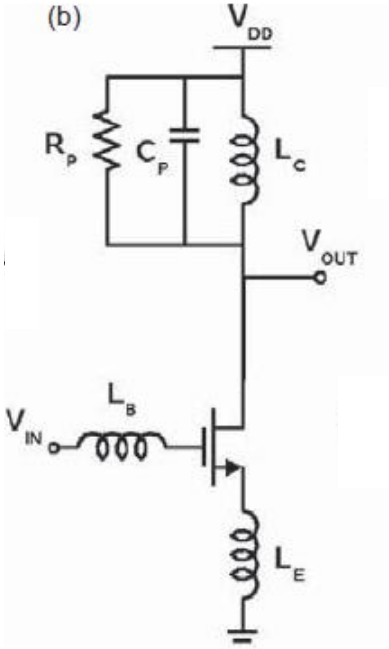
CS LNAs: Active Noise Matching

$$J_{OPT} = \frac{I_{DS}}{W}$$

$$g_m = \sqrt{2\mu C_{OX}\frac{W}{L}I_{DS}} = W\sqrt{2\mu C_{OX}\frac{J_{OPT}}{L}}$$

$$Z_{SOPT}(\text{FET}) \approx \frac{1}{\omega(C_{gs}+C_{gd})}\left[\sqrt{\frac{g_m(R_s+R_g)}{k_1}}+j\right]$$

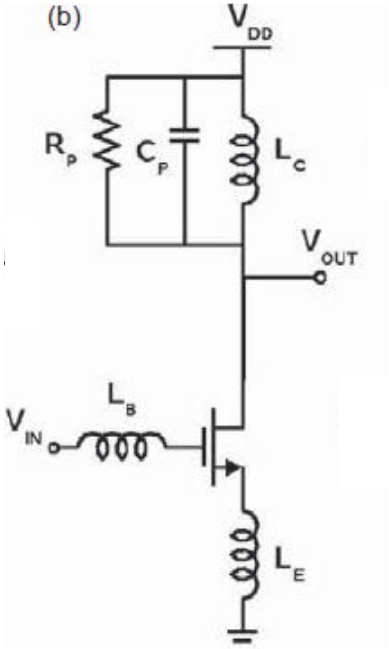
$$re\{Z_{SOPT}\} \downarrow \; as \; W \uparrow$$



- To minimize the number of components/simplify matching circuit → Active matching
- Re{Z_{SOPT}} decreases as the total transistor W increases
- Calculate the total width W or (N) for optimum noise impedance, i.e. re{Z_{SOPT}}=Zo
- Noise matching now only requires a single series reactive component → significant simplification to matching circuit

CS LNAs: Input Matching by Degeneration

- Adding a lossless degeneration inductor L_S forms a series–series feedback network
  - Doesn't change the re{Z_{SOPT}}
  - NF_{min} remains the same
  - Increases re{Z_{in}} according to the following:



$$Z_{IN} \approx R_b + r_E + \omega_T L_E + j\left(\omega L_E + \omega L_B - \frac{1}{\omega C_{IN}}\right)$$

$$\Re\{Z_{IN,MOS}\} = R_g + r_s + R_{LB} + R_{LE} + \omega_{T,MOS} L_E$$

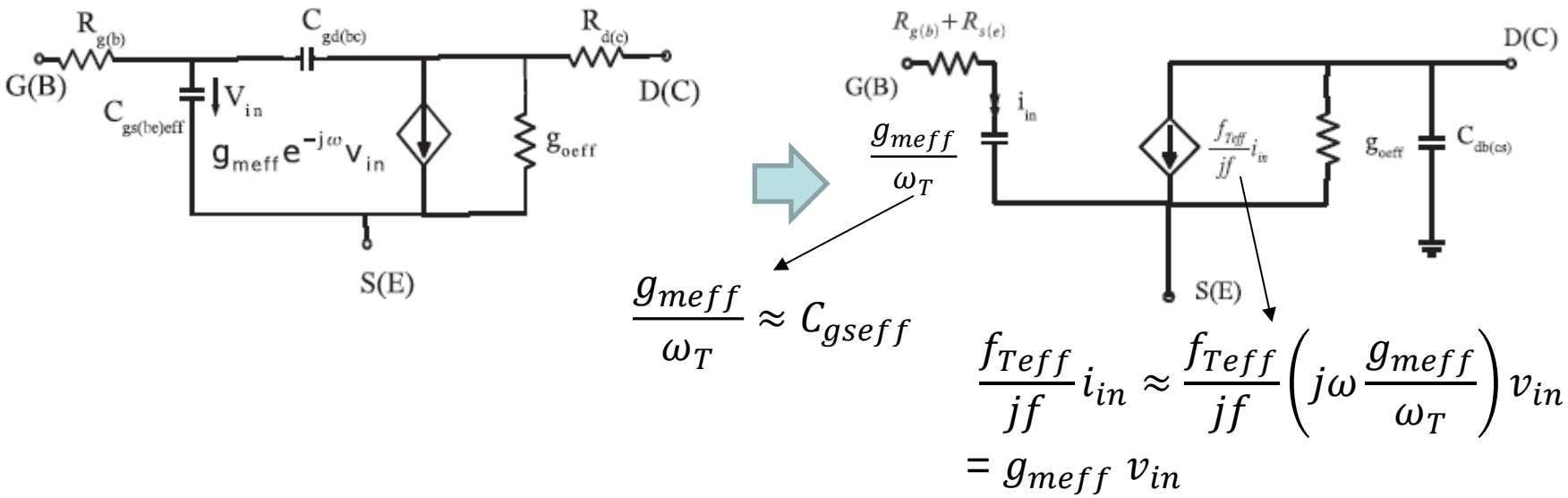
$$L_S = \frac{Z_0 - R_g - R_s}{2\pi f_T}$$

$$C_{IN} = C_{gseff} + C_{gd}$$

$$C_{IN} = \frac{g_{meff}}{\omega_T}$$

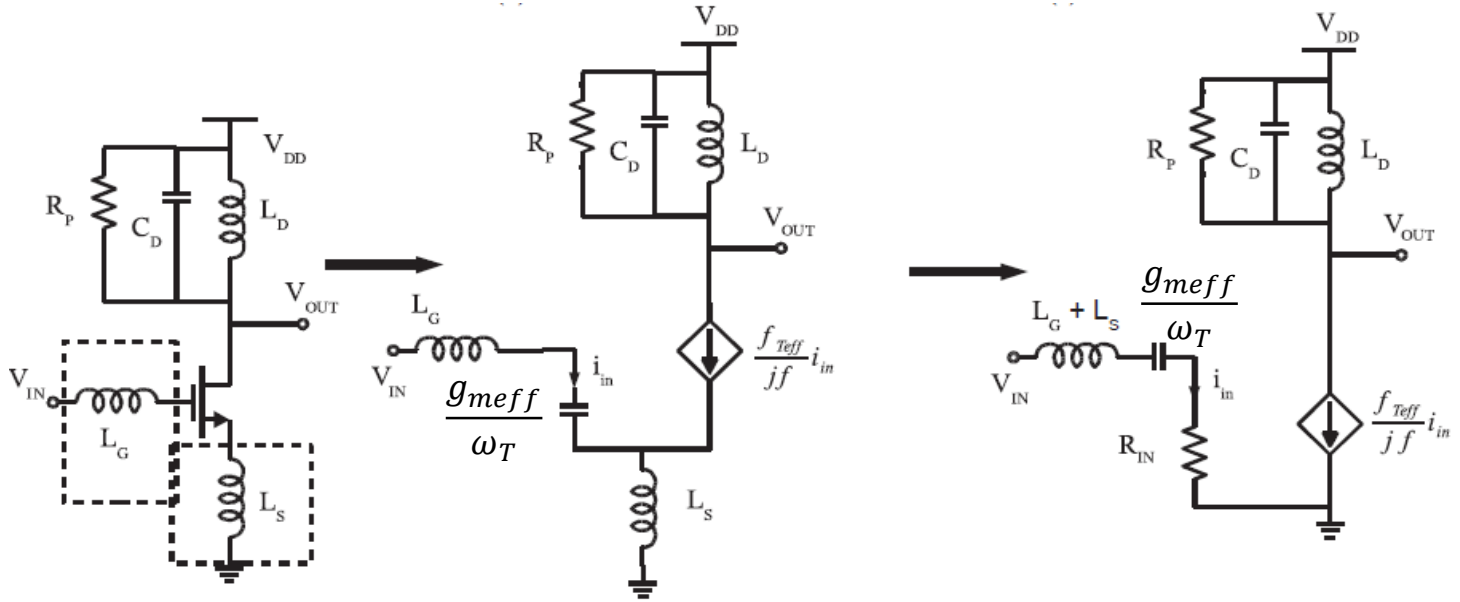
- Input of the LNA behaves as a series resonant RLC circuit
- Re{Z_{in}} is freq. independent, proper choice of L_S can set Re{Z_{in}}=Z_o
- Only a single series reactive component is necessary to achieve input match → simplify input matching/reduce its losses

Unilateral Transistor equivalent circuit



- Simplified, unilateral, transistor equivalent circuit based on frequency-dependent current source neglects feedback from output to input due to C_{gd}
- Model neglects Miller effect

Tuned CS LNA Gain



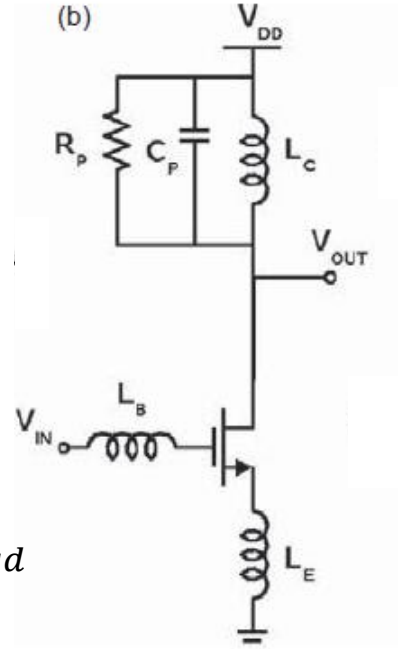
- Using the unilateral transistor equivalent circuit model

$$v_{in} = i_{in}\left(j\omega L_G + R_g + R_s + \frac{\omega_{Teff}}{j\omega g_{meff}} + j\omega L_S\right) + j\omega L_S \frac{\omega_{Teff}}{j\omega} i_{in} \qquad i_{sc} = \frac{-f_{Teff}}{jf} i_{in} = j\frac{f_{Teff}}{f} i_{in}$$

$$Z_{in} = R_g + R_s + \omega_{Teff} L_S + j\left[\omega(L_G + L_S) - \frac{\omega_{Teff}}{\omega g_{meff}}\right]. \qquad C_{IN} = \frac{g_{meff}}{\omega_{Teff}} \text{ and } R_{IN} = R_s + R_g + \omega_{Teff} \times L_S$$

CS LNAs: Input Matching by Degeneration

- Adding a lossless degeneration inductor L_S forms a series–series feedback network
  - Doesn't change the re{Z_{SOPT}}
  - NF_{min} remains the same
  - Increases re{Z_{in}} according to the following:



$$Z_{IN} \approx R_b + r_E + \omega_T L_E + j\left(\omega L_E + \omega L_B - \frac{1}{\omega C_{IN}}\right)$$

$$C_{IN} = \frac{g_{meff}}{\omega_T}$$

$$\Re\{Z_{IN,MOS}\} = R_g + r_s + R_{LB} + R_{LE} + \omega_{T,MOS} L_E$$

$$C_{IN} = C_{gseff} + C_{gd}$$

$$L_S = \frac{Z_0 - R_g - R_s}{2\pi f_T}$$

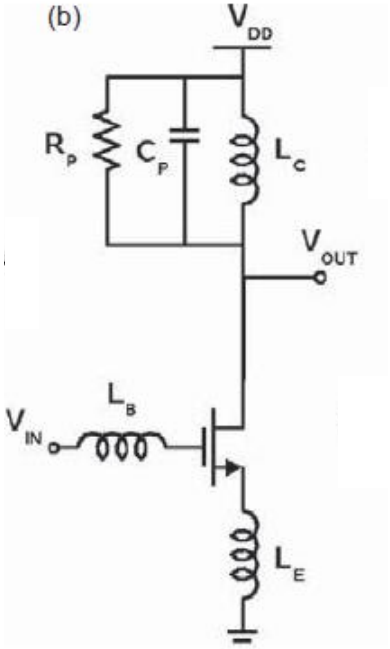
- Input of the LNA behaves as a series resonant RLC circuit
- Re{Z_{in}} is freq. independent, proper choice of L_S can set Re{Z_{in}}=Z_o
- Only a single series reactive component is necessary to achieve input match → simplify input matching/reduce its losses

CS LNAs: Reactive Input/Noise Matching

$$Z_{IN} \approx R_b + r_E + \omega_T L_E + j\left(\omega L_E + \omega L_B - \frac{1}{\omega C_{IN}}\right)$$

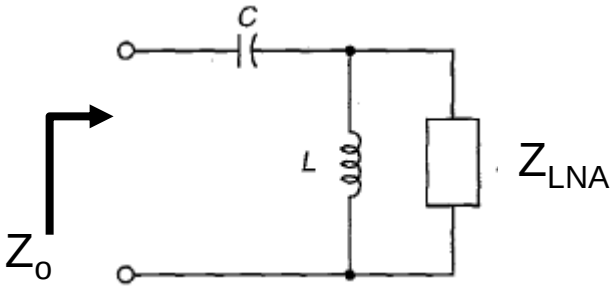
- The input series inductor L_G is added to tune out the im{Z_{in}} to zero at the LNA operating frequency:

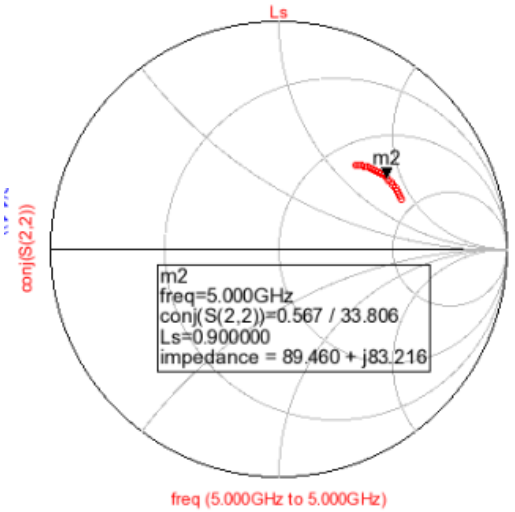
$$L_G \approx \frac{\omega_T}{\omega^2 g_{meff}} - L_S$$



- For both FETs and HBTs, the imaginary part of the optimum noise impedance im{Z_{SOPT}} and imaginary part of the input impedance im{Z_{in}} are roughly equal
- L_G also cancels out X_{SOPT} → Simultaneous gain and noise match

Output matching to maximize gain





- LNA output impedance is usually capacitive with real part>Z_o
- The simplest matching network can be realized with an L-section
- A shunt inductor, L connected to VDD, followed by a series capacitor towards the load

Tuned CS LNA Gain (Cont'd)

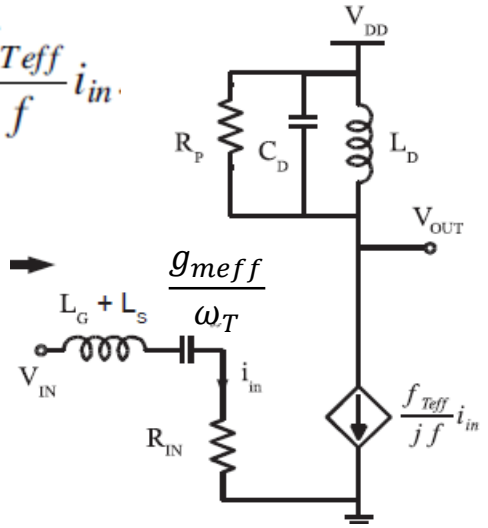
$$V_{out} = \frac{I_{sc} \times R_P}{2} = j\frac{f_{Teff} \times R_P}{2f} i_{in}$$

$$i_{sc} = \frac{-f_{Teff}}{jf} i_{in} = j\frac{f_{Teff}}{f} i_{in}$$

$$I_{load} = \frac{I_{sc}}{2} = j\frac{f_{Teff}}{2f} i_{in}$$

$$P_{load} = V_{out} \times I_{load}^{*} = \frac{f_{Teff}^2 \times R_P}{4f^2} |i_{in}|^2$$

$$P_{in} = v_{in} \times i_{in}^{*} = i_{in} \times R_{IN} \times i_{in}^{*} = R_{IN} |i_{in}|^2.$$



- Only half of the short-circuit current ends up in the matched load, with the other half flowing through the R_P
- The power gain in a matched load R_P can be expressed:

$$G = \frac{P_{load}}{P_{in}} = \frac{f_{Teff}^2}{4f^2} \times \frac{R_P}{R_{IN}}$$

→ $R_{IN}=Z_o$ for input matching

- To maximize the LNA gain the parallel tank resistance R_P must be increased, i.e. designing for a high-Q load inductor L_D (narrowband)

$$R_P = Q\omega_0 L_C$$

CS/CE LNA Linearity

- Linearity is determined by the VGS non-linearity at large input voltages
- Series-Series feedback via L_S improves the LNA linearity by reducing the swing on VGS
- The linearity is proportional to the feedback provided by the L_S:

$$1 + j\omega L_S g_{meff}$$

- To maximize linearity, the LNA transistor must be biased at high current density, (large g_m) & use a large L_S
- To increase LNA linearity:
  - Increase the bias current by making transistors larger while still biasing them at J_{OPT}
  - $R_{SOPT} < Z_o$ → Noise impedance mismatch
  - R_n is reduced → noise impedance mismatch does not lead to significant degradation from NF_{MIN}

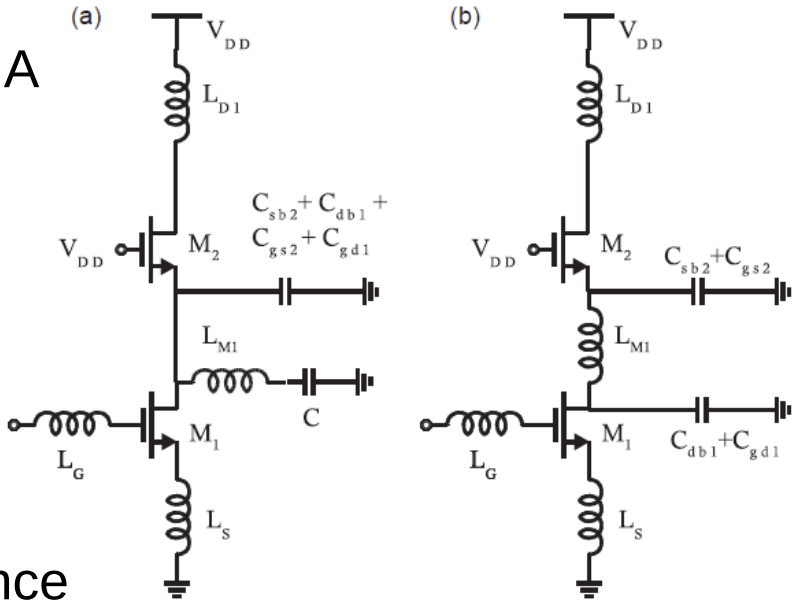
$$F = F_{MIN} + \frac{R_n}{G_s}\left|Y_s - Y_{sopt}\right|^2$$

BW Extension for Cascode CS LNAs

- Cascode LNA allows increasing the LNA gain with slight hit in NF
- Cascode noise circulates in device
- Placing a shunt inductor L_{M1} to an AC ground → resonates the parasitic capacitances:

$$C_{gd1} + C_{db1} + C_{sb2} + C_{gs2}$$

- Shunt inductor → narrow band resonance



- Series inductor L_{M1} forms an artificial transmission line
- This absorbs the effect of the parasitic capacitance
- L_{M1} also improves the noise figure of the cascode stage at mm-waves (CG noise sources degenerated by higher impedance)

BW Extension for Cascode CS LNAs

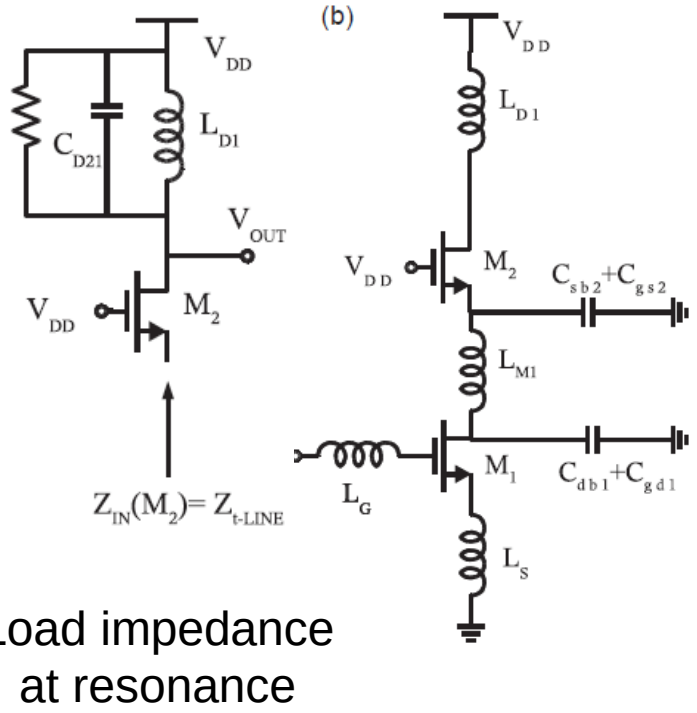
- The characteristic impedance of this TL can be expressed as:

$$Z_{01} = \sqrt{\frac{L_{M1}}{C_{gs2} + C_{sb2}}}$$

- The inductance L_{M1} is set to match the TL characteristic impedance to the impedance seen at the source of the CG:

$$Z_{01} = Z_{M2,in} = \frac{1}{g_{m2}} + \frac{\omega L_{D1} Q}{2(1 + g_{m2} r_{o2})}$$

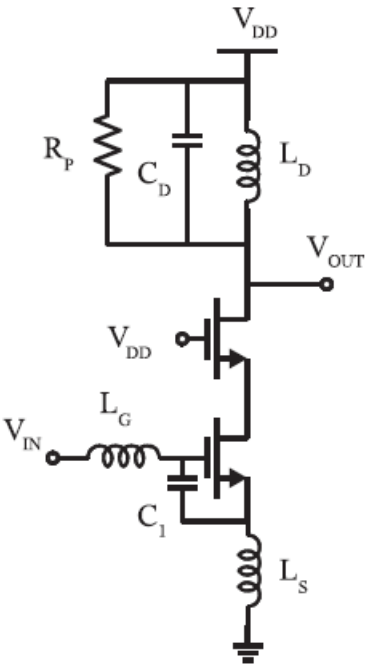
Load impedance at resonance



- Satisfying this condition guarantees maximizing the cascode gain by avoiding interstage mismatches
- The 1/2 factor is due to the extra loading with a matched Z_L to that of the inductor L_{D1} at resonance

POWER-CONSTRAINED CMOS LNAs

- Drawback of CS LNA is the need for large device sizes (& I_{DS}) at frequencies below 20GHz → higher power consumption
- Capacitor C_1 allows reducing R_{SOPT} until it reaches Z_o **<u>without increasing the LNA current</u>**:



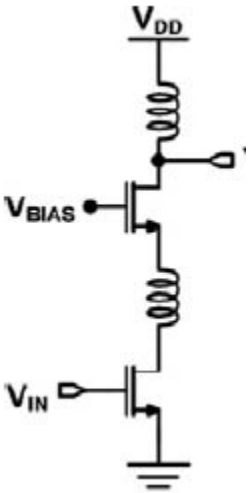
$$Z_{SOPT}(\text{FET}) \approx \frac{1}{\omega(C_{gs}+C_{gd})}\left[\sqrt{\frac{g_m(R_s+R_g)}{k_1}}+j\right]$$

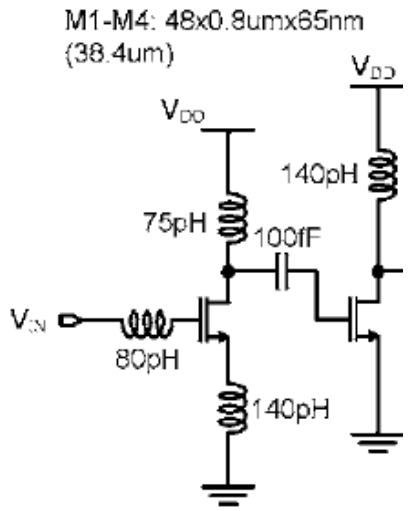
$$\omega_T = \frac{g_m}{C_{gs}+2C_{gd}} \qquad L_S = \frac{Z_0 - R_g - R_s}{2\pi f_T}$$

$$f_T' \rightarrow \frac{f_T}{1+\frac{C_1}{C_{gs}+2C_{gd}}} \qquad L_S' \rightarrow L_S\left(1+\frac{C_1}{C_{gs}+2C_{gd}}\right)$$

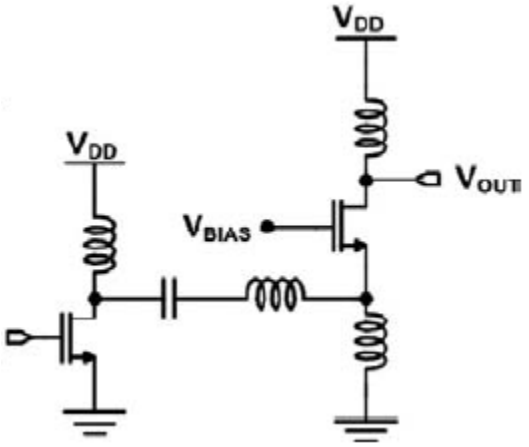
- Drawbacks:
  - f_T of artificial transistor drops by $1+C_1/(C_{gs}+2C_{gd})$
  - Degeneration inductor increases by the same factor
  - LNA gain & NF_{MIN} will also degrade

LOW-VOLTAGE LNA TOPOLOGIES





Multi-stage CS LNA



AC-coupled cascode CS LNA

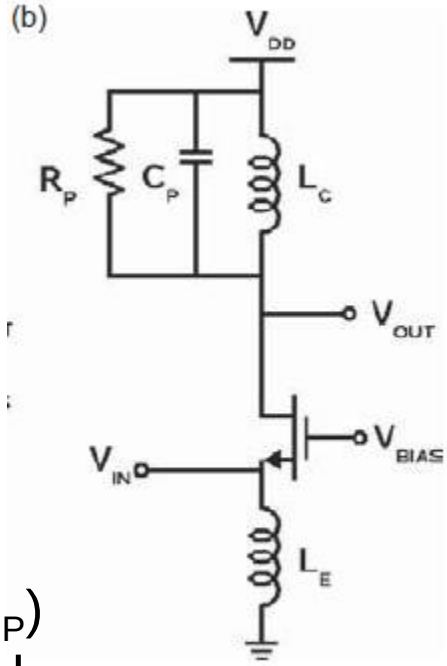
- In advanced CMOS nodes, supply voltages are reduced → can't stack FETs without reducing V_{DS} (degraded f_T and f_{MAX})
- Could employ a multi-stage CS LNA → degraded isolation
- AC-coupled cascode CS stages:
  - reduce the number of transistors in the vertical stack
  - robustness to process & supply variation
  - cost is doubling the bias current

Common Gate CG LNAs

- CG LNA are suitable for:
  - lower power LNAs
  - Wide bandwidth LNA down to DC
- Provides higher NF & lower linearity compared to CS/cascode LNAs
- The re{Z_{in}} is set by I_{DS} (or g_m) of the transistor:

$$\Re\{Z_{IN,CG}\} = \frac{1}{g_{m,MOS}} + \frac{R_P}{1 + \frac{g_{m,MOS}}{g_o}}$$

- Conductance g_o degrades the isolation input to output



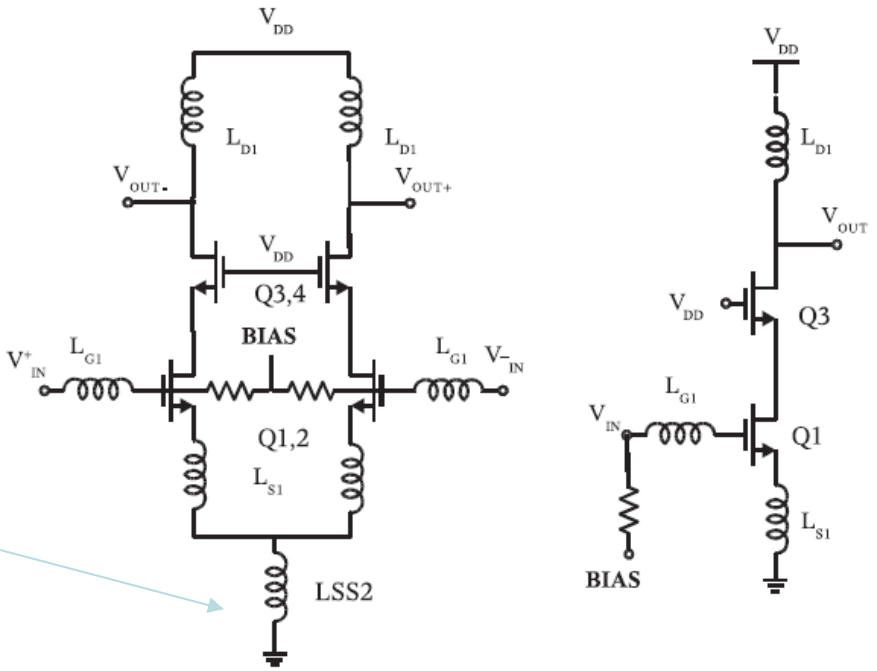
- re{Z_{in}} is a function of the bias and the load resistance (R_P)
- Input capacitance (C_{gs}) is canceled by the shunt inductor L_E
- To increase CG linearity higher current is required → trade-off between linearity and match
- **CG LNA can't be independently noise & impedance matched** (no independent parameters are available)

DIFFERENTIAL LNA DESIGNS

$$Z_{soptdiff} = 2Z_{sopt}(half\_ckt)$$

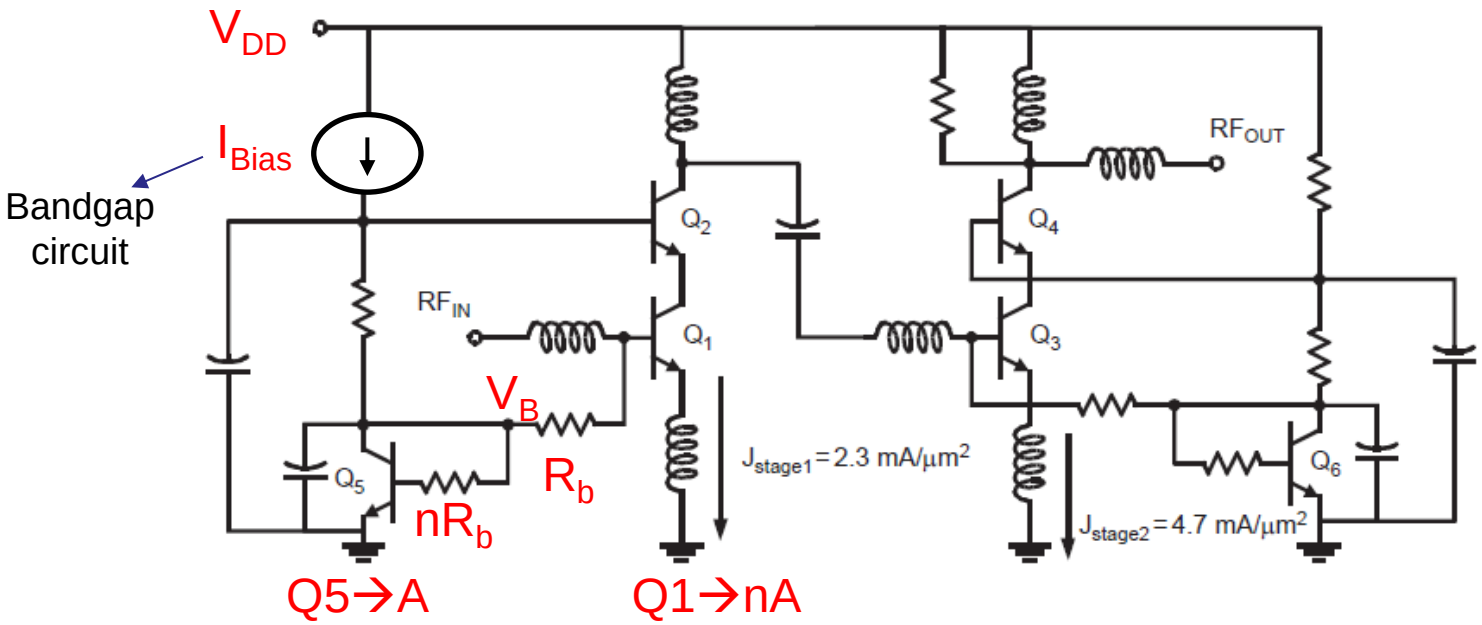
$$Z_{INdiff} = 2\omega_T L_{S1}$$

Common mode inductor added to improve high frequency CMRR



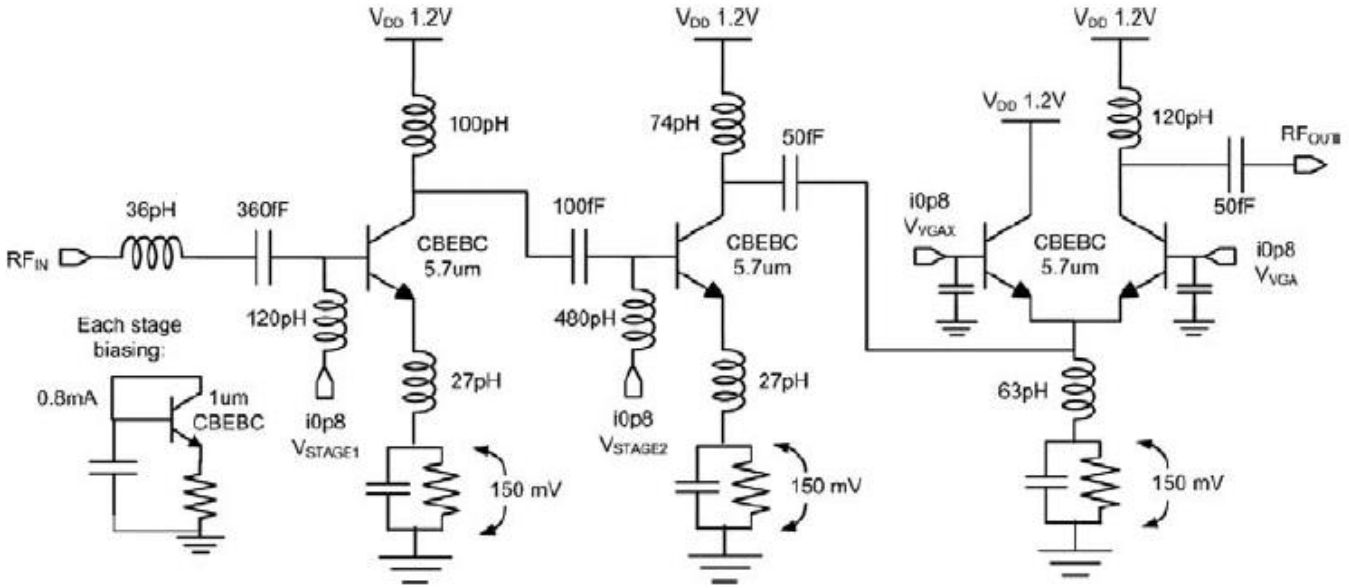
- The differential-mode Z_{SOPT} is 2x the differential-mode half circuit
- L_{S1} is the degeneration inductance per side and ω_T is the cutoff frequency of the differential-mode half circuit
- RF amplifiers typically don't use current sources for biasing due to their low CMRR at high frequency

LOW-NOISE BIAS NETWORKS FOR LNAs



- Bias network must not degrade the NF, high resistance value for R_b ~1-5KΩ (R_b noise current 4kT/R input referred)
- Capacitors, are placed at the cascode base
  - Provides low impedance for gain improvement (gain vs. linearity trade-off)
  - Cascode base capacitor self-resonance frequency > the highest frequency of interest to avoid oscillation
- Decoupling caps are placed at V_B (&V_{DD}) to provide a low impedance in the bandwidth of interest → helps filter noise of bias circuit & supply

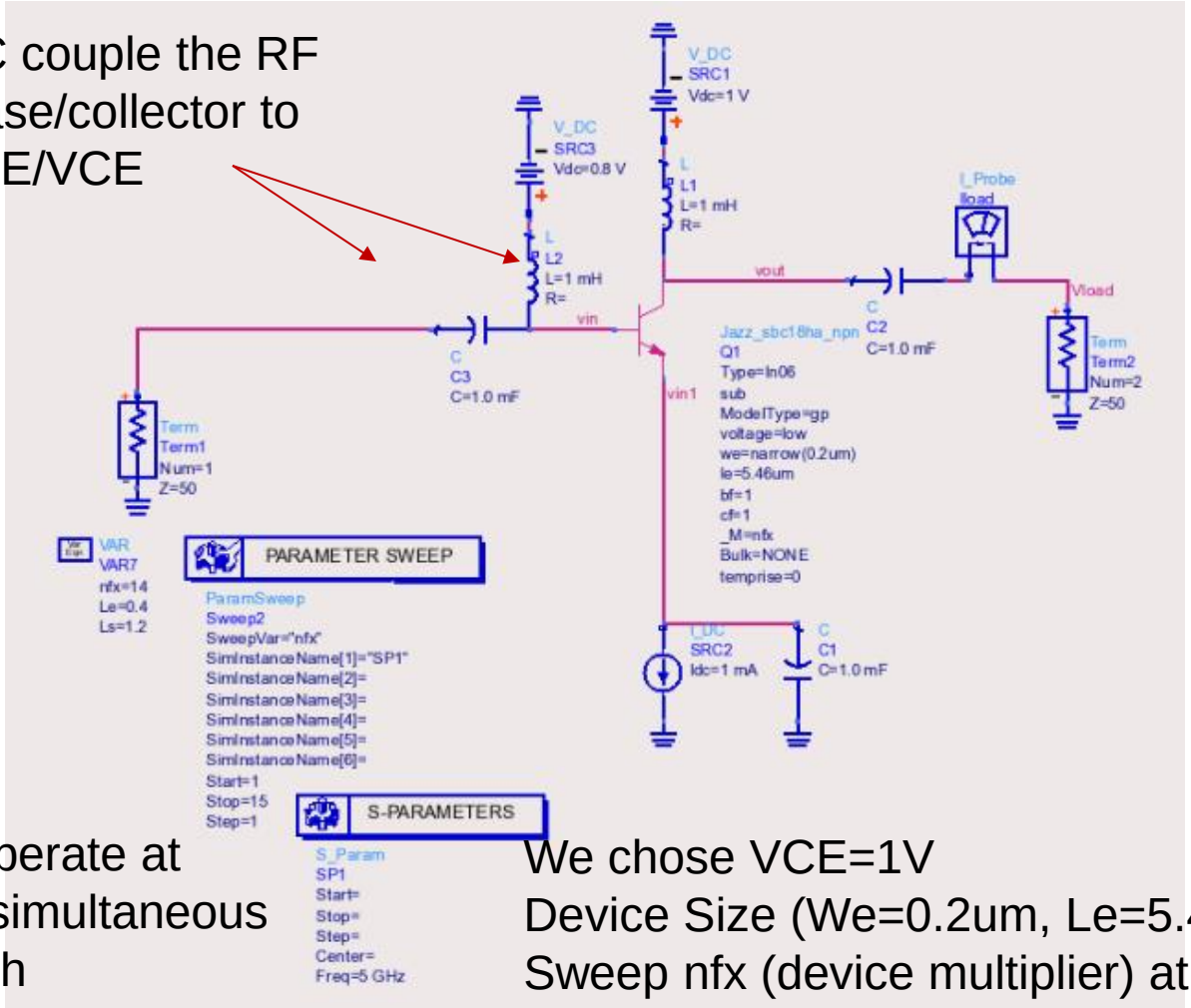
LOW-NOISE BIAS NETWORKS FOR LNAs



- The series bias resistor can be replaced by an inductor→ part of the LNA matching network
- Emitter degeneration resistors can be used to stabilize the bias across PVT
  - Bias degeneration resistor is bypasses to eliminate its impact on LNA gain & noise

Design Example: CE Optimum Current Density

Ideal bias-T used to AC couple the RF signal and Bias the base/collector to the desired VBE/VCE



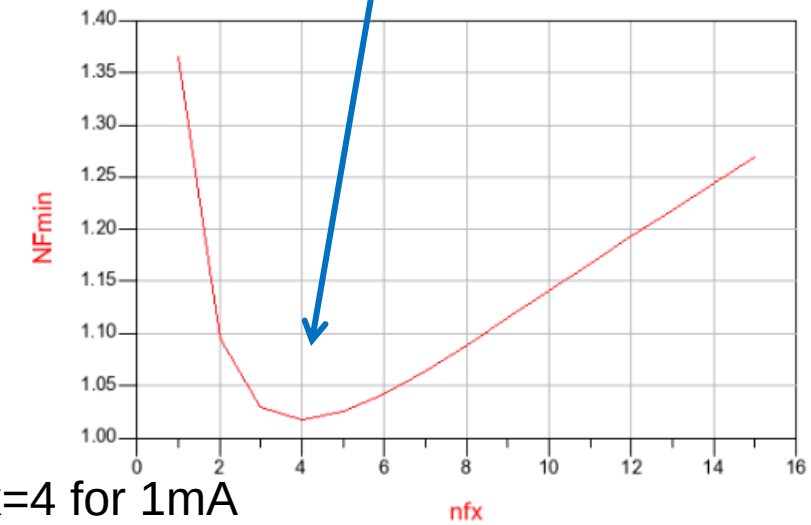
- Design an LNA to operate at 5GHz and achieve simultaneous noise & power match

We chose VCE=1V
Device Size (We=0.2um, Le=5.46um)
Sweep nfx (device multiplier) at **1mA**

Design Example: CE Optimum Current Density

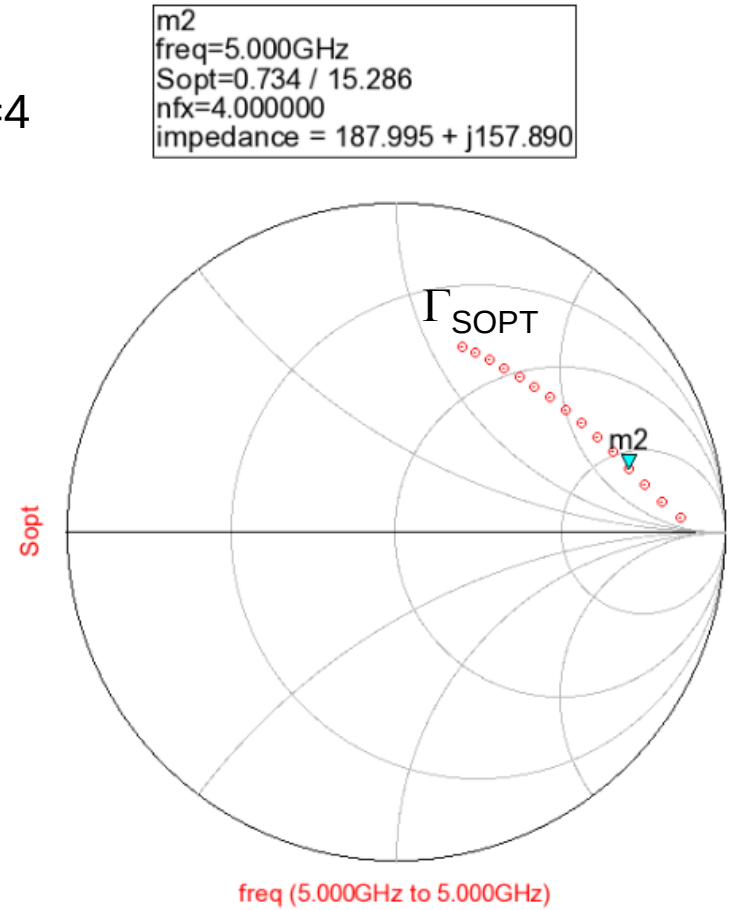
J_{c_opt}= I_c/Device Size = 1mA/(4*0.2*5.46)=0.23mA/um^2

Optimum number of devices in parallel =4



Nfx=4 for 1mA

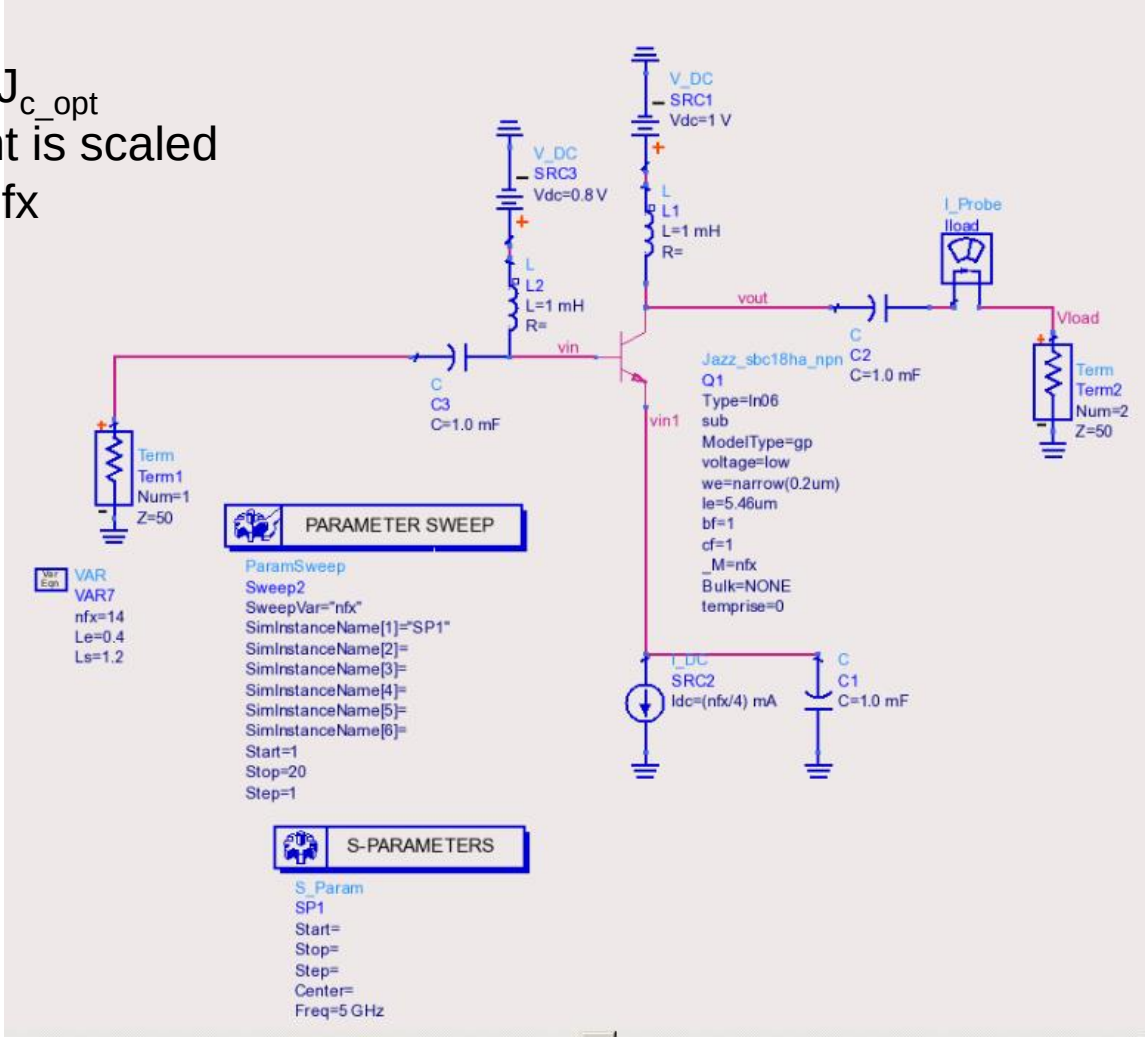
Then, Nfx will equal 8 for 2mA (I_E=nfx/4 mA)



Z_{SOPT} = 187.9+j157.89 -> far from being 50 Ohm matched

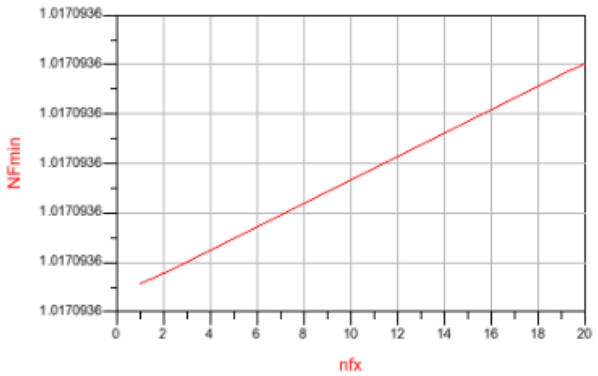
Scale the Current for Re{Z_{SOPT}}=50 Ohms

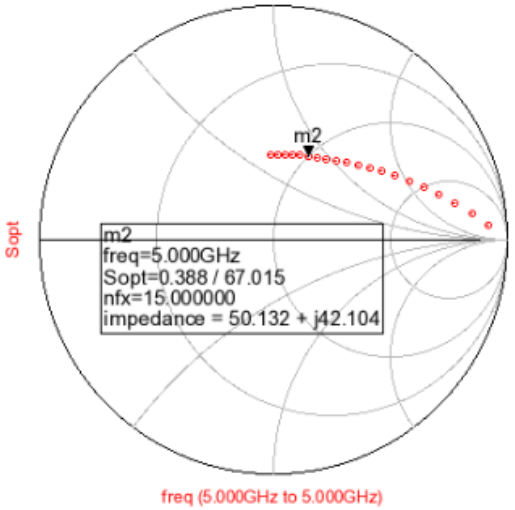
- Current density fixed at: J_{c_opt}
- We swept nfx and current is scaled accordingly: $I_C=J_{c\_opt}$ x nfx

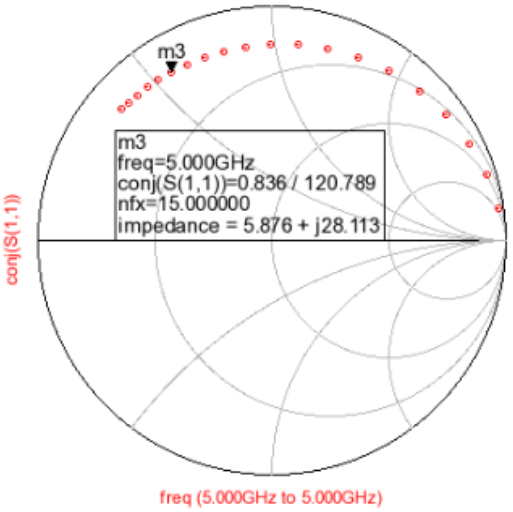


Scale the Current to get re{Z_{SOPT}}=50 Ohms

NF_{min} doen't change since current density is fixed at J_{c_opt}



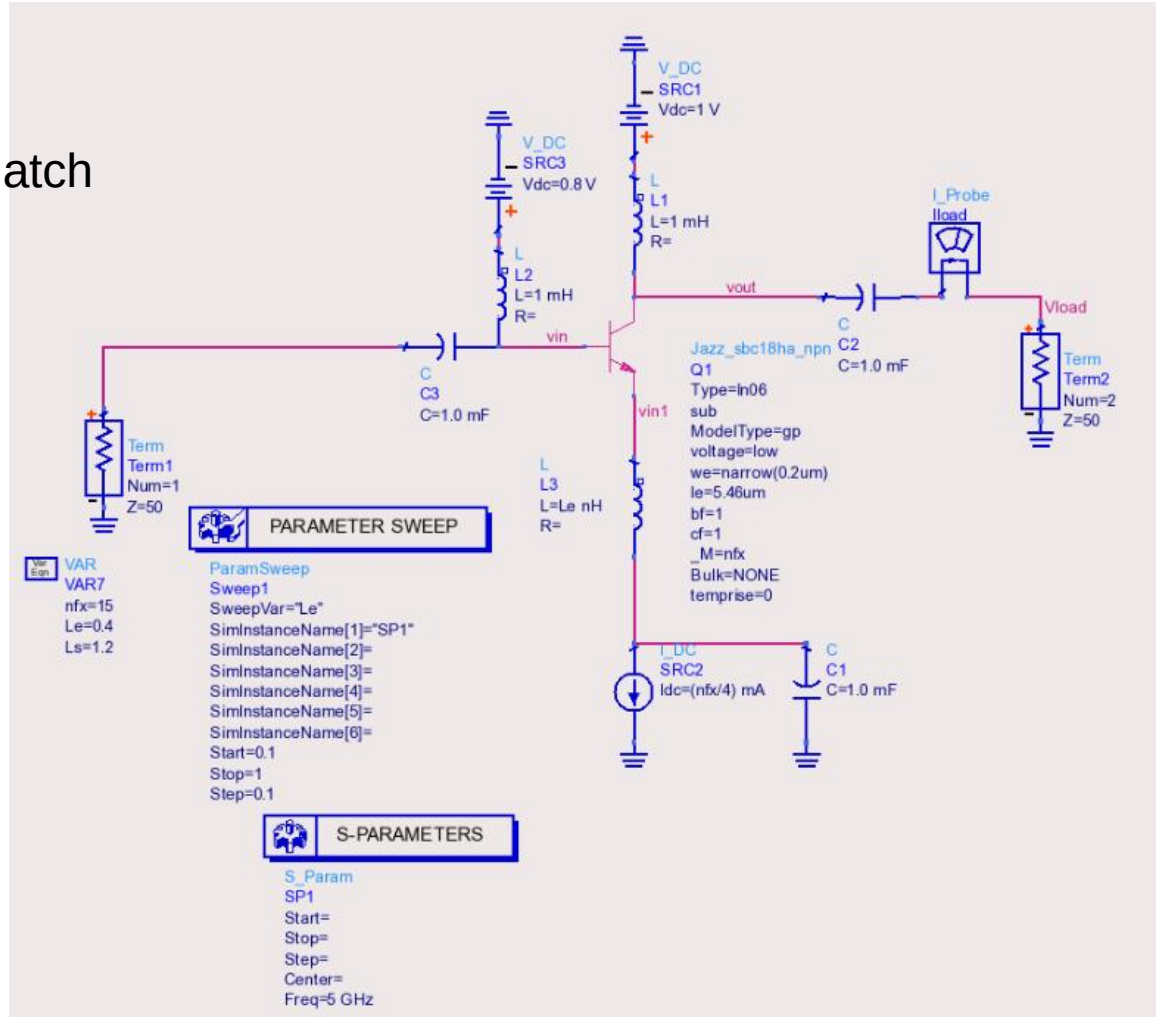




- We swept nfx to get re{Z_{opt}}=50 Ohms
- However, conj (Z_{in})=5.87+j28 Ohms
- The device is large and hence its input impedance is small
- increase re{Z_{in}} without deteriorating the noise match → inductor degeneration

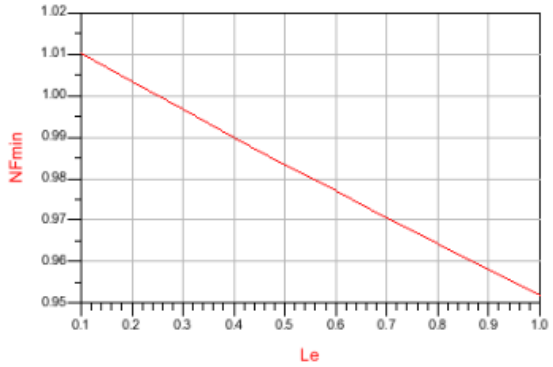
Inductor Degeneration L_E

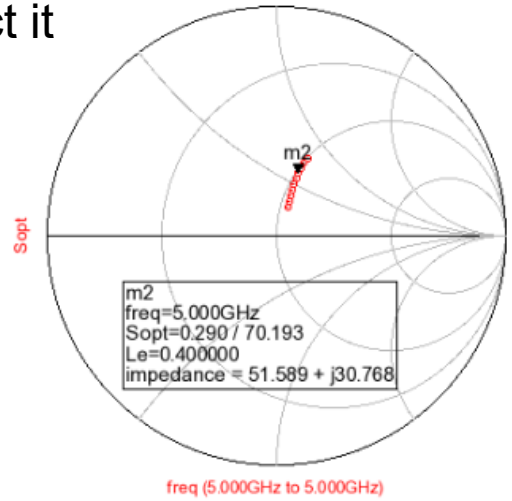
Sweep L_E to match re{Z_{in}} to Z_o

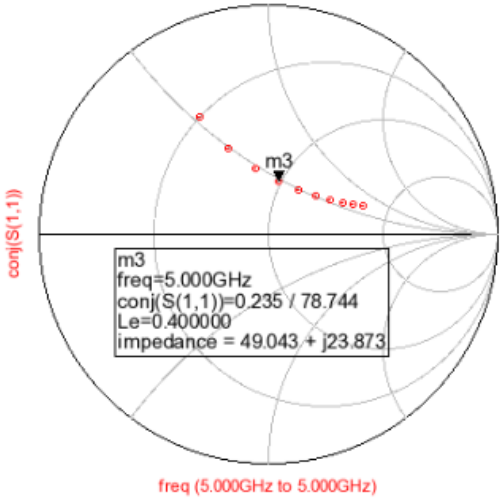


Inductor Degeneration L_E

NF_{min} doen't change since series-series feedback using L_E doesn't affect it



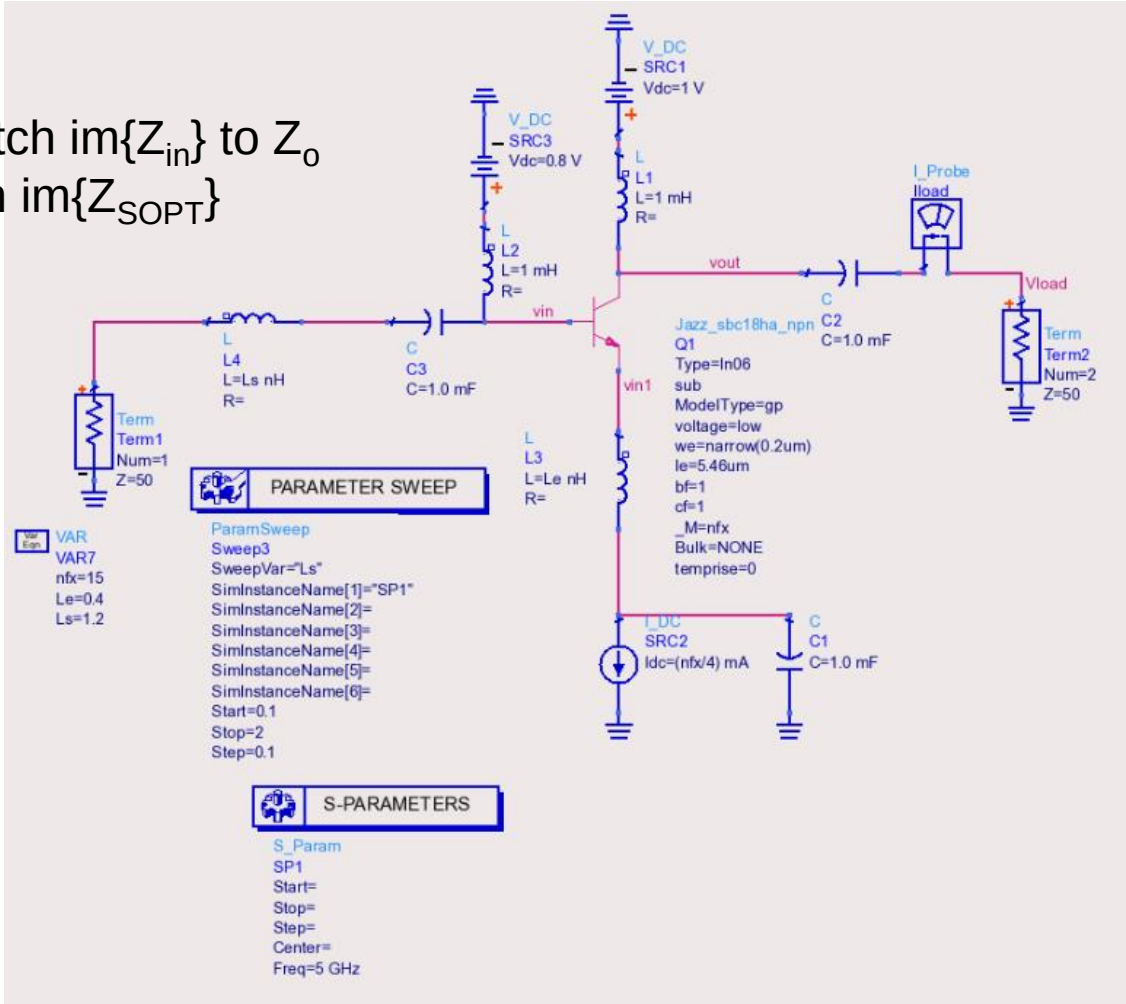




- re{Z_{in}*} is 50 Ohms at Le=0.4nH
- re{Z_{SOPT}} doesn't change much from 50 Ohms
- There is a **small** difference between im{Z_{SOPT}} and im{Z_{in}*}
- Both Z_{SOPT} and Z_{in}* require a series inductor

Series input Inductor L_B

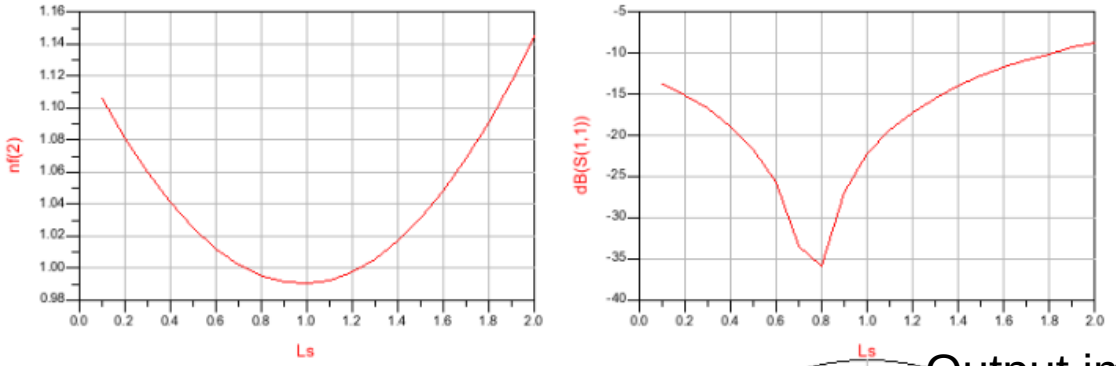
Sweep L_B to match im{Z_{in}} to Z_o
and noise match im{Z_{SOPT}}

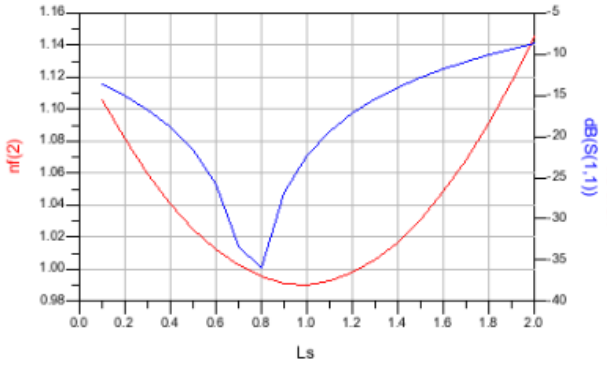


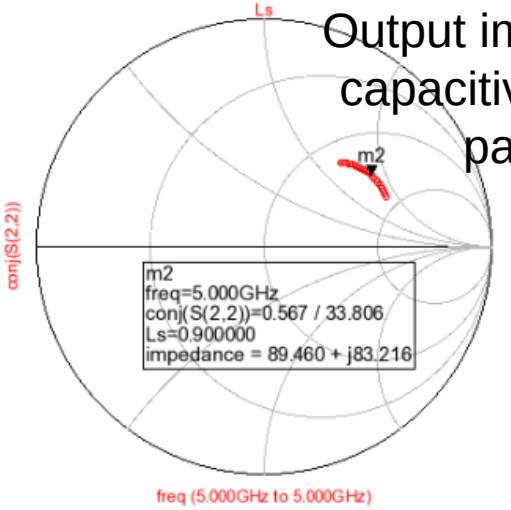
Series input Inductor L_B

- L_B=1nH for optimum noise, L_B=0.8nH for best gain match
- We can set Ls=0.9nH

After noise match was done NF=NF_{min}

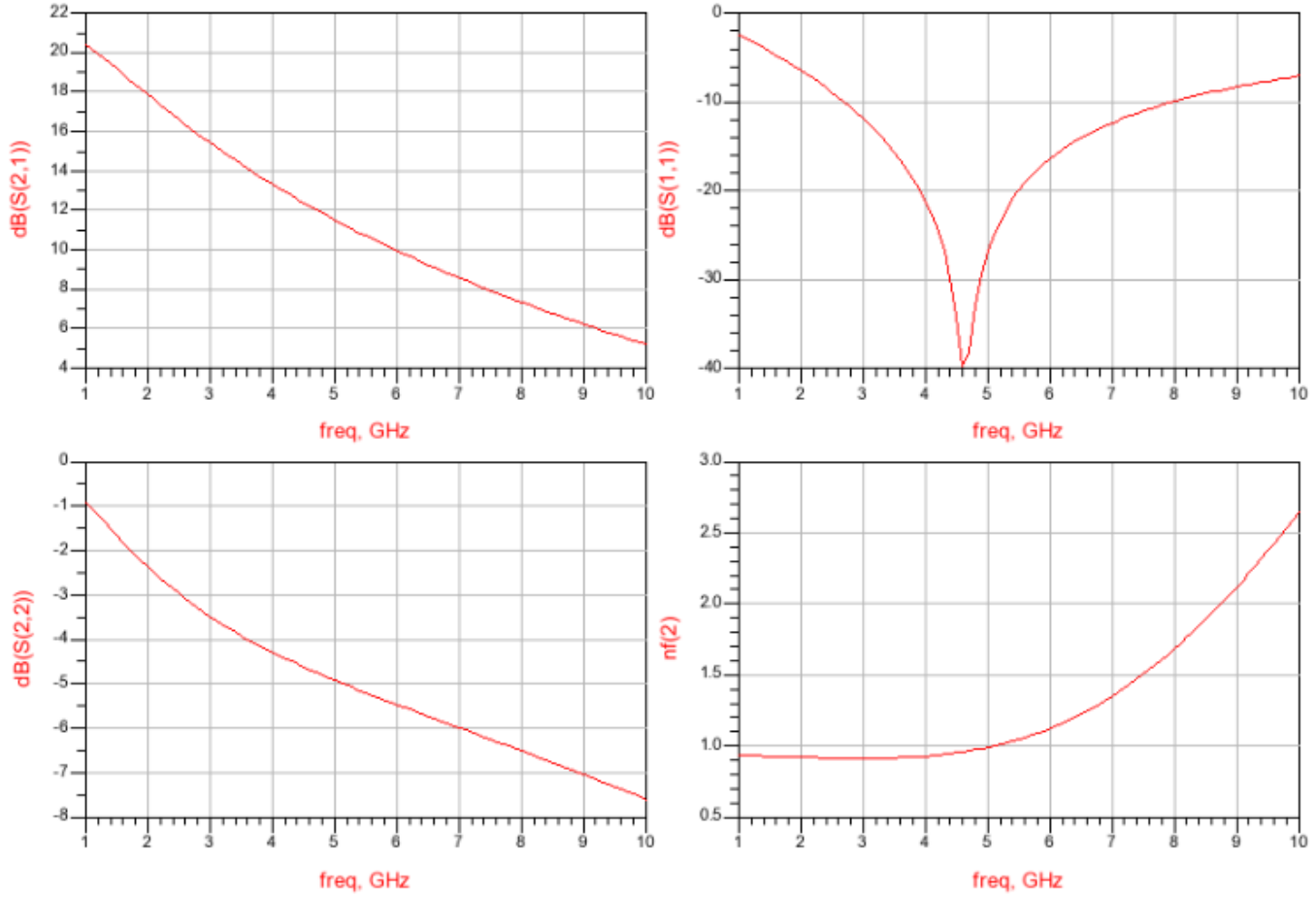




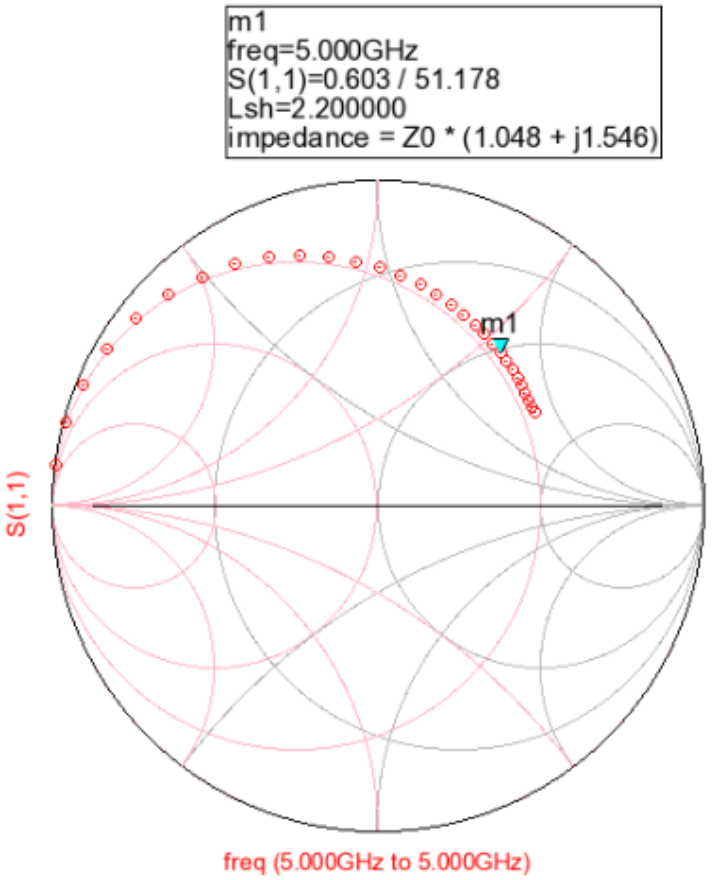


Output impedance is capacitive with real part>Z_o

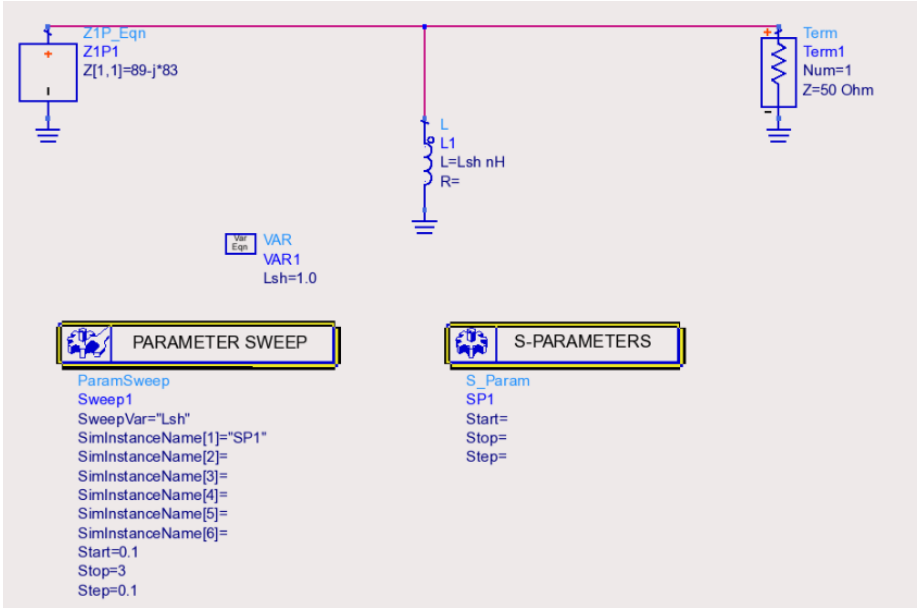
What's the total performance up till now?



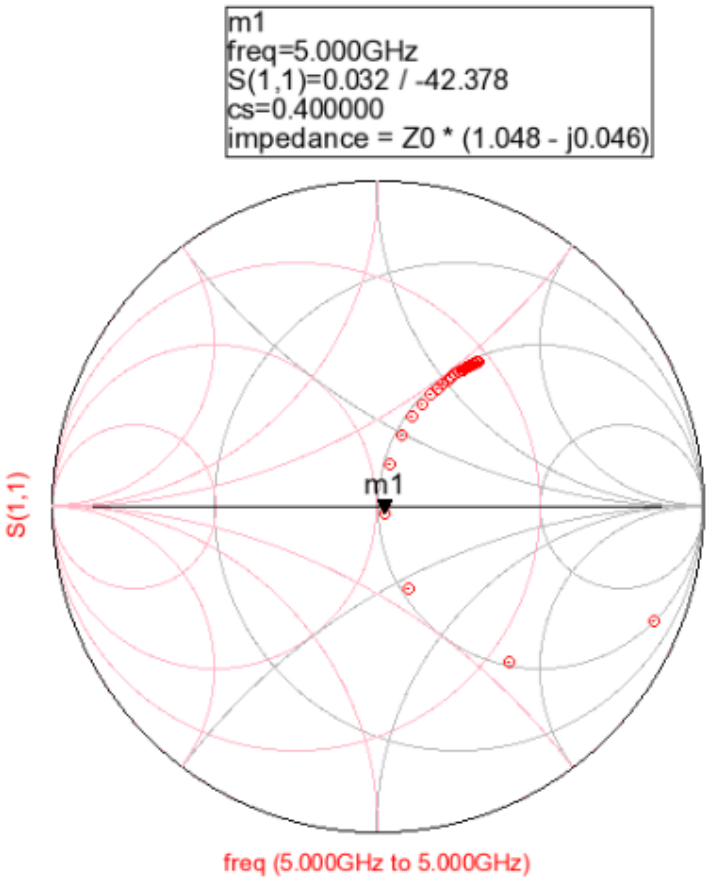
Output Match: Shunt L



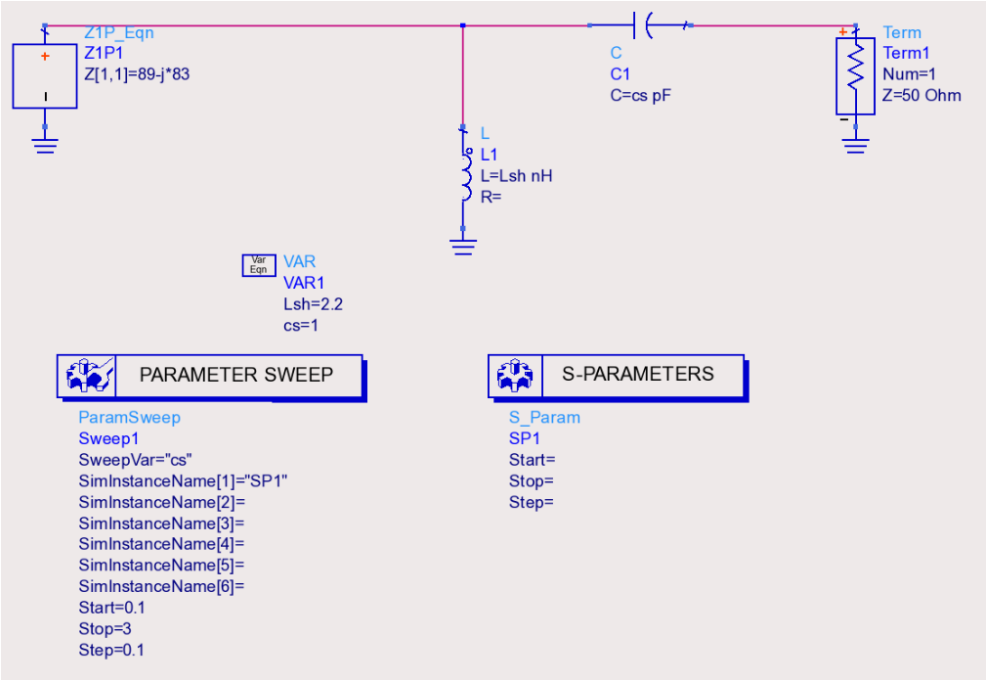
- Size the shunt inductor to get the real part to Z_o



Output Match: Series C

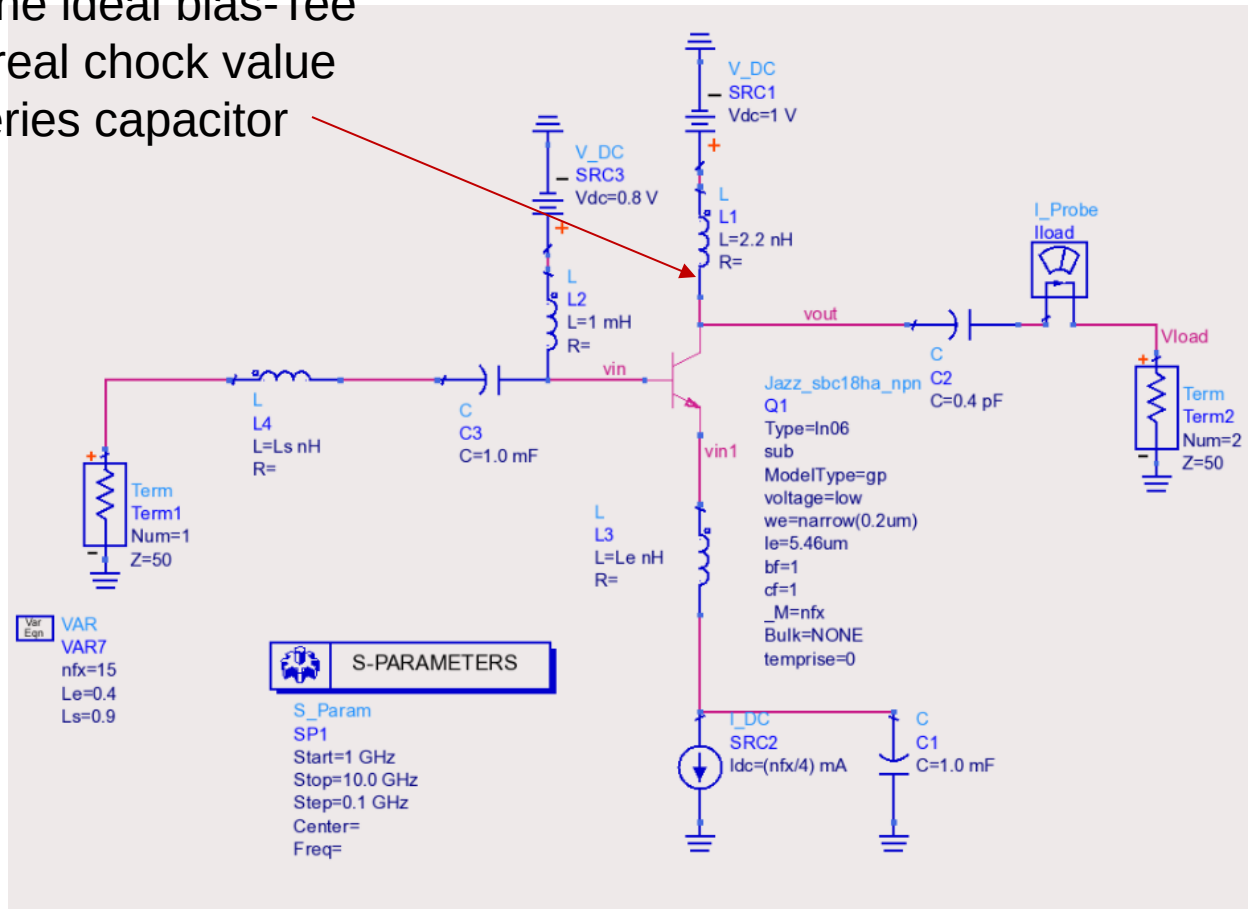


- Size the series capacitor to resonate the imaginary part



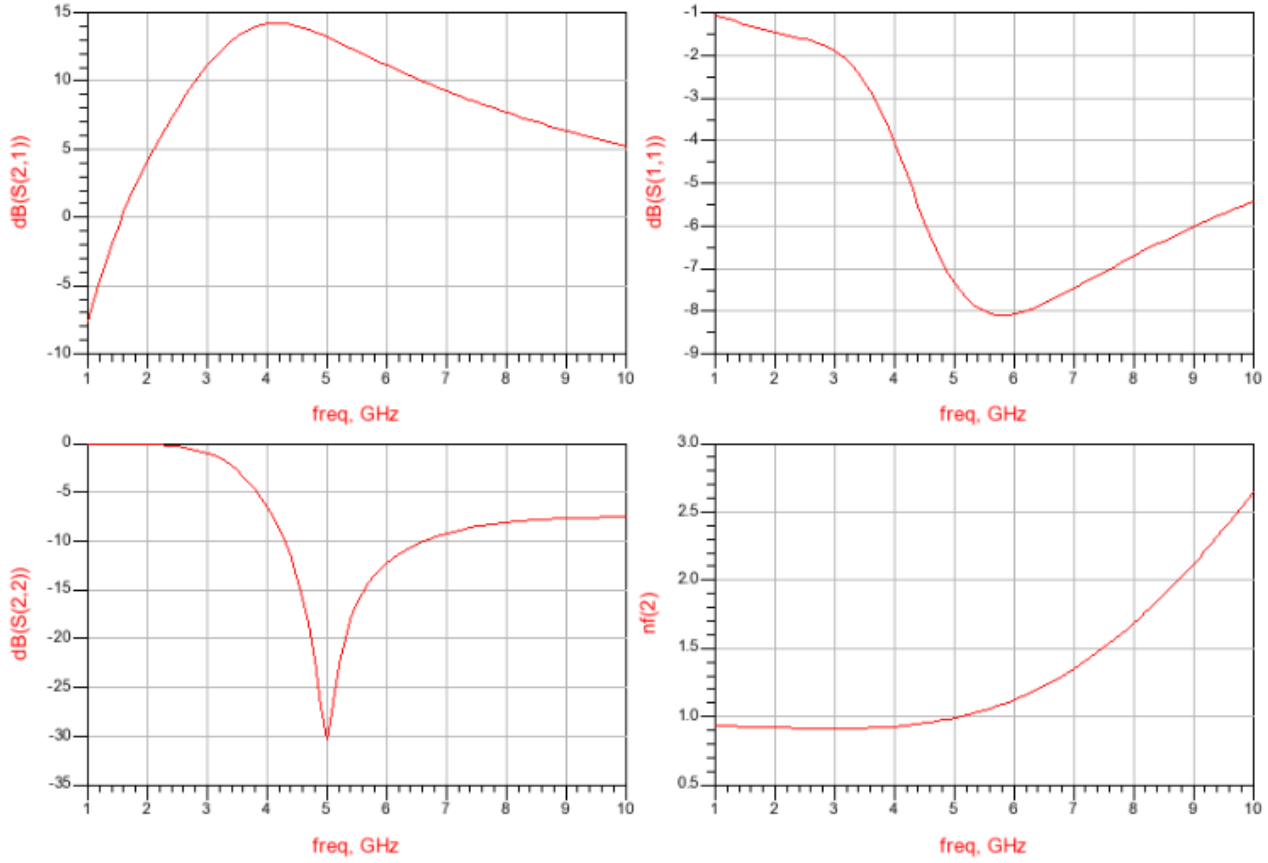
Output Matching

Replace the ideal bias-Tee with the real chock value and series capacitor



Initial LNA Response

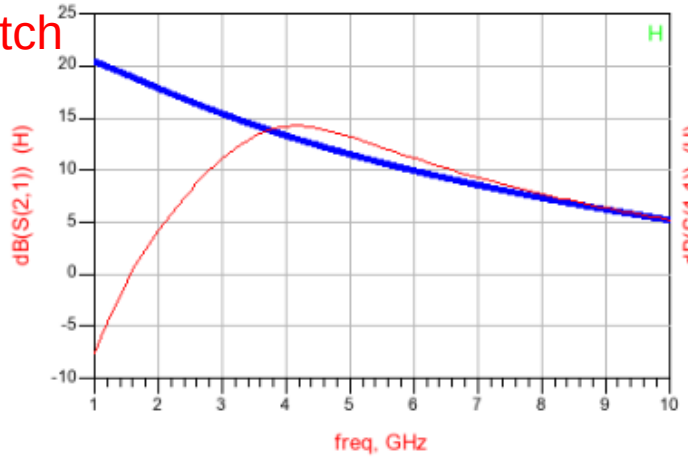
The output is matched but the input has been affected. Why?
Is the output really decoupled from the input?

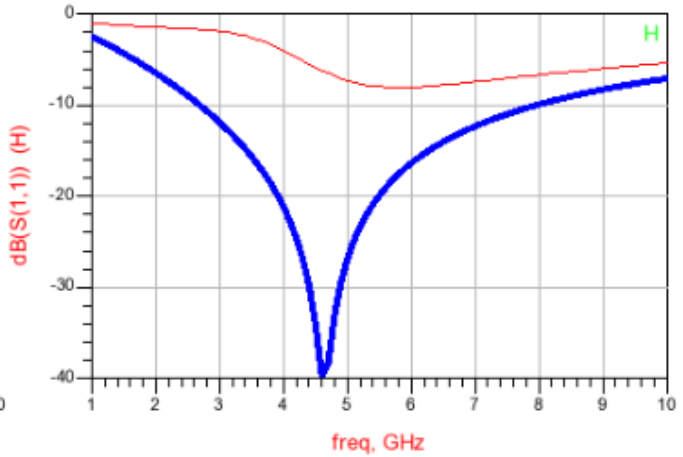


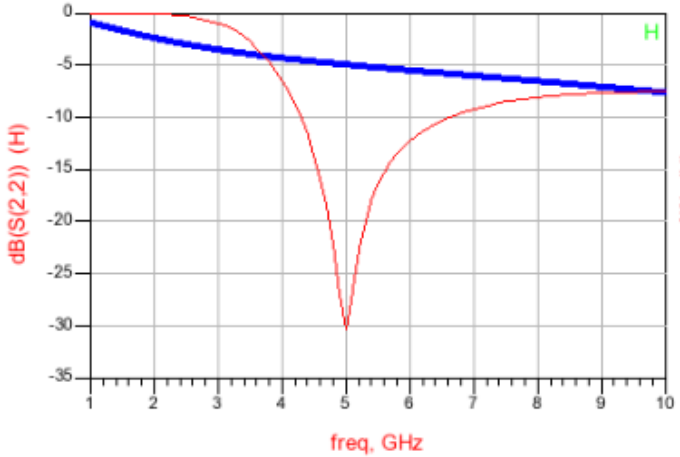
Before and After the O/P match

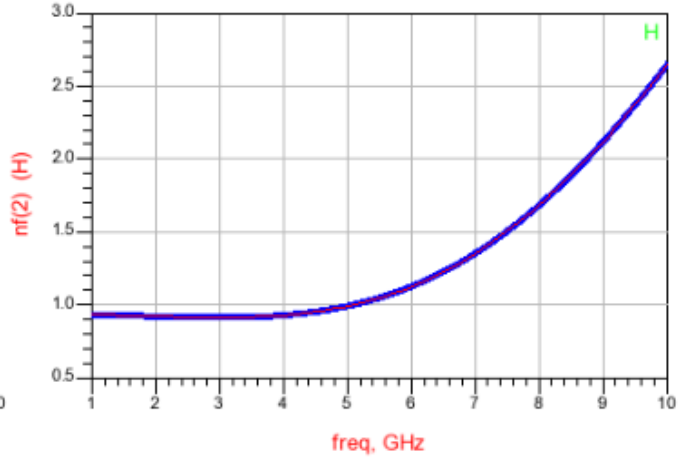
Before output match

After output match

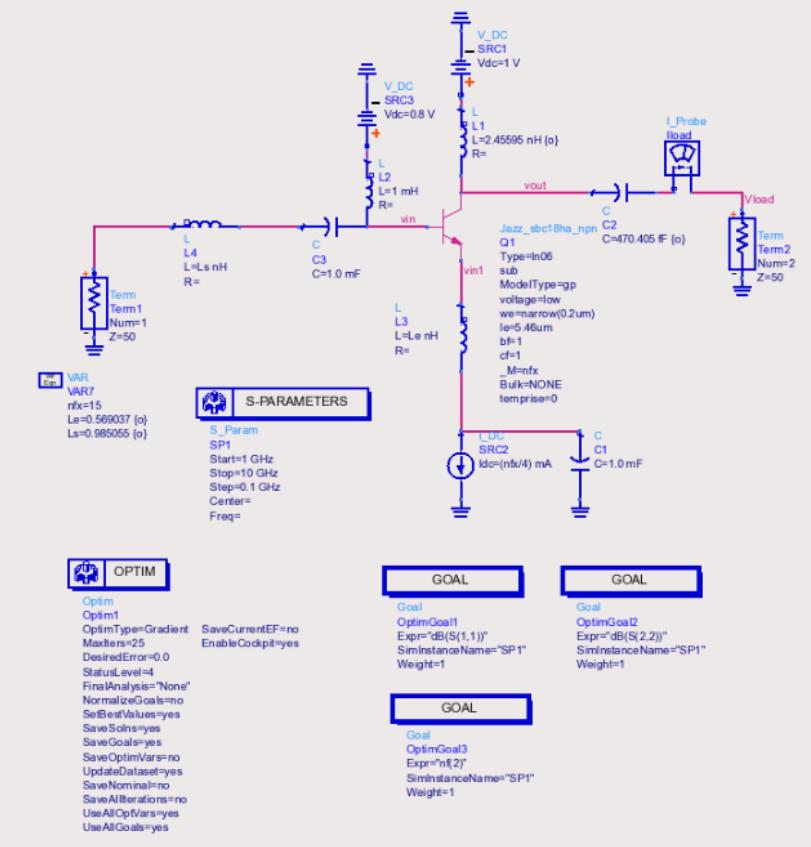








Optimize the design

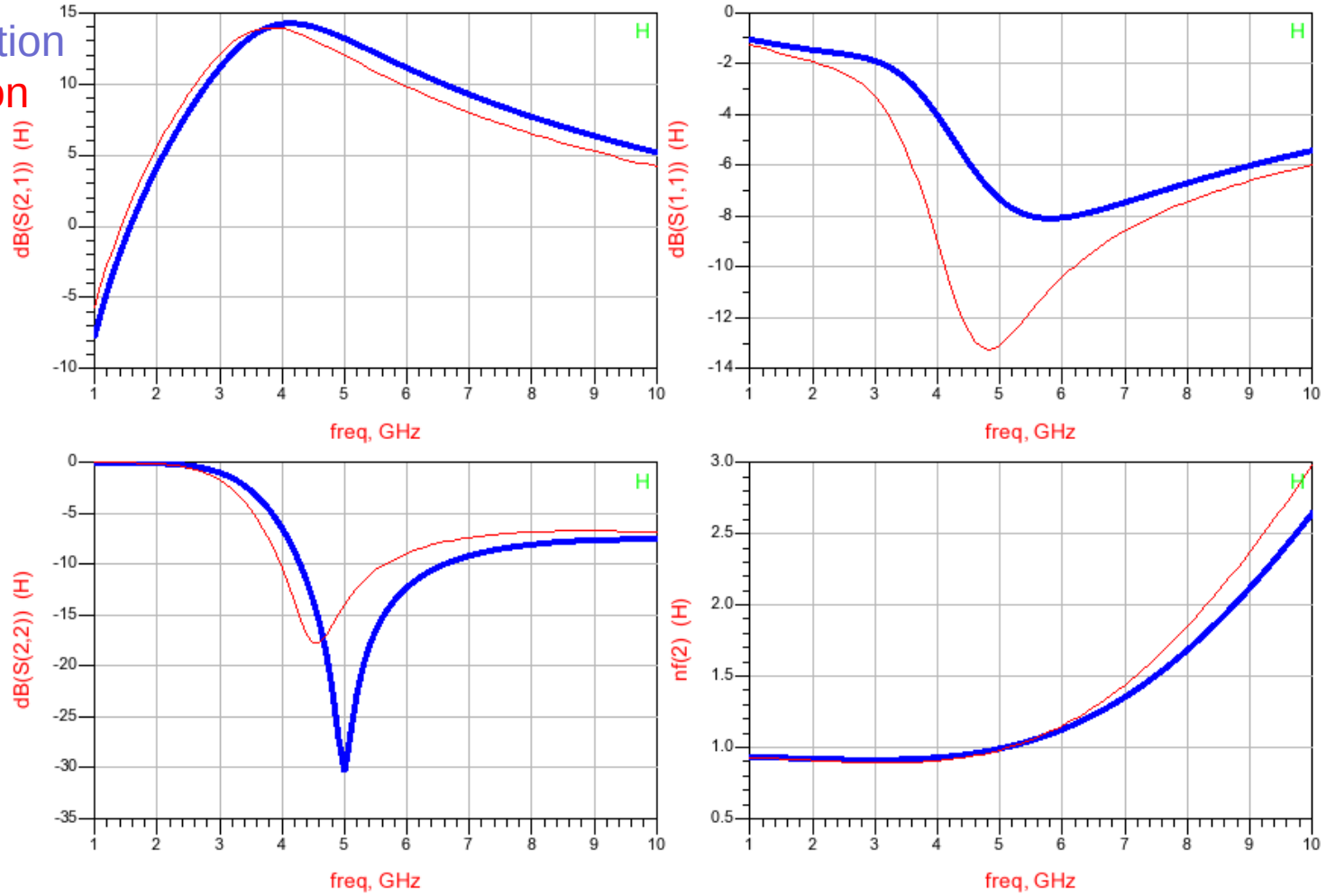


- After reaching the preliminary design ADS optimizer can be used to tweak the passive components & device current/size to improve the LNA results
- Goals can be set on NF, S_{11}, S_{22}, & S_{21}

Before and after optimization

Before optimization

After optimization



Design Steps for Cascoded CS with L_{M1}

1. Set the bias to the optimum NF_{MIN} current density (J_{OPT})
2. Choose the optimal W_f to minimize NF_{MIN}
3. Find the best L_M value for the cascode biased at J_{OPT} by plotting the f_T of the cascode versus L_M
4. With all devices biased at J_{OPT}, scale the number of fingers (N), and L_M to match R_{SOPT} to Z_o
5. Find L_S to match re{Z_{in}}
6. Add L_G to tune out Im{Z_{IN}} and Im{Z_{SOPT}}
7. Add output matching network to maximize gain