CMOS Low-Noise Amplifier Design Optimization Techniques

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CMOS Low-Noise Amplifier Design Optimization Techniques

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***Abstract*—This paper reviews and analyzes four reported low-noise amplifier (LNA) design techniques applied to the cascode topology based on CMOS technology: classical noise matching, simultaneous noise and input matching (SNIM), power-constrained noise optimization, and power-constrained simultaneous noise and input matching (PCSNIM) techniques. Very simple and insightful sets of noise parameter expressions are newly introduced for the SNIM and PCSNIM techniques. Based on the noise parameter equations, this paper provides clear understanding of the design principles, fundamental limitations, and advantages of the four reported LNA design techniques so that the designers can get the overall LNA design perspective. As a demonstration for the proposed design principle of the PCSNIM technique, a very low-power folded-cascode LNA is implemented based on 0.25-μm CMOS technology for 900-MHz Zigbee applications. Measurement results show the noise figure of 1.35 dB, power gain of 12 dB, and input third-order intermodulation product of −4 dBm while dissipating 1.6 mA from a 1.25-V supply (0.7 mA for the input NMOS transistor only). The overall behavior of the implemented LNA shows good agreement with theoretical predictions.**

***Index Terms*—CMOS, low-noise amplifier (LNA), low power, low voltage, noise optimization, RF, Zigbee.**

I. Introduction

CMOS HAS become a competitive technology for radio transceiver implementation of various wireless communication systems due to the technology scaling, higher level of integrability, lower cost, etc. [1], [2]. In a typical radio receiver, the low-noise amplifier (LNA) is one of the key components, as it tends to dominate the sensitivity. The LNA design involves many tradeoffs between noise figure (NF), gain, linearity, impedance matching, and power dissipation [3]. Generally, the main goal of LNA design is to achieve simultaneous noise and input matching (SNIM) at any given amount of power dissipation. A number of LNA design techniques have been reported to satisfy these goals. To name a few representatives: the classical noise matching (CNM) technique [4], SNIM technique [5], power-constrained noise optimization (PCNO) technique [6], and power-constrained simultaneous noise and input matching (PCSNIM) technique [7]. However, these previously reported works describe only one of these techniques and the analysis approaches tend to be inconsistent with each other. The goal of this paper is to analyze the four LNA design techniques based on the noise parameter expressions and try to provide consistent and perspective understanding of CMOS-based LNA design techniques. Section II-A summarizes the reported analytic details of the CNM technique based on the noise parameter expressions and points out the limitations. In Section II-B, the noise parameter expressions of the SNIM technique are newly introduced, and the LNA design principles, as well as the limitations, are discussed. Section II-C summarizes the key concept and limitations of the PCNO technique described in [6]. In Section II-D, the noise parameter expressions of the PCSNIM technique are newly introduced, and the LNA design principles, potential as low-power LNAs, and practical limitations are explained. Section III describes the design and measurement details of a very low-power LNA following the design guidelines provided in Section II-D based on 0.25-μm CMOS technology. Section IV concludes this study.

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II. Noise Optimization Techniques

A. CNM Technique

The CNM technique was reported in [4]. In this technique, the LNA is designed for minimum NF $F_{\min}$ by presenting the optimum noise impedance Z_{opt} to the given amplifier, which is typically implemented by adding a matching circuit between the source and input of the amplifier. By using this technique, the LNA can be designed to achieve an NF equal to $F_{\min}$ of the transistor, the lowest NF that can be obtained with the given technology. However, due to the inherent mismatch between Z_{opt} and Z_{in}^* (where Z_{in}^* is the complex conjugate of the amplifier input impedance), the amplifier can experience a significant gain mismatch at the input. Therefore, the CNM technique typically requires compromise between the gain and noise performance.

Fig. 1(a) shows a cascode-type LNA topology, which is one of the most popular topology due to its wide bandwidth, high gain, and high reverse isolation. In the given example, the selection of the cascode topology simplifies the analysis, and the gate–drain capacitance can be neglected.

Fig. 1(b) shows the simplified small-signal equivalent circuit of the cascode amplifier for the noise analysis including the intrinsic transistor noise model. In Fig. 1(b), the effects of the common-gate transistor M_2 on the noise and frequency response are neglected [3], [8], as well as the parasitic resistances of gate, body, source, and drain terminal.

In Fig. 1(b), $\overline{i_{nd}^2}$ represents the mean-squared channel thermal noise current, which is given by [9]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \quad (1)$$

Why M_2 is neglected in noise analysis?

Due To Friz law The First block or First Device will hold most of The noise contribution so we neglect Them. because M_1 generally have large $\frac{g_m}{g_{ds}}$ so The noise of M_2 reffered To The Input & Divided by M_1 gain $\Rightarrow$ can be neglected

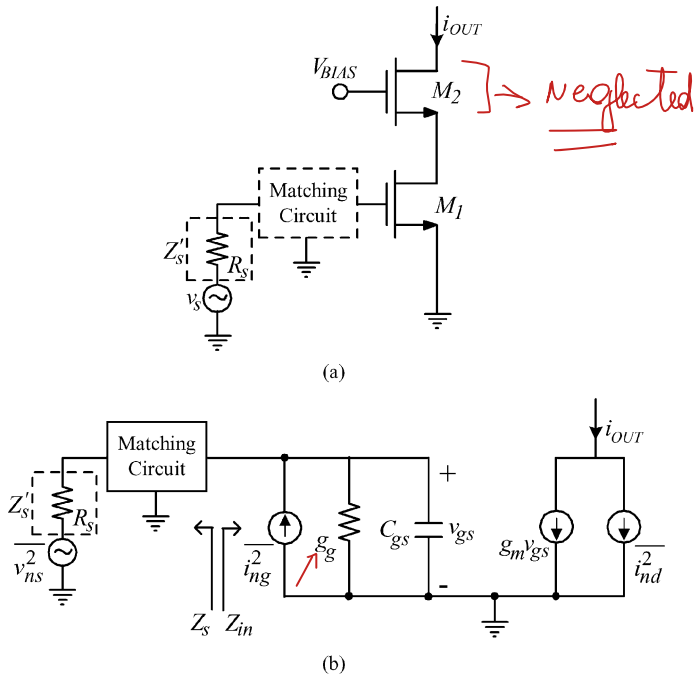

Fig. 1. (a) Schematic of a cascode LNA topology adopted to apply the CNM technique. (b) Its small-signal equivalent circuit.

where g_{do} is the drain–source conductance at zero drain–source voltage $V_{\rm DS}$, k is the Boltzmann constant, T is the absolute temperature, and Δf is the bandwidth, respectively. The parameter γ has a value of unity at zero $V_{\rm DS}$ and 2/3 in saturation mode operation with long channel devices. The value of γ increases at high $V_{\rm GS}$ and $V_{\rm DS}$ and can be more than two in short-channel devices.

The fluctuating channel potential due to the channel noise current shown in (1) couples capacitively into the gate terminal, leading to a noisy gate current. As in [9], the mean-squared gate-induced noise current is given by

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{2}$$

where

$$g_g = \frac{\omega^2 C_{\rm gs}^2}{5 g_{d0}}. \tag{3}$$

In (2), δ is a constant with value of 4/3 in long-channel devices, and $C_{\rm gs}$ represents the gate–source capacitance of the input transistor. Like γ, the value of δ also increases in short-channel devices and at high $V_{\rm GS}$ and $V_{\rm DS}$. Since the gate-induced noise current has a correlation with the channel noise current, a correlation coefficient is defined as follows [9]:

$$c \equiv \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}} \cdot \sqrt{\overline{i_{nd}^2}}}. \tag{4}$$

With long channel devices, c can be predicted theoretically as $j0.395$ [9]. The value of c is purely imaginary, reflecting the capacitive coupling between the channel and gate-induced noise sources. After some lengthy algebraic derivations [3], the noise parameters for the cascode amplifier shown in Fig. 1(a) can be expressed as

$$R_n^o = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{5}$$

$$Y_{\rm opt}^o = \alpha\omega C_{\rm gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} - sC_{\rm gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{6}$$

$$F_{\rm min}^o = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \tag{7}$$

where R_n^o represents the noise resistance, $Y_{\rm opt}^o$ is the optimum noise admittance, and $F_{\rm min}^o$ is the minimum noise factor, respectively. In (7), the cutoff frequency ω_T is equal to $g_m/C_{\rm gs}$, and $\alpha \equiv g_m/g_{do}$ is unity for long-channel devices and decreases as channel length scales down. In (5)–(7), the superscripted zero is adopted as a differentiation with other cases.

Note that, from Fig. 1(b), the input admittance is purely capacitive, i.e., $Y_{\rm in}^o = j\omega C_{\rm gs}$. By comparing the complex conjugate of $Y_{\rm in}^o$ with (6), it can be seen that the optimum source admittance for input matching is inherently different from that of the noise matching in both real and imaginary parts. Thus, with the given example, one cannot obtain both input matching and minimum NF simultaneously. This is the main limitation of the CNM technique when applied to the LNA topology shown in Fig. 1(a). Note that the imaginary component of (6) is inductive, but the frequency response is like that of a capacitor. Hence, there is a fundamental limitation in achieving broad-band noise matching.

B. SNIM Technique

Feedback techniques are often adopted in designing low-noise amplifiers in order to shift the optimum noise impedance $Z_{\rm opt}$ to the desired point. Parallel feedback has been applied for wide-band [10]–[12] and better input/output matching [13]. Series feedback has been preferred to obtain SNIM without the degradation of the NF [14]–[17]. The series feedback with inductive source degeneration, which is applied to the common-source or cascode topology, is especially widely used for narrow-band applications [5], [18]–[24].

Fig. 2(a) and (b) shows a cascode LNA with inductive source degeneration and the simplified small-signal equivalent circuit.

In Fig. 2(b), the same simplifications are applied as in Fig. 1(b). The following are the ways to obtain the noise parameter expressions of a MOSFET with series feedback: noise transformation formula using noise parameters [25], using the noise matrix [26], [27], or Kirchoff's current law/Kirchoff's voltage law (KCL/KVL) with noise current sources [3], [6]. As in (5)–(7), the noise parameters seen in the gate of the circuit shown in Fig. 2(b) can be obtained. The procedures described in [3] and [6] are used in this study. The derivation is somewhat tedious, but the result is simple enough to provide useful insights. The detailed derivations are summarized in the Appendix assuming the inductors are lossless. In the Appendix , to simply the derivation, it is assumed that the matching circuit is implemented by a series inductor L_g, and

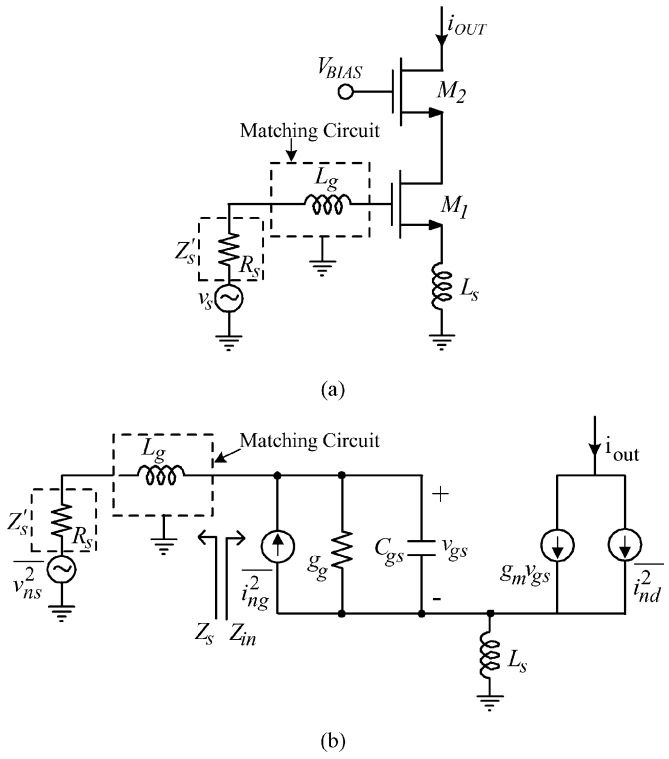

Fig. 2. (a) Schematic of a cascode LNA topology adopted to apply the SNIM technique. (b) Its small-signal equivalent circuit.

$Z_s' = R_s$. As shown in the Appendix, the noise factor and noise parameters can be given by

$$F = 1 + \frac{1}{g_m^2 R_s} \cdot \left\{ \gamma g_{d0} \cdot \left\{ \left[1 + s^2 C_{\rm gs}(L_g + L_s) \left(1 + |c|\alpha \sqrt{\frac{\delta}{5\gamma}} \right) \right]^2 - (sC_{\rm gs}R_s)^2 \left(1 + |c|\alpha \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\} - \frac{\alpha\delta}{5} \left(1 - |c|^2\right) g_m \left(sC_{\rm gs}\right)^2 \left(R_s^2 - sL_g^2\right) \right\} \quad (8)$$

$$R_n = R_n^o = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \quad (9)$$

$$Z_{\rm opt} = Z_{\rm opt}^o - sL_s \quad (10)$$

$$F_{\rm min} = F_{\rm min}^o = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta\left(1 - |c|^2\right)}. \quad (11)$$

In (9)–(11), the noise parameters with superscripted zeros are those of the cascode amplifier with no degeneration [see (5)–(7)]. Note that (10) is expressed in impedance, as it is simpler in this case, and $Z_{\rm opt}^o$ is given by

$$Z_{\rm opt}^o = \frac{1}{Y_{\rm opt}^o} = \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma\left(1-|c|^2\right)}} + j\left(1 + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{\rm gs}\left\{ \dfrac{\alpha^2\delta}{5\gamma\left(1-|c|^2\right)} + \left(1 + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2 \right\}}. \quad (12)$$

Note that, from (9)–(11), only $Z_{\rm opt}$ is shifted and there is no change in R_n and $F_{\rm min}$. Also, note that (9)–(11) are valid for any arbitrary matching circuits, as well as the source impedance Z_S' in Fig. 2. In addition, as shown in Fig. 2(b), the input impedance $Z_{\rm in}$ of the given LNA can be expressed as

$$Z_{\rm in} = sL_s + \frac{1}{sC_{\rm gs}} + \frac{g_m L_s}{C_{\rm gs}} = sL_s + \frac{1}{sC_{\rm gs}} + \omega_T L_s. \quad (13)$$

As can be seen from (13), the source degeneration generates the real part at the input impedance. This is important because there is no real part in $Z_{\rm in}$ without degeneration, while there is in $Z_{\rm opt}$. Therefore, if not excessive, L_s helps to reduce the discrepancy between the real parts of $Z_{\rm opt}$ and $Z_{\rm in}$ of the LNA. Furthermore, from (13), the imaginary part of $Z_{\rm in}$ is changed by sL_s, and this is followed by the same change in $Z_{\rm opt}$, as shown in (10). From (12), (10) can be re-expressed as

$$Z_{\rm opt} = {\rm Re}\left[Z_{\rm opt}^o\right] - m\frac{1}{sC_{\rm gs}} - sL_s \quad (14)$$

where the constant m, for the typical device parameters of long-channel MOSFETs, is approximately equal to 0.6. With technology scaling, the ratio δ/γ stays nearly constant at 2 [3], [9], α becomes lower than 1 [28], and c is slightly higher than 0.4 (e.g., $c \approx 0.5$ with 0.25-μm technology [29]), such that the constant m is expected to become closer to 1. Therefore, from (13) and (14), it can be seen that the inductive source degeneration helps to bring the $Z_{\rm opt}$ point close to the optimum source impedance point $Z_{\rm in}^*$ while causing no degradation in $F_{\rm min}$ and R_n. This characteristic reveals the potential for the SNIM technique.

For the circuit shown in Fig. 2(a), the condition that allows the SNIM is

$$Z_{\rm opt} = Z_{\rm in}^*. \quad (15)$$

From (9)–(11), and (13), the conditions that satisfy (15) and the matching with the source impedance Z_s are as follows:

$${\rm Re}[Z_{\rm opt}] = {\rm Re}[Z_s] \quad (16)$$

$${\rm Im}[Z_{\rm opt}] = {\rm Im}[Z_s] \quad (17)$$

$${\rm Im}[Z_{\rm in}] = -{\rm Im}[Z_s] \quad (18)$$

$${\rm Re}[Z_{\rm in}] = {\rm Re}[Z_s]. \quad (19)$$

As described above, based on (13) and (14), (17) and (18) are the same, especially in advanced technology. Therefore,(18) should be dropped considering the importance of the noise performance. Some amount of mismatch in the input matching has a negligible effect on the LNA performance, while the mismatch in $Z_{\rm opt}$ directly affects the NF. Now then, from (9)–(13), the design parameters that can satisfy (16), (17), and (19) are $V_{\rm GS}$, the transistor size W (or $C_{\rm gs}$), and L_s. Minimum gate length is assumed to maximize the transistor cutoff frequency ω_T. Therefore, for the given value of Z_s, (16), (17), and (19) can be solved since three effective equations are provided with three unknowns.

Qualitatively, the LNA design based on the SNIM technique can be explained as follows. Following (10), (12), and (16), for an arbitrary signal source impedance Z_s, choose a transistor size ($C_{\rm gs}$), which satisfies ${\rm Re}[Z_{\rm opt}] = {\rm Re}[Z_s]$. For the given transistor size $C_{\rm gs}$, choose the degeneration inductor size L_s

that satisfies (17), $\mathrm{Im}[Z_{\mathrm{opt}}] = -\mathrm{Im}[Z_s]$. For the given values of C_{gs} and L_s, the value of V_{GS} can then be determined from (19), $\mathrm{Re}[Z_{\mathrm{in}}] = \mathrm{Re}[Z_s]$. Note that, as discussed above, for the given L_s, the imaginary value of the optimum noise impedance would automatically be approximately equal to that of the input impedance with an opposite sign $\mathrm{Im}[Z_{\mathrm{in}}] \approx -\mathrm{Im}[Z_s]$. Now, from Fig. 2(b), if $Z_s = Z_s'$, then the SNIM is achieved to the signal source impedance. If not, the matching circuit shown in Fig. 2 should be added. The design methodology described above guarantees the NF of the LNA equal to F_{min} of the common-source transistor with nearly perfect input impedance matching.

The above LNA design technique suggests that, by the addition of L_s, in principle, the SNIM can be achieved at any values of Z_s by satisfying (16), (17), and (19) assuming (9)–(11) are valid. Many cases, especially those with large transistor size, high power dissipation, and high frequency of operation [i.e., (16), (17), and (19)] can be satisfied without much difficulty, while (9)–(11) stay valid. The problem occurs when the transistor size is small (hence, the power dissipation is small) and the LNA operates at low frequencies. Equation (12) indicates that the small transistor size and/or low frequency leads to high value of $\mathrm{Re}[Z_{\mathrm{opt}}]$. Therefore, from (13), for the given bias point or ω_T, the degeneration inductor L_s has to be very large to satisfy (19). The problem is that for the L_s to be greater than some value, (11) becomes invalid and F_{min} increases significantly [30]. As a result, the minimum achievable NF of the LNA can be considerably higher than F_{min} of the common-source transistor, spoiling the idea of SNIM. In other words, the SNIM technique is not applicable for the transistor sizes and bias levels (or the power dissipation levels) as $\mathrm{Re}[Z_{\mathrm{opt}}]$ becomes greater than $\mathrm{Re}[Z_{\mathrm{in}}]$ for the value of L_s, which does not degrade the F_{min} of the LNA. The inaccuracy of (11) for large L_s might be caused by the negligence of C_{gd}. With large L_s, the transconductance of the common-source stage can degrade significantly and the feedback signal through C_{gd} could become nonnegligible. As a practical design technique, the minimum value of L_s, which does not degrade F_{min}, can be identified by monitoring the F_{min} of the LNA as a function of L_s in simulation.

Note that, from (13), even with a small transistor, low power, and low frequency, input matching can still be satisfied by proper selection of the degeneration inductance. It was found that, for the small amount of power dissipation where the SNIM technique is not applicable, there exists an optimum transistor size that provides a minimum NF while satisfying input matching [6]. However, the achievable minimum NF is higher than F_{min} of the common-source transistor. This power-constrained LNA optimization technique is the subject of the topic that will be discussed in Section II-C.

C. PCNO Technique

With a constrained amount of power dissipation, the simultaneous gain and noise matching approach can still be useful. At any given amount of power dissipation, (18) and (19) can be satisfied by the proper selection of L_s for the given C_{gs} with the help of the matching circuit shown in Fig. 2, which is typically implemented by a series inductance L_g. It can be shown that, under fixed drain current and while satisfying (18) and (19),

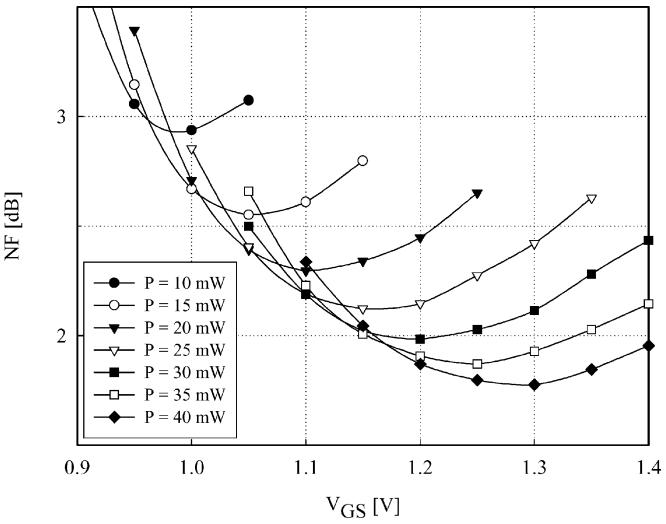

Fig. 3. Simulated NF of a cascode LNA with inducting degeneration as function of power dissipation and transistor size. A 0.8-μm high-resistivity-substrate CMOS technology is used for the simulation at 2 GHz.

there exists a transistor size where the NF of the amplifier becomes minimum [6]. From [3], this optimum transistor size is given by

$$W_{\mathrm{opt}} \approx \frac{1}{3\omega C_{\mathrm{ox}} R_s Q_{\mathrm{in,opt}}} \tag{20}$$

where

$$Q_{\mathrm{in,opt}} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|c|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right]. \tag{21}$$

In (20), C_{ox} represents the gate–oxide capacitance of the MOSFET per unit area. The minimum NF in this case $F_{\mathrm{min}\,P}$ can be given by [3]

$$F_{\mathrm{min}\,P} \approx 1 + 2.4\frac{\gamma}{\alpha}\left[\frac{\omega}{\omega_T}\right]. \tag{22}$$

As described in [3], $F_{\mathrm{min}\,P}$ is higher than F_{min}, the minimum NF of the common-source transistor. The reason for $F_{\mathrm{min}\,P} > F_{\mathrm{min}}$ is due to the mismatch between Z_s and Z_{opt} and/or the high values of L_s, which leads to higher F_{min}, as discussed previously. Fig. 3 shows the NF of a cascoded LNA with inductive degeneration as a function of power dissipation and transistor size. In Fig. 3, the simulation is done at 2 GHz based on a 0.8-μm high-resistivity-substrate CMOS technology and the inductors are assumed ideal. As can be seen in Fig. 3, at each level of power dissipation, there exists a transistor size that provides a minimum NF. The PCNO technique will eventually converge to the SNIM technique as the power dissipation increases and, therefore, satisfies (16), (17), and (19).

D. PCSNIM Technique

As described in Sections II-B and C, the SNIM and PCNO techniques do not allow SNIM at low-power implementations. However, the need for low-power implementation of a radio transceiver is one of the inevitable technical trends. Fig. 4(a) shows a cascoded amplifier topology that can satisfy the SNIM at low power. Note that the difference in Fig. 4(a) compared to the LNA shown in Fig. 2(a) is one additional capacitor C_{ex}.

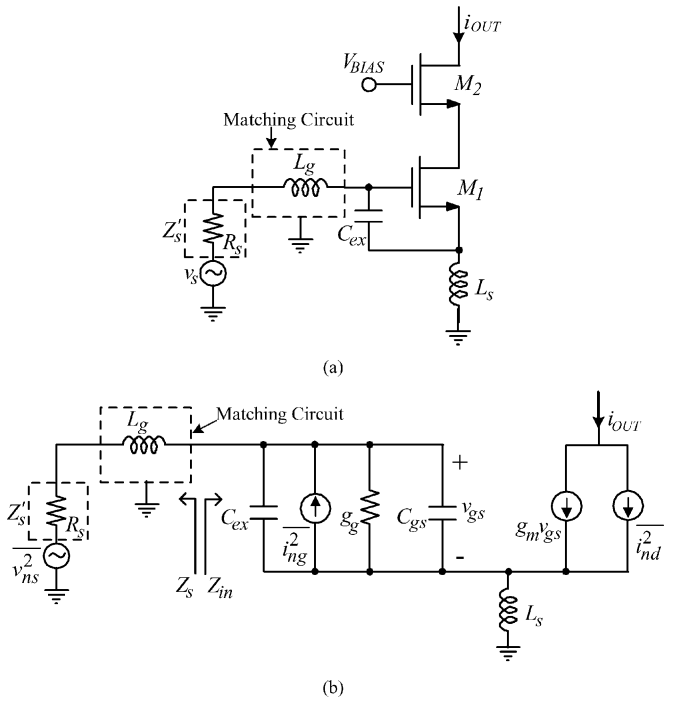

Fig. 4. (a) Schematic of a cascode LNA topology adopted to apply the PCSNIM technique. (b) Its small-signal equivalent circuit.

Fig. 4(b) shows the simplified small-signal equivalent circuit of Fig. 4(a). Again, in Fig. 4(b), the same simplifications are applied as in Figs. 1(b) and 2(b). For the given small-signal circuit shown in Fig. 4(b), following a similar approach as described in the Appendix , rather simple sets of noise parameter equations can be derived by replacing (2) with the following expression:

$$\overline{i_{ng}^2} = 4kT\delta_{\text{eff}}\frac{\omega^2 C_t^2}{5g_{do}}\Delta f \tag{23}$$

where $\delta_{\text{eff}} = \delta.\left(C_{\text{gs}}^2/C_t^2\right)$ and $C_t = C_{\text{gs}} + C_{\text{ex}}$. Equation (23) is the same expression as (2), but is just rewritten for simpler mathematics. The noise parameters can be given by

$$R_n = \frac{\gamma}{\alpha}\cdot\frac{1}{g_m} \tag{24}$$

$$Z_{\text{opt}} = \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}} + j\left(\dfrac{C_t}{C_{\text{gs}}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{\text{gs}}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{\text{gs}}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} - sL_s \tag{25}$$

$$F_{\min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)}. \tag{26}$$

Interestingly, as can be seen from (24) and (26), the noise resistance R_n and minimum NF $F_{\min}$ are not affected by the addition of C_{ex}, which is the same as the cases shown in Figs. 1 and 2. From Fig. 4(b), the input impedance of the LNA can be given by

$$Z_{\text{in}} = sL_s + \frac{1}{sC_t} + \frac{g_m L_s}{C_t}. \tag{27}$$

It can now be seen that the (24)–(27) are similar to (9)–(11) and (13). As discussed in Section II-B, (24)–(26) are valid for rather small values of L_s.

As with the LNA topology shown in Fig. 2(a), for the SNIM of the circuit shown in Fig. 4(a), (15) now needs to be satisfied, and that means that the conditions shown in (16)–(19) should be satisfied. From (25) and (27), (16)–(19) can be re-expressed as follows:

$$\frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}}}{\omega C_{\text{gs}}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{\text{gs}}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} = \text{Re}[Z_s] \tag{28}$$

$$\frac{j\left(\dfrac{C_t}{C_{\text{gs}}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{\text{gs}}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{\text{gs}}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} - sL_s = \text{Im}[Z_s] \tag{29}$$

$$sL_s + \frac{1}{sC_t} = -\text{Im}[Z_s] \tag{30}$$

$$\frac{g_m L_s}{C_t} = \text{Re}[Z_s]. \tag{31}$$

As discussed in Section II-B, for the typical values of advanced CMOS technology parameters, (29) is approximately equal to (30). Therefore, (30) can be dropped, which means that, as in Section II-B, for the given value of L_s, the imaginary value of the optimum noise impedance becomes approximately equal to that of the input impedance with an opposite sign $\text{Im}[Z_{\text{in}}] \approx -\text{Im}[Z_s]$ automatically. The design parameters that can satisfy (28), (29), and (31) are V_{GS}, W (or C_{gs}), L_s, and C_{ex}. Since there are three equations and four unknowns, (28), (29), and (31) can be solved for an arbitrary value of Z_s by fixing the value of one of the design parameters. Therefore, in the PCSNIM LNA design technique, by the addition of an extra capacitor C_{ex}, the SNIM can be achieved at any level of power dissipation.

Note that, like the case of the SNIM technique, (24)–(26) are derived assuming L_s is not very large. The validity of this assumption in a low-power LNA can be investigated. From (28) and (31), the following approximated relation can be made:

$$L_s \approx \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}}}{\omega\omega_T C_t}. \tag{32}$$

Equation (32) indicates that L_s is a function of C_t and ω_T (which is a function of V_{GS}). In comparison, for the SNIM tech-

nique, a similar relation can be obtained from (10), (14), (16), and (19) as

$$L_s \approx \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma\left(1-|c|^2\right)}}}{\omega\omega_T C_{\rm gs}}. \tag{33}$$

By comparing (32) and (33), it can be seen that, in the PCSNIM technique applied for the low-power design, where $C_{\rm gs}$ is small, the required degeneration inductance L_s can be reduced by the addition of $C_{\rm ex}$. In fact, by applying the PCSNIM technique to the SNIM technique-based LNA, the required degeneration inductance L_s can be reduced below what the SNIM technique requires.

The qualitative description of the PCSNIM design process would be as follows.

First, choose the dc-bias $V_{\rm GS}$, for example, the bias point that provides minimum $F_{\rm min}$. Second, choose the transistor size W based on the power constraint P_D. Third, choose the additional capacitance $C_{\rm ex}$, as well as the degeneration inductance L_s to satisfy (28) and (31) simultaneously. The value of $C_{\rm ex}$ should be chosen considering the compromise between the size of L_s and the available power gain. As described before, too much L_s can lead to the increase in $F_{\rm min}$, while large $C_{\rm ex}$ leads to the gain reduction due to the degradation of the effective cutoff frequency of the composite transistor (transistor including $C_{\rm ex}$). Note that, as discussed above, for the given L_s, the imaginary value of the optimum noise impedance would automatically equal that of the input impedance with an opposite sign $\Im[Z_{rmin}] \approx -\Im[Z_s]$. At this point, the SNIM is achieved. As the last step, if there exists any mismatch between $Z_{\rm in}$ and Z_s', as shown in Fig. 4(b), an impedance matching circuit can be added.

The limitation of the PCSIM technique is the high value of noise resistance. From (24), the noise resistance R_n of the proposed topology is not affected by the addition of $C_{\rm ex}$, but depends only on the value of g_m. Therefore, the small transistor size and low-power dissipation can lead to very high R_n. High R_n can be a serious limitation for the practical high-yield LNA design. Fig. 5 shows the simulated NF and input return loss S_{11} as a function of frequency for the LNA topology shown in Fig. 4(a) for three transistor sizes. In Fig. 5, the simulation is based on 0.25-μm CMOS technology with the supply voltage of 1.25 V. The amount of power dissipation is varied by changing the transistor size, which leads to the supply current of 1.6, 4.8, and 9.6 mA for a given value of gate–source voltage. As can be seen in Fig. 5, in addition to good input matching, for all power levels, the NF of the designed LNAs coincides with the $F_{\rm min}$ of the transistor at the frequency of interest. Note that, as explained above, with reduction in the amount of power dissipation (smaller transistor size), due to the larger R_n, the NF of LNAs increases sharply at the frequencies away from the optimum point.

Considering the relationship between the cutoff frequency (f_T) and the total input capacitance, the addition of $C_{\rm ex}$ leads to power-gain degradation. For example, if $C_{\rm ex} = 3C_{\rm gs}$, the f_T of the LNA is expected to be reduced by a factor of four. This would lead to the reduction of the maximum oscillation frequency ($f_{\rm max}$) by the factor of $\sqrt{2}$, 71%, due to the square-root functional dependence of $f_{\rm max}$ on f_T. Therefore, it could be considered that the power gain is a slow function of $C_{\rm ex}$. From the simulation of the case shown in Fig. 5, the maximum available gain of the LNA is degraded by 1 dB for $C_{\rm ex} = 1.5C_{\rm gs}$ at 900 MHz.

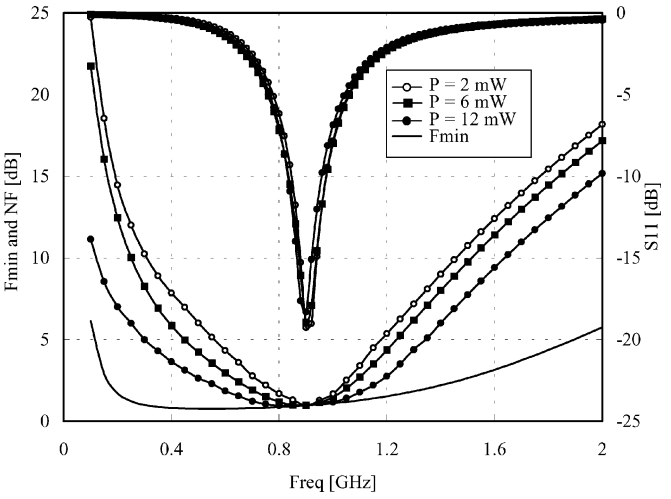

Fig. 5. Simulated NF, $F_{\rm min}$, and S_{11} of the LNA shown in Fig. 4 following the PCSNIM technique as a function of frequency. The simulation includes LNA design for three levels of power dissipation based on 0.25-μm CMOS technology.

TABLE I
SUMMARY OF THE CHARACTERISTICS FOR THE FOUR LNA DESIGN TECHNIQUES

Parameters	CNM [4]	SNIM [5]	PCNO [6]	PCSNIM [7]
Power-Constrained	Yes	Yes, at rather high power dissipation	Yes	Yes
Input matching	Typically No	Yes	Yes	Yes
NF = F_{min}	Yes	Yes	Mostly no	Yes

Table I summarizes and compares the advantages and disadvantages of the four LNA design techniques discussed in Section II. As can be seen in Table I, the PCSNIM technique offers a new prospect in low-power LNA design.

III. LNA DESIGN

The LNA designs following the CNM, SNIM, and PCNO techniques have been confirmed through fabrications and measurements [30]–[33]. However, none of the measurement results have been reported following the design principles of the PCSNIM technique. Fig. 6 shows a folded-cascode-type LNA topology that is chosen to apply the PCSNIM technique. The LNA shown in Fig. 6 is designed based on 0.25-μm CMOS technology for 900-MHz Zigbee application [34], which requires very low-power dissipation and low supply voltage. In Fig. 6, the folding of the common-gate transistor helps to extend the cutoff frequency of the common-source transistor. Furthermore, the parasitic capacitances at the drain node of the common-source transistor can easily be eliminated by the resonance with the inductance at the supply pin L_d. The elimination or the reduction of this parasitic capacitance helps to suppress the noise contribution of the common-gate transistor at the output and avoid the signal loss into the silicon substrate [32]. In Fig. 6, the size of $C_{\rm ex}$ and L_s are chosen following the design principle of the PCSNIM technique, and L_g is inserted for the input

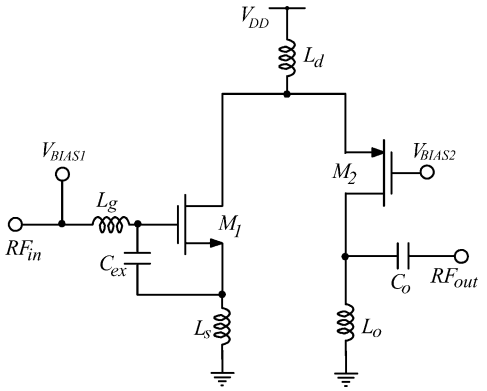

Fig. 6. Schematic of a folded-cascode LNA, which adopts the PCSNIM technique.

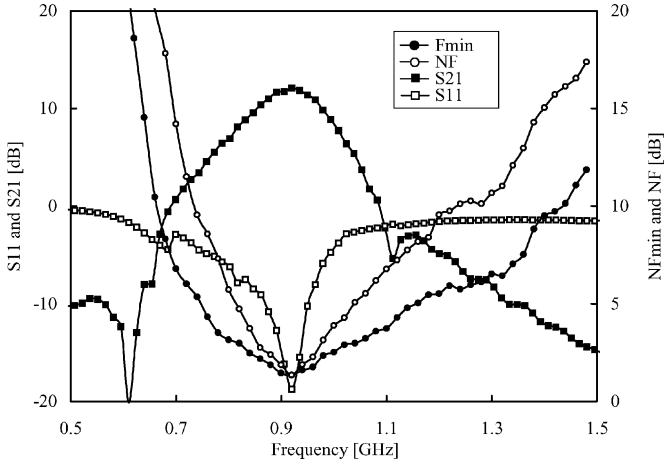

Fig. 7. Measured NF, $F_{\min}$, power gain, and S_{11} of the LNA shown in Fig. 6 as a function of frequency.

matching to the signal source impedance of 50 Ω. In this design, the value of L_d is 33 nH, and L_s is 3.9 nH, which is implemented by combining off-chip inductor and wire bonding. The size of transistor M_1 is 0.25 μm× 160 μm. The values of $C_{\rm ex}$ and L_g are 500 fF and 33 nH, respectively. A simple L-C network using an off-chip inductor L_o and an on-chip capacitor C_o are used to match the output of the LNA. The high-Q and 20-nH off-chip inductor L_o helps to improve the linearity of the LNA [35]. In Fig. 6, the LNA dissipates the total current of 1.6 mA from the supply voltage of 1.25 V where the common-source and common-gate stages consume 0.7 and 0.9 mA, respectively. Considering the linearity, the higher amount of current is allocated at the common-gate stage.

Fig. 7 shows the measurement results of the LNA shown in Fig. 6. As can be seen in Fig. 7, the LNA shows power gain of 12 dB, NF of 1.35 dB, and S_{11} of −18 dB, respectively, at 910 MHz. Note that, in Fig. 7, $F_{\min}$ of the LNA is also shown as a function of frequency, and it can be seen that the NF of the LNA coincides with $F_{\min}$ very well at the frequencies of interest, showing good agreement with what was expected theoretically. From Fig. 5, the simulated NF and S_{11} of the same circuit at 910 MHz are 1.05 dB and −19 dB, respectively. Fig. 8 shows the measured input third-order intermodulation product (IIP3) of −4 dBm and Fig. 9 shows the microphotograph of the

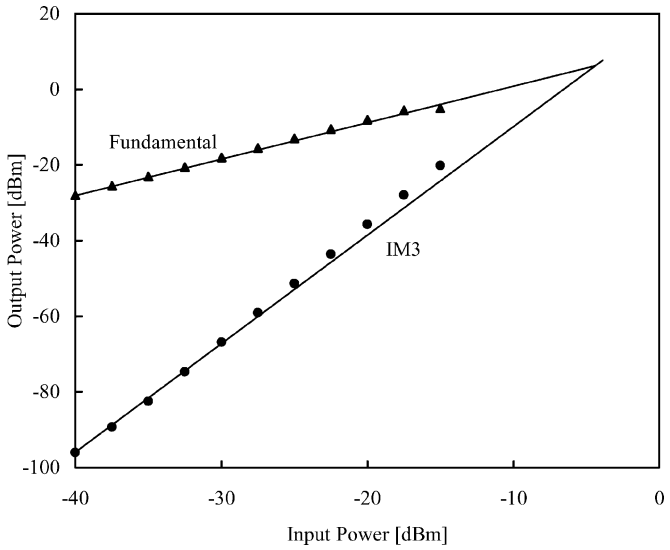

Fig. 8. Measured IIP3 of the LNA shown in Fig. 6.

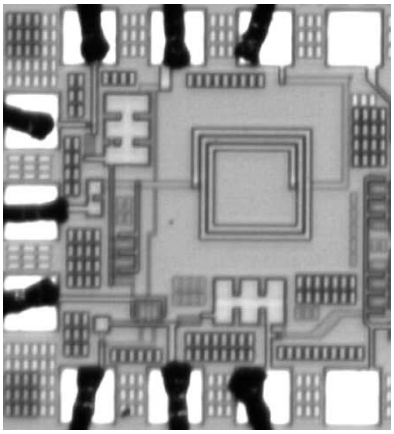

Fig. 9. Microphotograph of the LNA shown in Fig. 6.

TABLE II
SUMMARY OF THE MEASURED 900-MHz LNA PERFORMANCES

Parameters	Values
Operating frequency [MHz]	900
Power Gain [dB]	12
Noise Figure [dB]	1.35
IIP3 [dBm]	-4
Technology [μm]	0.25
Power dissipation [mW]	1.6x1.25

LNA. Table II summarizes the measured performances of the LNA.

IV. CONCLUSION

Four well-known LNA design optimization techniques, i.e., the CNM, SNIM, PCNO, and PCSNIM techniques, have been reviewed and analyzed. Very simple and insightful sets of noise parameter expressions have been newly introduced for the cases of SNIM and PCSNIM techniques. Based on the noise parameter expressions, the design principles, advantages, and limitations of each technique are discussed. With the CNM technique, the LNA can be designed for the minimum NF $F_{\min}$

of the given technology at any given amount of power dissipation. However, the LNA typically experiences inherent input mismatch problems. With the SNIM technique, the condition for the SNIM can be satisfied by the proper selection of the transistor sizes and degeneration inductances. This technique, in principle, can be applied for any levels of power dissipation as long as $\mathrm{Re}[Z_{\mathrm{opt}}] = \mathrm{Re}[Z_{\mathrm{in}}]$ is satisfied and the $F_{\min}$ of the LNA is not degraded by the degeneration inductance. However, with low-power application, the SNIM technique is not useful. With low-power design, the increase in the value of the degeneration inductance to force the condition of $\mathrm{Re}[Z_{\mathrm{opt}}] = \mathrm{Re}[Z_{\mathrm{in}}]$ leads to the degradation of $F_{\min}$. In this situation, the PCNO technique can be applied. The PCNO technique, which is proposed as a low-power LNA design technique, provides an optimum transistor size that can obtain a minimum NF for the given amount of power dissipation. However, with the PCNO technique, the NF of the LNA is higher than the $F_{\min}$ of the LNA. As an alternative, the PCSNIM technique can be used for the low-power design. The PCSNIM technique allows the same performance advantages as the SNIM technique, i.e., SNIM at the power level where the SNIM technique cannot be applied. The disadvantages of the PCSNIM technique are the higher value of noise resistance R_n and the lower value of effective cutoff frequency. With the production development, higher R_n can be the source of lower yield. Overall, based on the noise parameter equations, this study provides a clear understanding of the design principles, fundamental limitations, and advantages of the reported LNA design techniques so that the designers can get the general LNA design perspective.

As a demonstration for the proposed design principle of the PCSNIM technique, a very low-power folded-cascode LNA is fabricated based on 0.25-μm CMOS technology for 900-MHz Zigbee applications. Measurement results show the NF of 1.35 dB, power gain of 12 dB, and IIP3 of -4 dBm while dissipating 1.6 mA from a 1.25-V supply. The NMOS input stage of the LNA dissipates only 0.7 mA. The overall behavior of the implemented LNA shows good agreement with the proposed design principle.

APPENDIX

As can be seen in Fig. 2(b), the mean-squared output noise current of the source terminal is given by

$$\overline{i_{o,ns}^2} = \left|\frac{R_s}{D}\cdot g_m\right|^2 \cdot \overline{i_{ns}^2}. \tag{A1}$$

Here, the denominator D is

$$D = 1 + s^2 C_{\mathrm{gs}}\left(L_g + L_s\right) + s\left(C_{\mathrm{gs}}R_s + g_m L_s\right). \tag{A2}$$

When the admittance of the source termination is purely resistive, the source admittance is expressed as $Y_s = G_s = (R_s)^{-1}$ so that the mean-squared noise current by the source is $\overline{i_{ns}^2} = 4kTG_s\Delta f$.

The mean-squared output noise current by the gate-induced noise source is

$$\overline{i_{o,ng}^2} = \left|\frac{R_s + s\left(L_g + L_s\right)}{D}\cdot g_m\right|^2 \cdot \overline{i_{ng}^2}. \tag{A3}$$

The mean-squared output noise current by the channel noise source is changed by the feedback source inductance L_s so that the expression is

$$\overline{i_{o,nd}^2} = \left|\frac{1 + s^2 C_{\mathrm{gs}}(L_g + L_s) + sC_{\mathrm{gs}}R_s}{D}\right|^2 \cdot \overline{i_{nd}^2}. \tag{A4}$$

At the resonance condition for the matching, the reactance of the input impedance is zero, therefore, the first two terms in the denominator of (A2) and the numerator of (A4) are summed to zero, i.e., $1 - \omega C_{\mathrm{gs}}(\omega L_g + \omega L_s) = 0$. Considering the correlation between the gate-induced and channel noise sources, the gate-induced noise current is expressed as the sum of uncorrelated and correlated components. The mean-squared expression of the gate-induced noise is

$$\overline{i_{ng}^2} = \overline{i_{ngu}^2} + \overline{i_{ngc}^2} = 4kT\delta g_g\left(1 - |c|^2\right) + 4kT\delta g_g|c|^2. \tag{A5}$$

Here, the coefficient of the correlation between gate-induced and channel noise sources is

$$\frac{i_{ngc}}{i_{nd}} = j|c|\frac{\sqrt{\overline{i_{ng}^2}}}{\sqrt{\overline{i_{nd}^2}}}. \tag{A6}$$

The total output noise current consists of the output current from the resistive source termination, gate-induced noise, and channel noise sources. Considering correlation, the total output noise current is expressed as

$$\begin{aligned}|i_{o,\mathrm{total}}|^2 &= |i_{o,ns} + i_{o,ng} + i_{o,nd}|^2 \\ &= |i_{o,ns}|^2 + |i_{o,ngc} + i_{o,nd}|^2 + |i_{o,ngu}|^2.\end{aligned} \tag{A7}$$

The noise factor (F) is defined as the ratio between the total mean-squared output noise current and the mean-squared output noise current due to the input source only, i.e.,

$$F \equiv \frac{|i_{o,\mathrm{total}}|^2}{|i_{o,ns}|^2}. \tag{A8}$$

Therefore, by using (A1)–(A8), the noise factor can be given by

$$\begin{aligned}F = 1 &+ \frac{1}{g_m^2 R_s} \\ &\cdot \left\{\gamma g_{d0}\cdot\left\{\left[1 + s^2 C_{\mathrm{gs}}(L_g + L_s)\left(1 + |c|\alpha\sqrt{\frac{\delta}{5\gamma}}\right)\right]^2\right. \\ &\qquad \left. - (sC_{\mathrm{gs}}R_s)^2\left(1 + |c|\alpha\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\} \\ &\quad \left. - \frac{\alpha\delta}{5}\left(1 - |c|^2\right)g_m\left(sC_{\mathrm{gs}}\right)^2\left(R_s^2 - sL_g^2\right)\right\}.\end{aligned} \tag{A9}$$

In general, F can be expressed as follows [4]:

$$F = F_{\min} + \frac{R_n|Y_s - Y_{\mathrm{opt}}|^2}{G_s}. \tag{A10}$$

The noise resistance R_n can be obtained by comparing (A9) with (A10). The optimum source impedance $Z_{\rm opt}$ can be obtained by solving the zero solutions after differentiating (A10) with respect to R_s and L_g. Now, by inserting the $Z_{\rm opt}$ expression into (A9), $F_{\rm min}$ can be obtained. After some tedious calculations, the noise parameters can be derived as follows:

$$R_n = R_n^o = \frac{\gamma}{\alpha}\cdot\frac{1}{g_m} \tag{A11}$$

$$Z_{\rm opt} = Z_{\rm opt}^o - sL_s \tag{A12}$$

$$F_{\rm min} = F_{\rm min}^o = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta\left(1-|c|^2\right)}. \tag{A13}$$

Here, the superscripted zero is adopted to represent the corresponding noise parameters of the common-source amplifier with no degeneration [see (5)–(8)].

In (A12), the optimum noise impedance without source degeneration is equal to

$$Z_{\rm opt}^o = \frac{1}{Y_{\rm opt}^o} = \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}} + j\left(1+\alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{\rm gs}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(1+\alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}}. \tag{A14}$$

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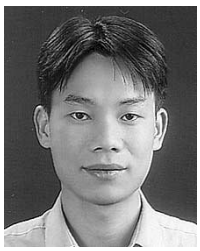

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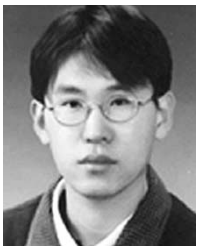

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