



Cairo University



Faculty of Engineering

Advanced Topics in Electronics-1

Under supervision of:

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Eng. Ahmed Atef

Students Names:

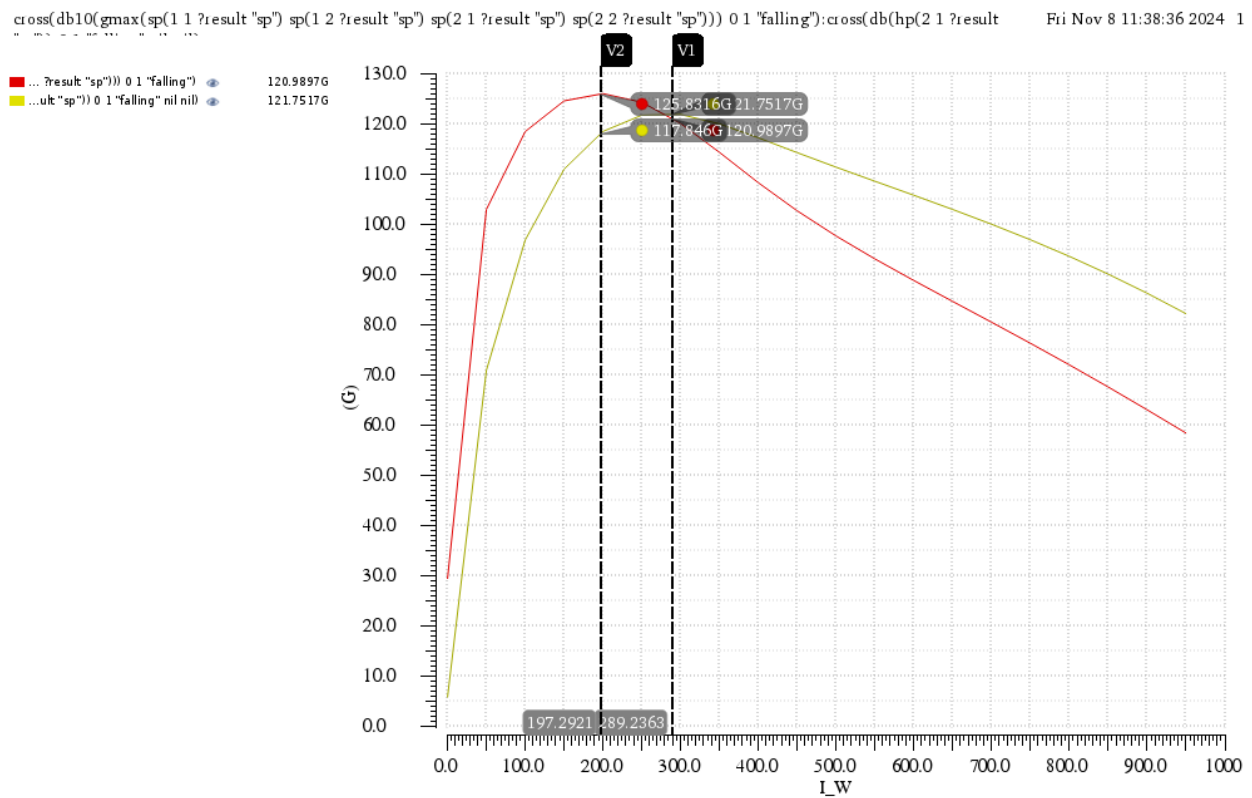
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1. F_t & F_{MAX} versus current density for $|V_{DS}| = 0.5V, 0.8V, 1.0V$ & $1.2V$.
Find J_{pFT} and J_{pFMAX}

NMOS:

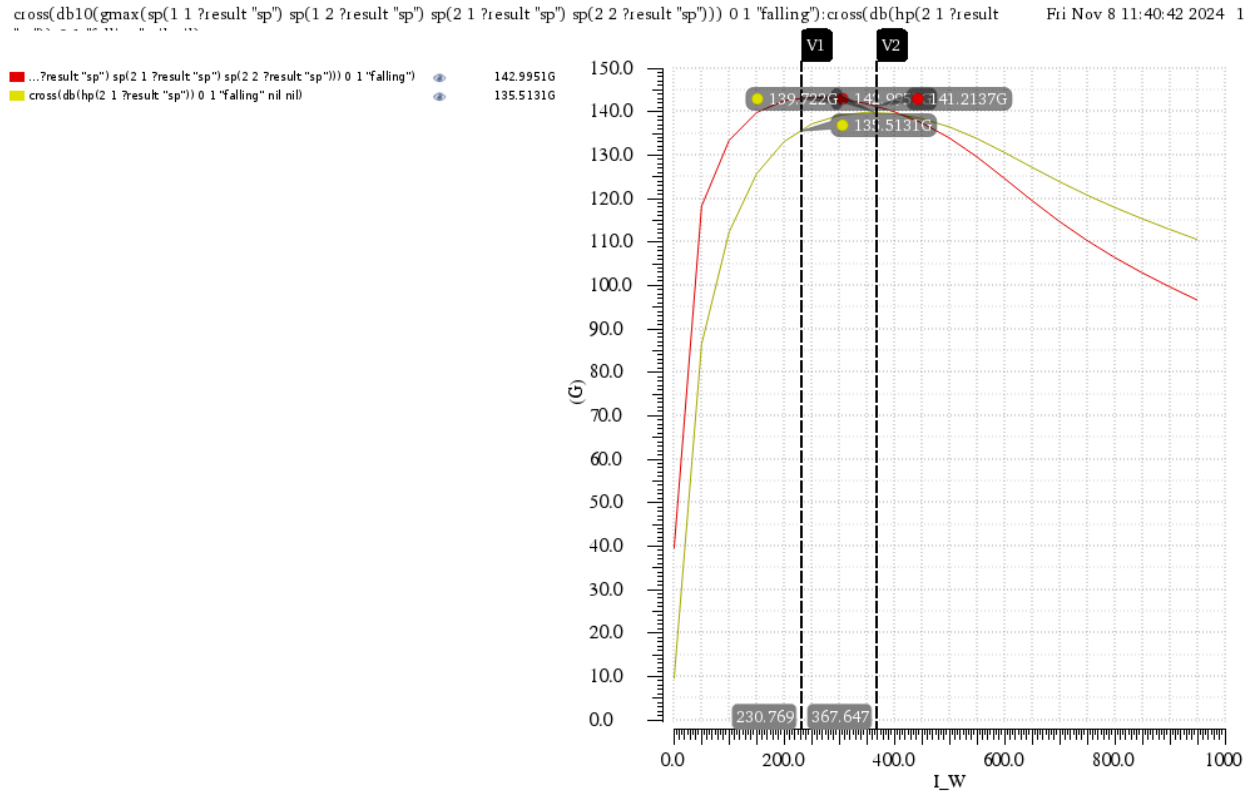
At $V_{DS} = 0.5V$



$J_{pFT} = 289.236 \mu A/\mu m$ with highest $F_T = 121.7517$ GHz.

$$J_{pFMAX} = 197.2921 \mu A/\mu m \text{ with highest } F_{MAX} = 125.8316 \text{ GHz.}$$

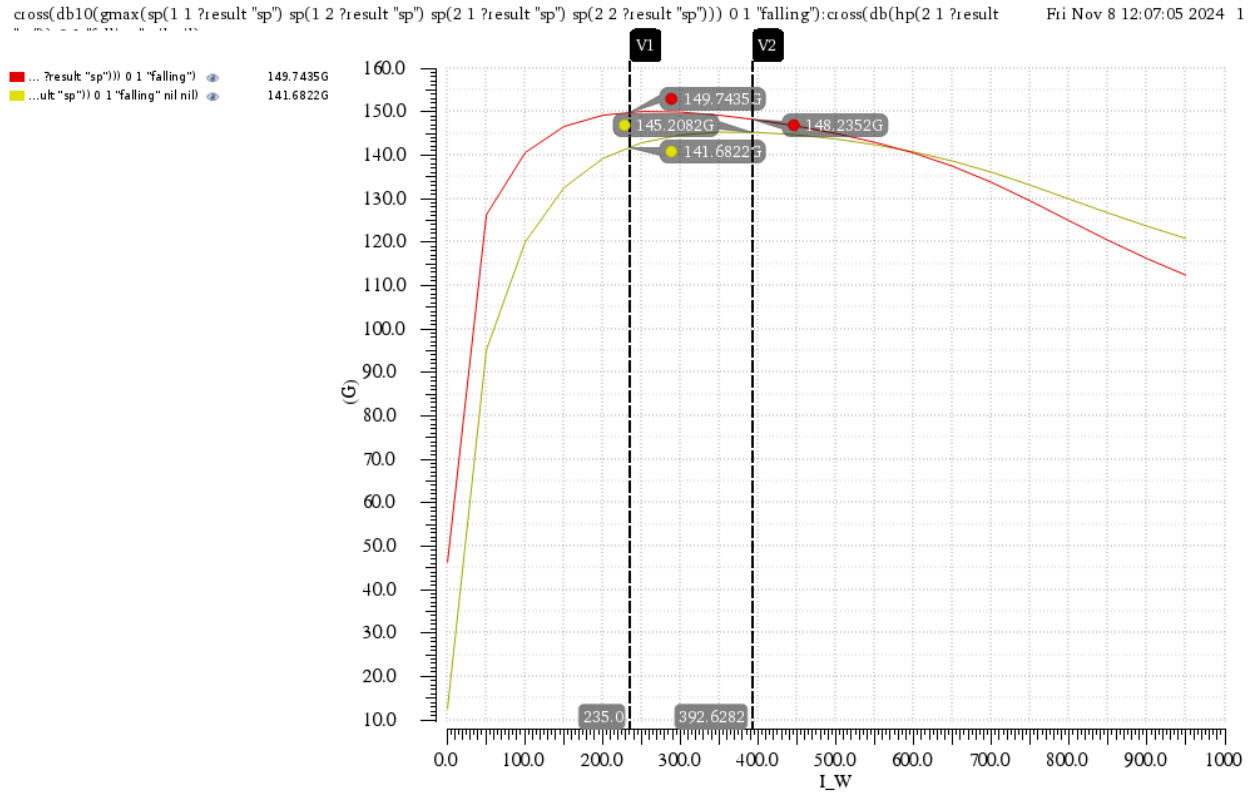
At $V_{DS} = 0.8V$:



$J_{pFT} = 367.647 \mu A/\mu m$ with highest $F_T = 139.722$ GHz.

$J_{pFMAX} = 230.769 \mu A/\mu m$ with highest $F_{MAX} = 142.995$ GHz.

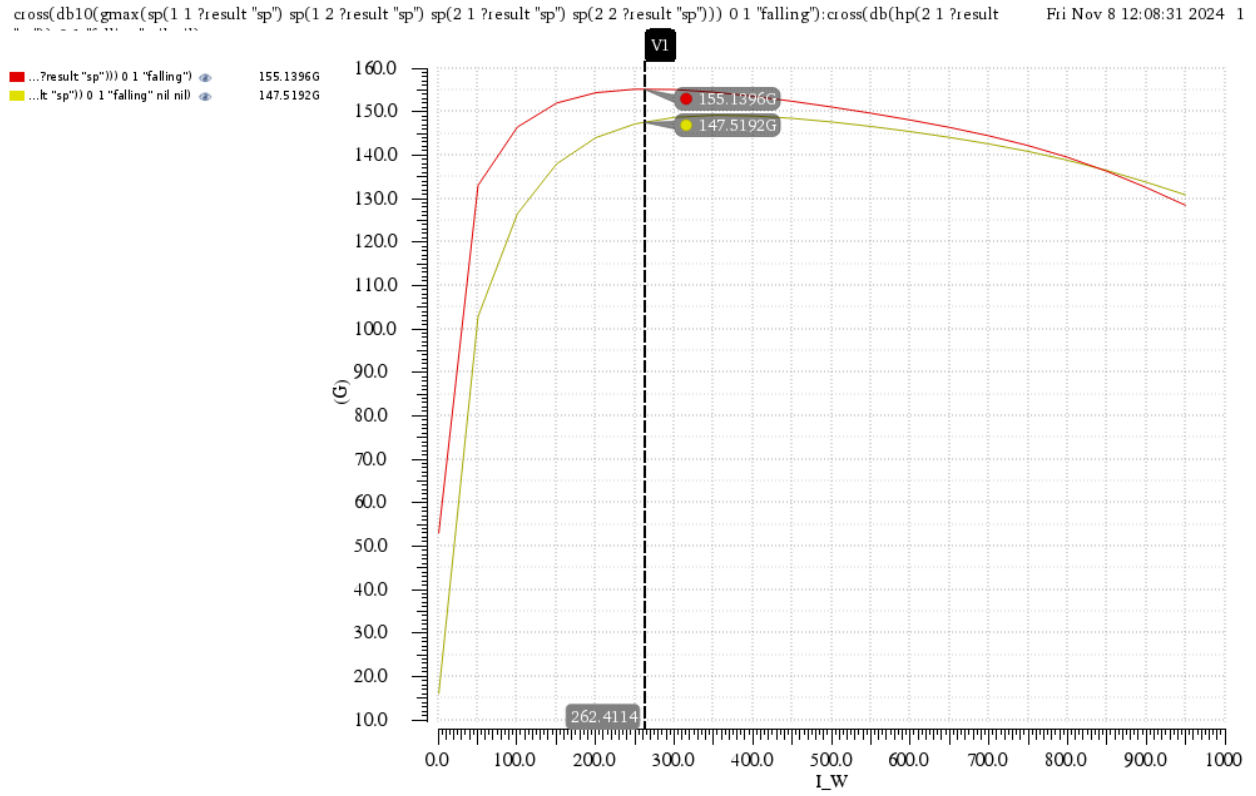
At $V_{DS} = 1.0V$:



$J_{pFT} = 392.6282 \mu A/\mu m$ with highest $F_T = 145.2082$ GHz.

$J_{pFMAX} = 235 \mu A/\mu m$ with highest $F_{MAX} = 149.7453$ GHz.

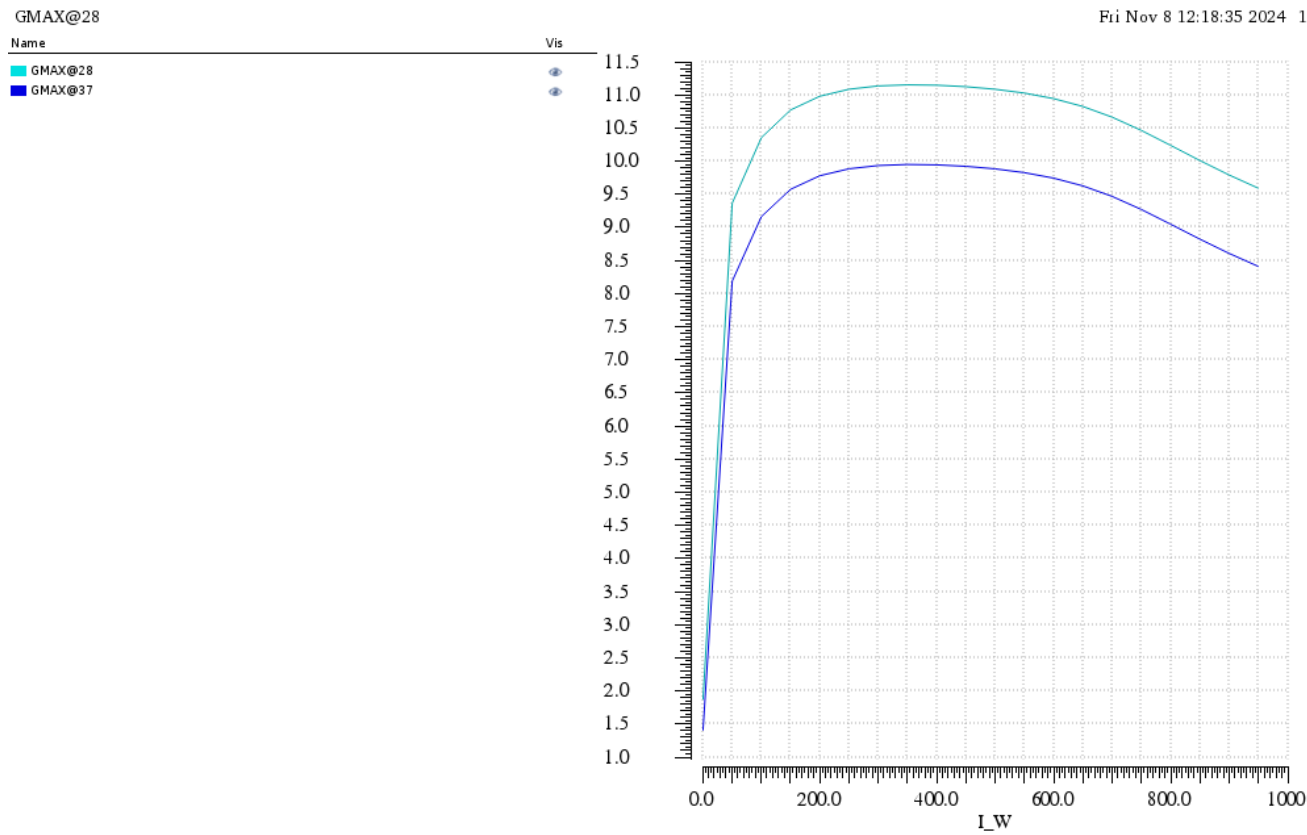
At $V_{DS} = 1.2V$:



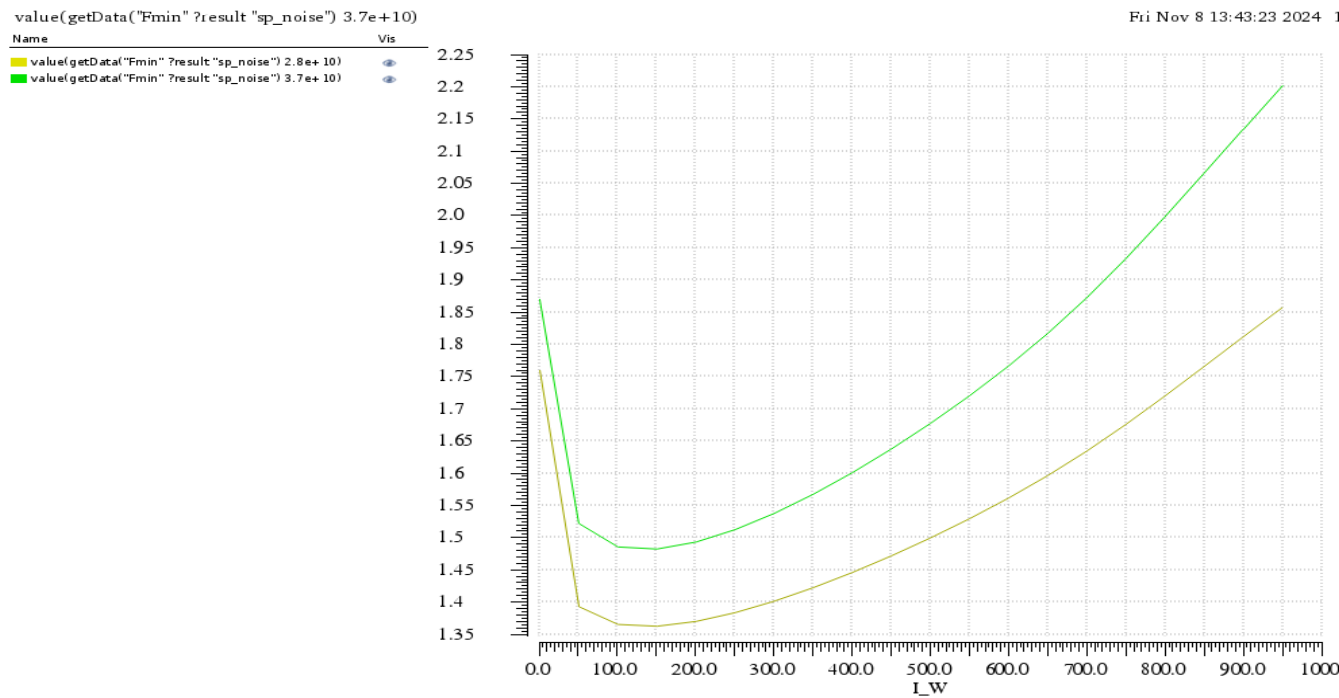
$J_{pFT} = 262.4114 \mu A/\mu m$ with highest $F_T = 147.5192$ GHz.

$J_{pFMAX} = 262.4114 \mu A/\mu m$ with highest $F_{MAX} = 155.1396$ GHz.

2. G_{MAX} @ 28Ghz & 37Ghz

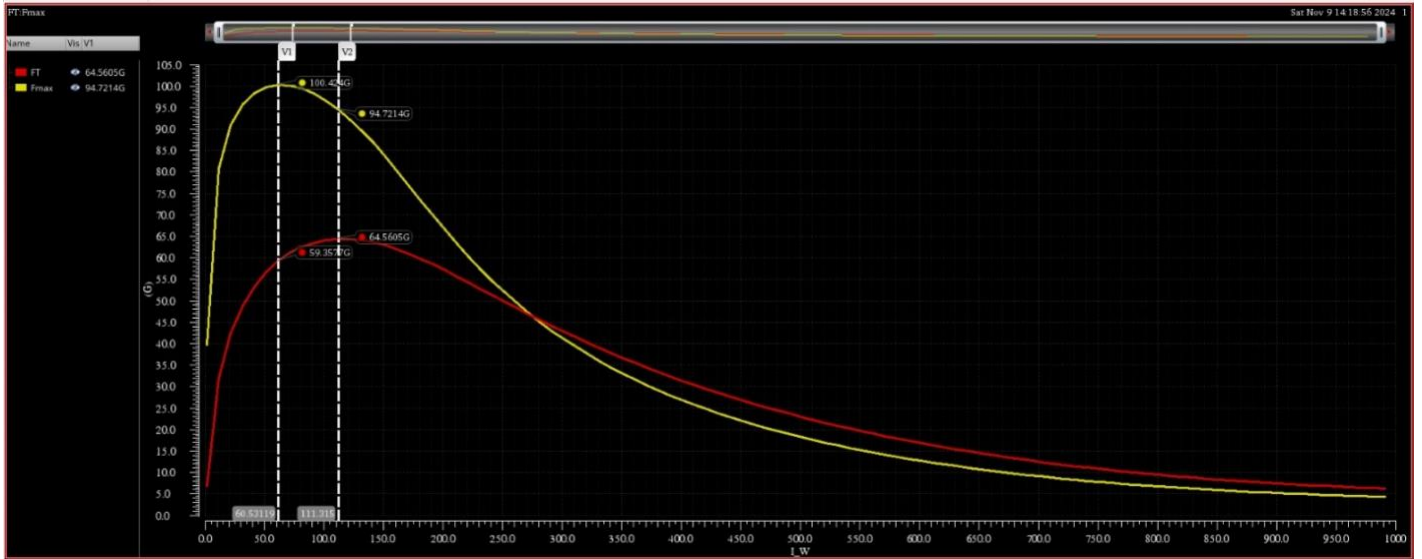


3. NF_{min} @ 28Ghz & 37Ghz



PMOS:

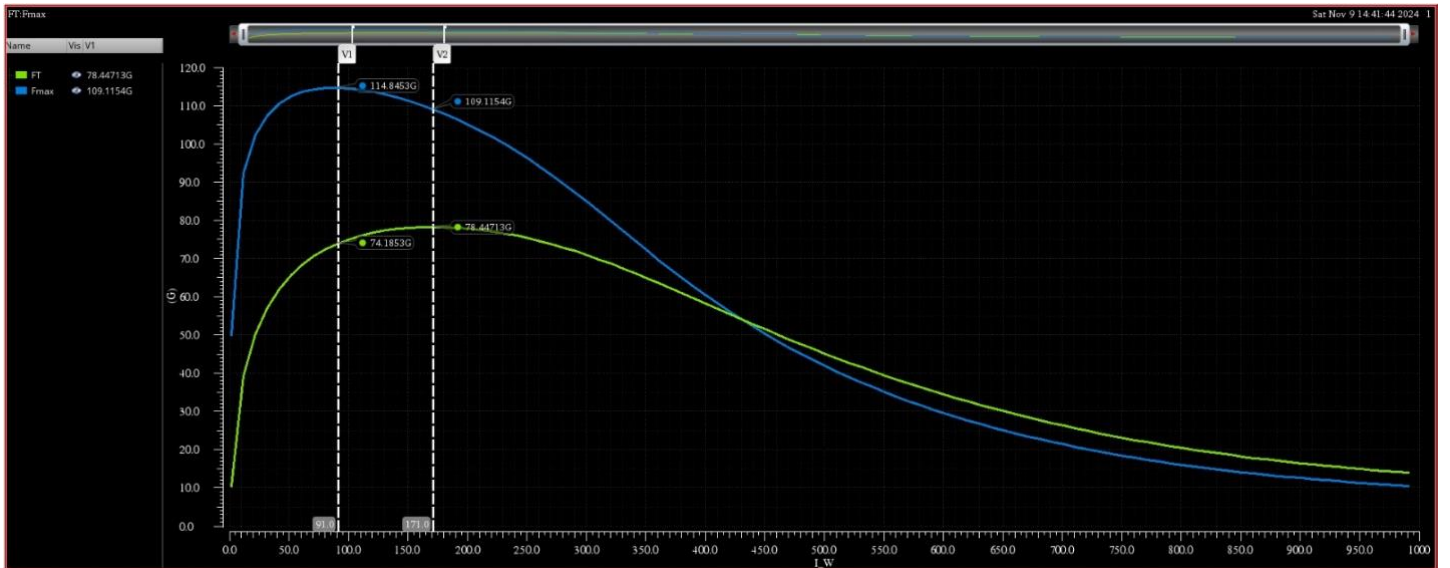
At $V_{DS} = 0.5V$



$J_{pFT} = 111.315 \mu A/\mu m$ with highest $F_T = 64.56$ GHz.

$J_{pFMAX} = 60.53119 \mu A/\mu m$ with highest $F_{MAX} = 100.42$ GHz.

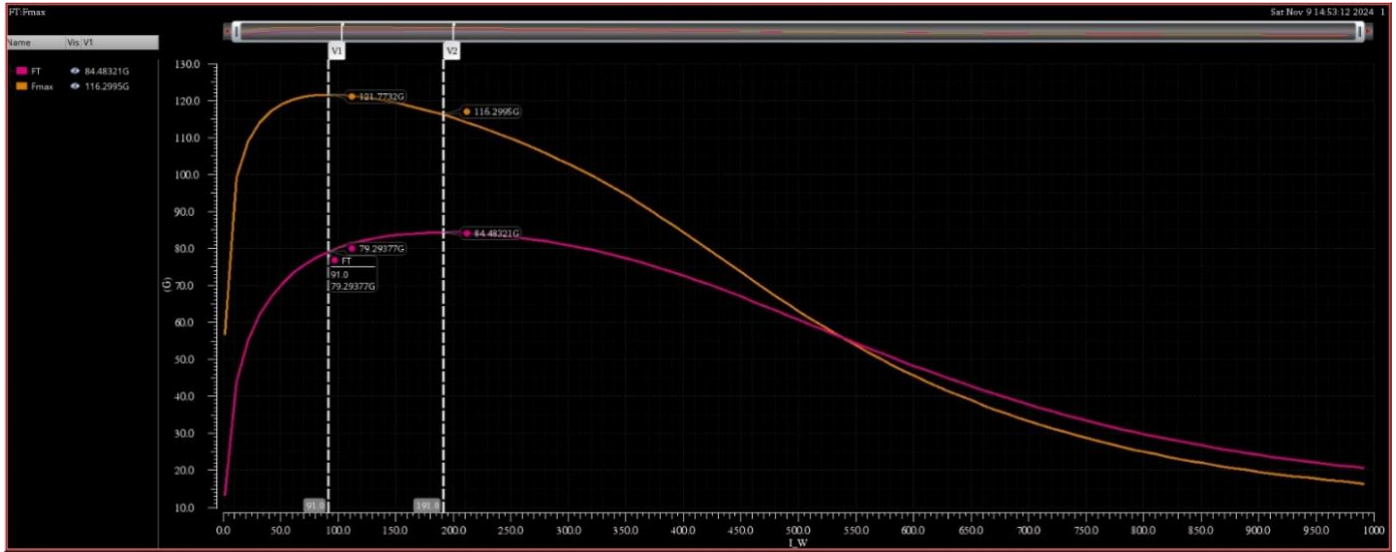
At $V_{DS} = 0.8V$



$J_{pFT} = 171 \mu A/\mu m$ with highest $F_T = 78.447$ GHz.

$J_{pFMAX} = 91 \mu A/\mu m$ with highest $F_{MAX} = 114.8453$ GHz

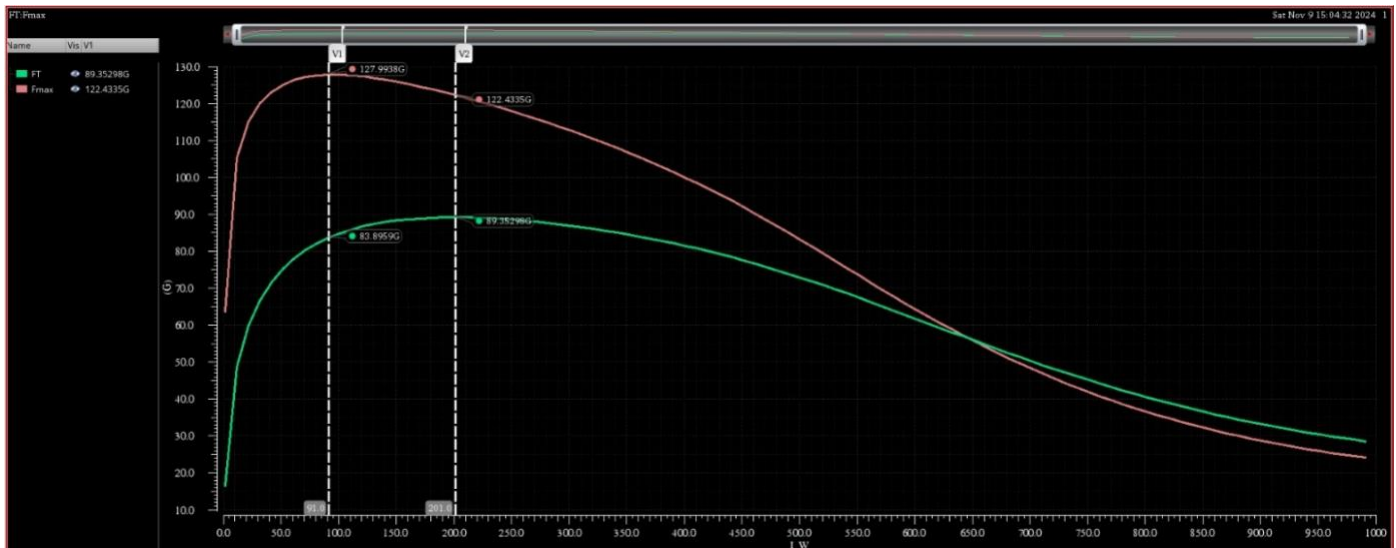
At $V_{DS} = 1.0V$



$J_{pFT} = 191 \mu A/\mu m$ with highest $F_T = 84.4322$ GHz.

$J_{pFMAX} = 91 \mu A/\mu m$ with highest $F_{MAX} = 121.7732$ GHz.

At $V_{DS} = 1.2V$



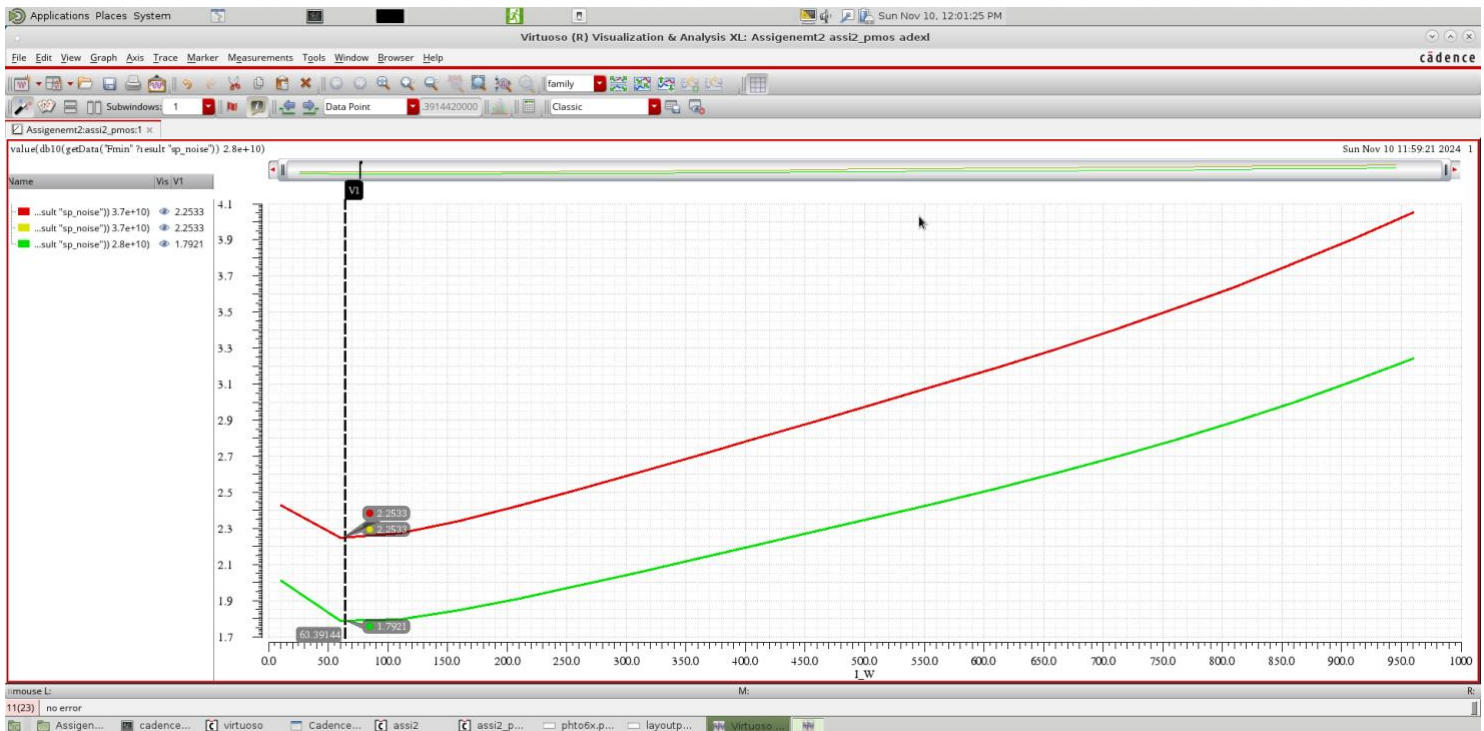
$J_{pFT} = 201 \mu A/\mu m$ with highest $F_T = 89.35298$ GHz.

$J_{pFMAX} = 91 \mu A/\mu m$ with highest $F_{MAX} = 127.9938$ GHz.

2. G_{MAX} @ 28Ghz & 37Ghz

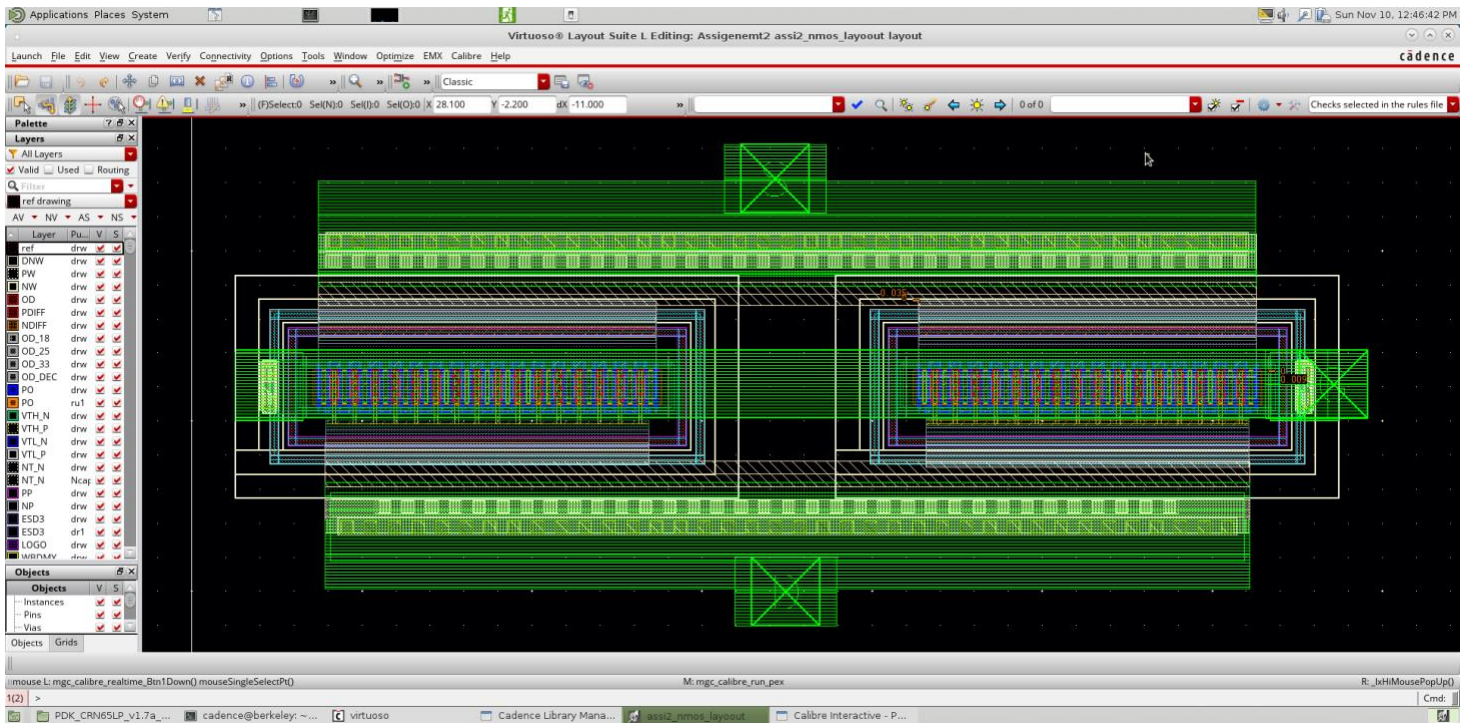


2. NF_{min} @ 28Ghz & 37Ghz



4. Repeat 1 to 3 after running RC extraction for the devices (make sure all the parasitics up to the top metallization with the routing of the 2 multipliers are included) and replot on the same graphs only for $V_{DS} = 1.0V$

NMOS layout



F_T & F_{MAX} at $V_{DS} = 1.0V$



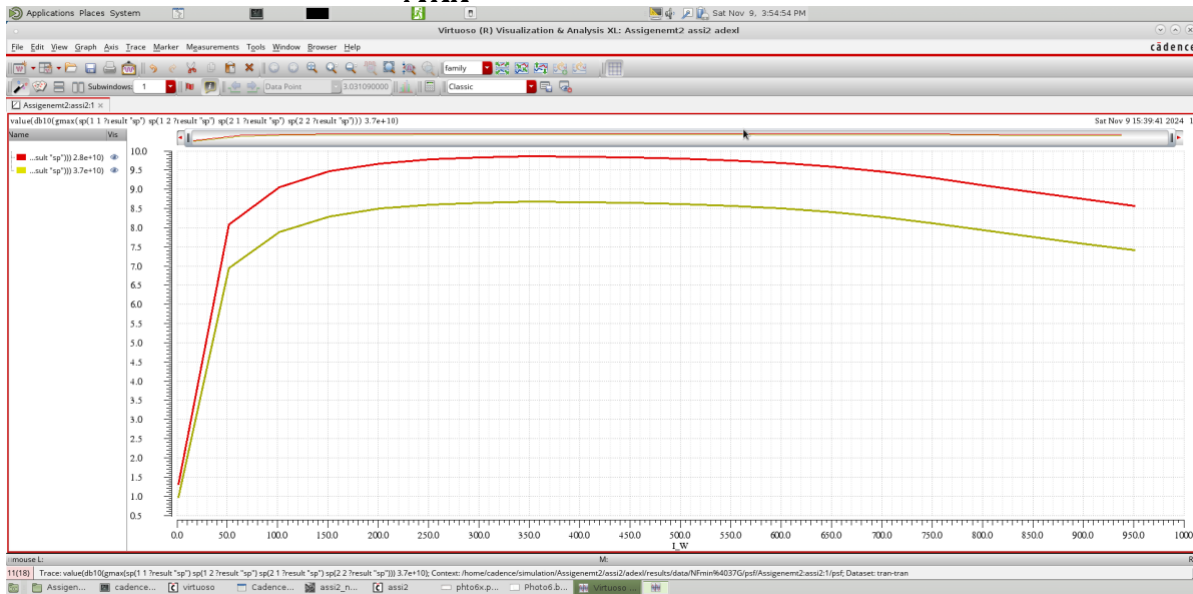
$J_{pFT} = 353.32 \mu A/\mu m$ with highest $F_T = 116$ GHz.

$J_{pFMAX} = 283.0311 \mu A/\mu m$ with highest $F_{MAX} = 129.59$ GHz.

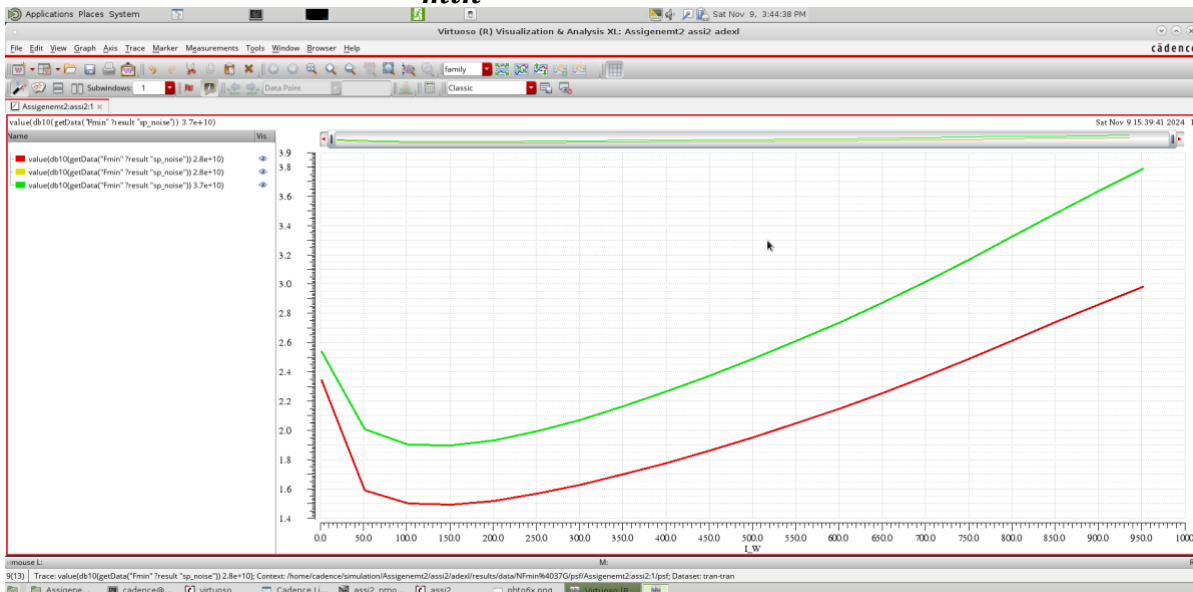
The value of F_{MAX} and F_T degrade because of parasitic generated by layout.

Before layout at $V_{DS} = 1.0V$. F_{MAX} was equal to 149.7453 GHz & $F_T = 145.2082$ GHz

G_{MAX} @ 28Ghz & 37Ghz

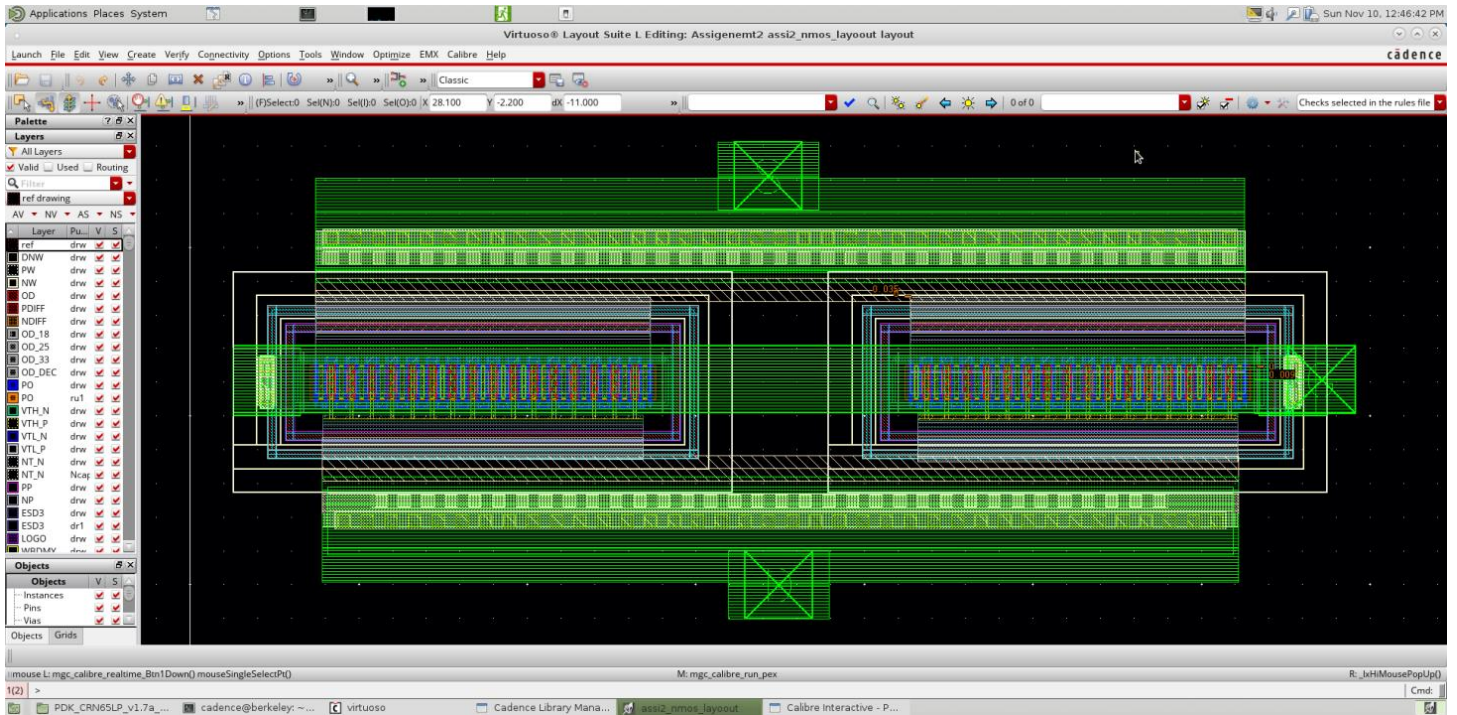


NF_{min} @ 28Ghz & 37Ghz



We can also see that the noise figure increased due to parasitics.

PMOS layout



$$F_T \text{ \& } F_{MAX} \text{ at } V_{DS} = 1.0V$$



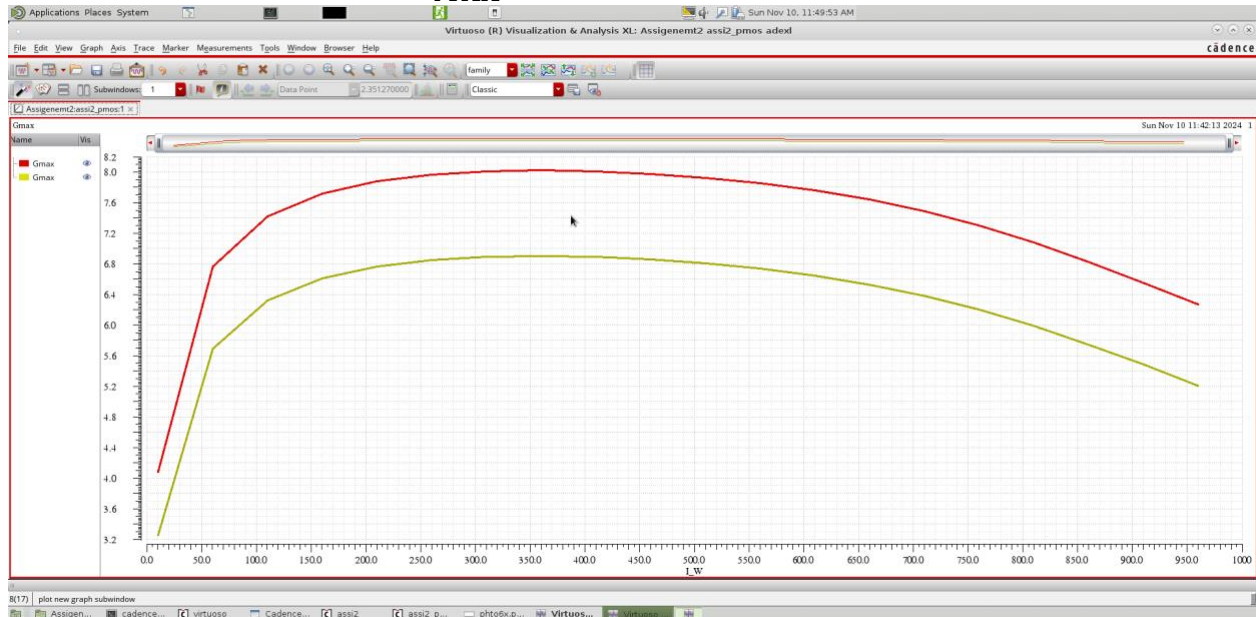
$J_{pFT} = 392.3513 \mu A/\mu m$ with highest $F_T = 69.7$ GHz.

$J_{pFMAX} = 185.5524 \mu A/\mu m$ with highest $F_{MAX} = 103.59$ GHz.

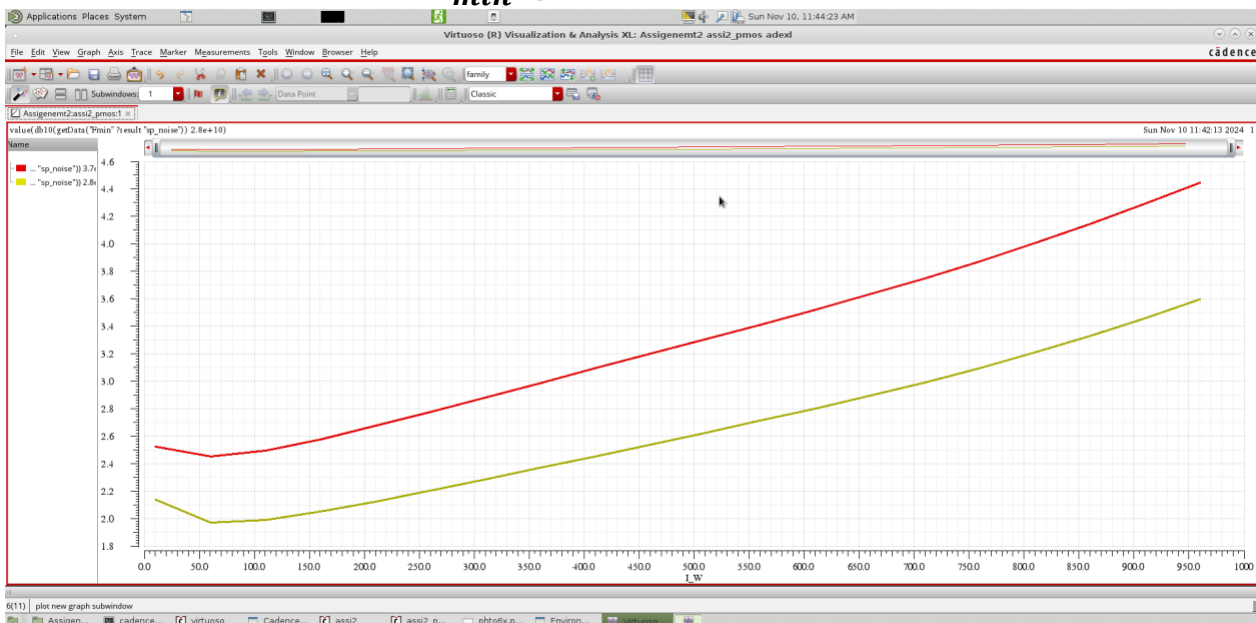
The value of F_{MAX} and F_T degrade because of parasitic generated by layout.

Before layout at $V_{DS} = 1.0V$. $F_T = 84.4322$ GHz & $F_{MAX} = 121.7732$ GHz

G_{MAX} @ 28Ghz & 37Ghz



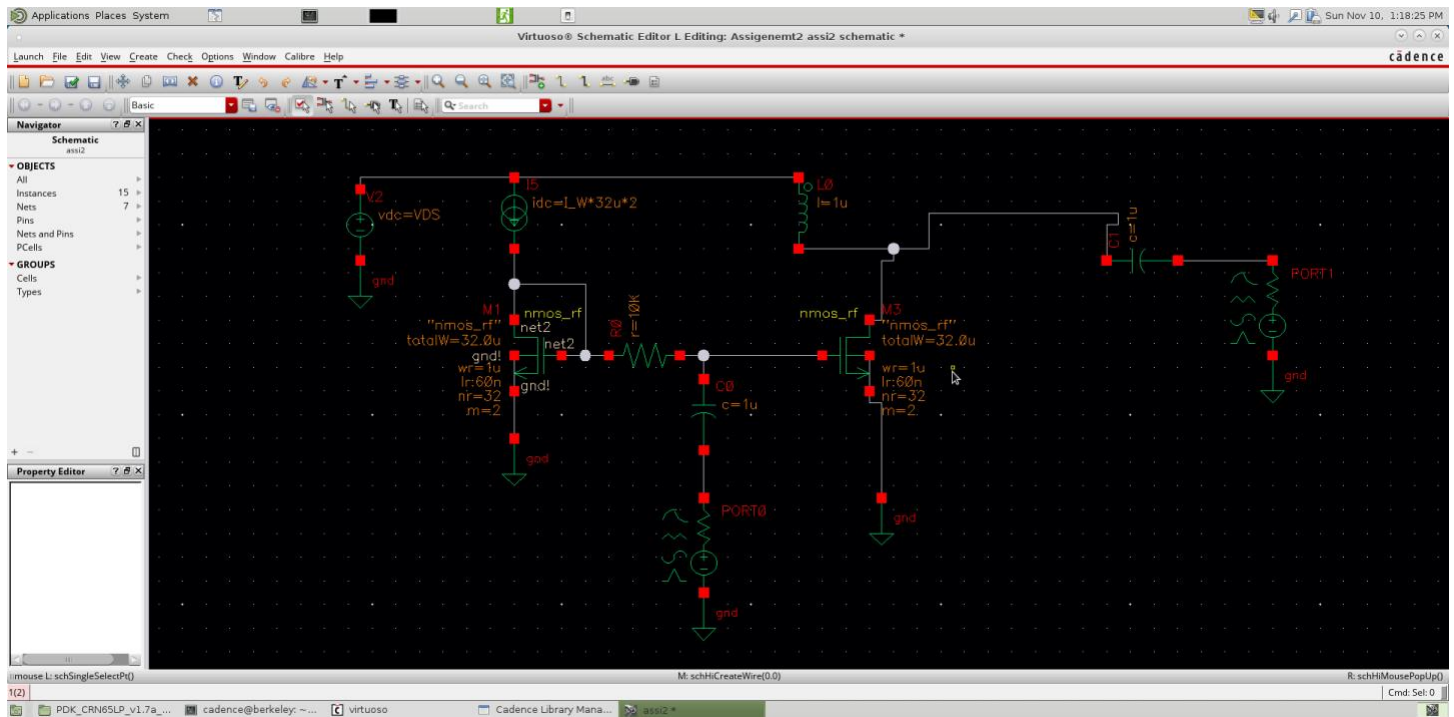
NF_{min} @ 28Ghz & 37Ghz



We can also see that the noise figure increased due to parasitics.

5. Show the testbench used to generate the results

NMOS testbench:

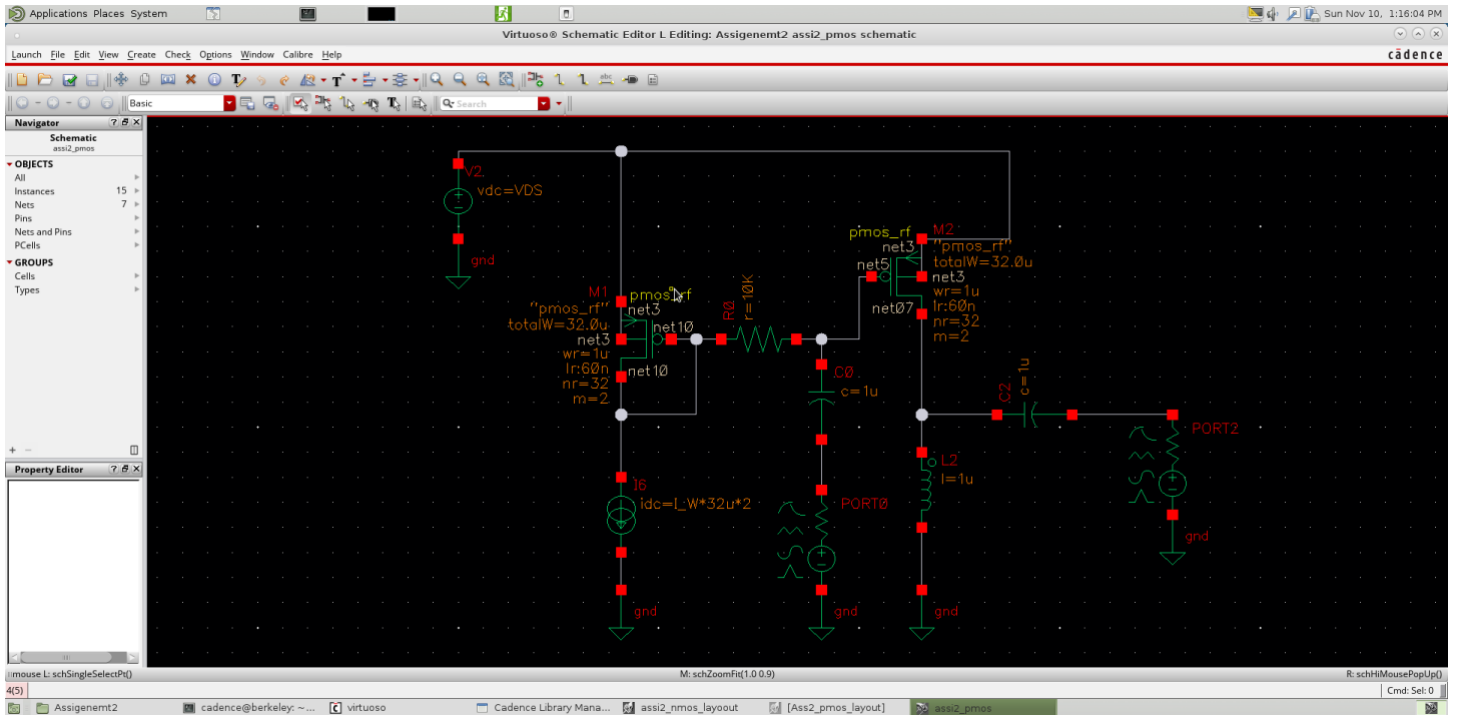


The screenshot displays the Virtuoso Analog Design Environment interface showing the test results. The "Data View" tab is active, displaying a table of test results. The table has columns for Test, Name, Type, Details, EvalType, Plot, Save, Spec, Weight, Units, Digits, Notation, and Suffix. The test results are as follows:

Test	Name	Type	Details	EvalType	Plot	Save	Spec	Weight	Units	Digits	Notation	Suffix
Assigenem2.ass2:1	Gmax dB10	expr	db10(gmax(sp1 1 ?result "sp") sp1 2 ?result "sp")	point								
Assigenem2.ass2:1	H21 dB20	expr	db(hp2 1 ?result "sp")	point								
Assigenem2.ass2:1		expr	cross(db10(gmax(sp1 1 ?result "sp") sp1 2 ?result "sp") 0.1 ?falling "nil")	point								
Assigenem2.ass2:1		expr	mag(db10(gmax(sp1 1 ?result "sp") sp1 2 ?result "sp") 0.1 ?falling "nil")	point								
Assigenem2.ass2:1	GMAX@28	expr	average(mag(db10(gmax(sp1 1 ?result "sp") sp1 2 ?result "sp") 0.1 ?falling "nil") 28)	point								
Assigenem2.ass2:1	NFmin dB10	expr	db10(gminData("Fmin" ?result "sp_noise"))	point								
Assigenem2.ass2:1		expr	value(db10(getData("Fmin" ?result "sp_noise"))	point								

The "Run Summary" tab is also visible, showing the test results for the "1 Test" run. The summary indicates that the test was successful, with 20 Point Sweeps, 0 Corner, and Nominal Corner.

PMOS testbench:



The screenshot shows the Cadence Virtuoso Analog Design Environment interface. The main workspace displays the testbench results. The results are shown in a table with columns: Test, Name, Type, Details, EvalType, Plot, Save, Spec, Weight, Units, Digits, Notation, and Suffix. The table contains the following data:

Test	Name	Type	Details	EvalType	Plot	Save	Spec	Weight	Units	Digits	Notation	Suffix
Assignem2.assi2_pmos:1	Nfmin dB10	expr	db10(getData("Fmin" ?result "sp_noise"))	point								
Assignem2.assi2_pmos:1	Fmax	expr	value(db10(getData("Fmin" ?result "sp_noise")))	point								
Assignem2.assi2_pmos:1	FT	expr	cross(db10(gmax(sp(1.1 ?result "sp") sp(1.2 ?result "sp")) 0.1 ?result "sp") 0.1 ?result "sp")	point								
Assignem2.assi2_pmos:1	Gmax	expr	value(db10(gmax(sp(1.1 ?result "sp") sp(1.2 ?result "sp")) 0.1 ?result "sp") 0.1 ?result "sp")	point								

The table also includes a 'Run Summary' section with the following data:

Run Summary	Test	Setup States	Reliability Analyses	Checks/Asserts
1 Test				
20 Point Sweeps				
0 Corner				
Nominal Corner				