

EE290C – Spring 2011

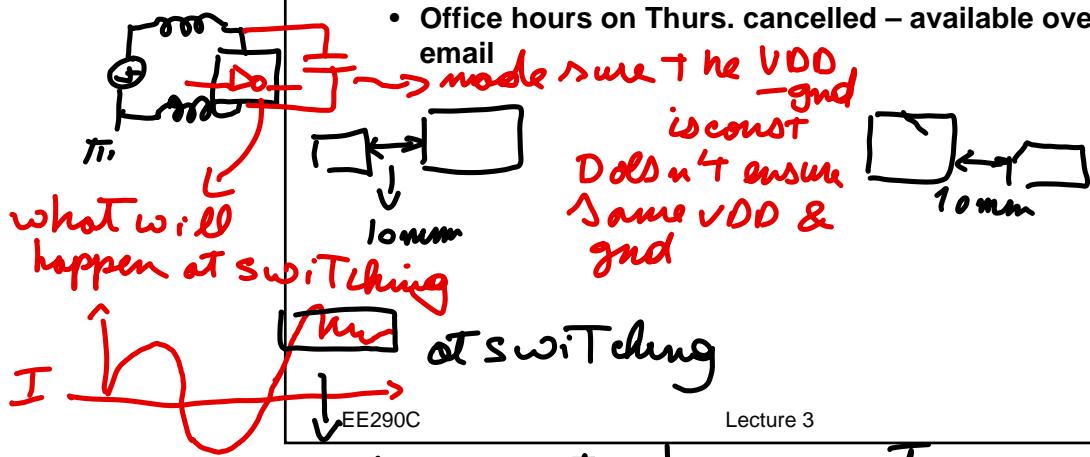
Lecture 3: Basic Transmitters and Receivers



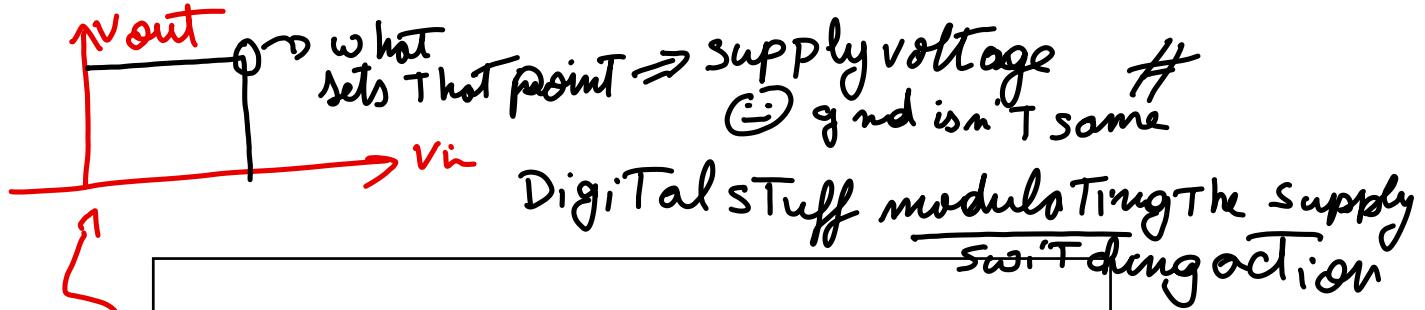
Elad Alon
Dept. of EECS

Administrative

- Elad will be out of town this Thurs.
 - Make-up lecture will be held on Mon. 1-31 1:30-3:00pm in 127 Dwinelle
 - Office hours on Thurs. cancelled – available over email



• Inductor gets a huge current
=> cause a huge change in voltage

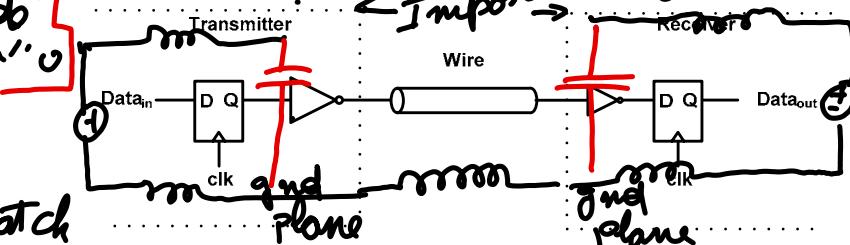


①

how Does The inverter Decide what α' & α'' is?
 how Does The Threshold of both inverter match
 \Rightarrow well actually, IT Does n't

Disadvantage

Plain Old Inverters – Why Not?



+ VDD isn't only local voltage source
 IT's a supply network with R_{out} so

with this switching action \Rightarrow create AC current [Noise]

Issues with this system:

- * Single ended
 - \hookrightarrow Noise immunity - CM rejection
- * No termination
- * Edge-rate control

Travel From VDD To Ground & cause VDD & ground variation

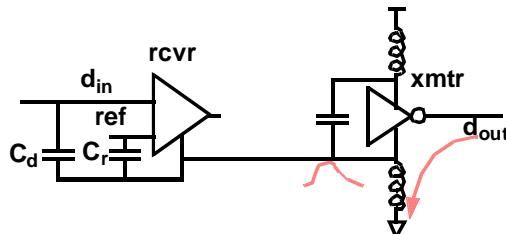
like inductor hate to change states fast \Rightarrow
 so in the wire \Rightarrow sharp edge mean a very small Z & L effect across
 even a slight discontinuity.

\hookrightarrow sharp edge is composed of high frequency component

Outline

- Signaling Basics
 - Single-ended vs. differential
 - "Current-mode" vs. "Voltage-mode" signaling
 - Termination
- TX Circuit Design
 - Z control
 - CML, VM drivers
 - Power vs. swing
 - Serialization options
- RX Circuit Design
 - Comparator review
 - Deserialization options

Single-Ended Signaling



- RX: comparing against a shared reference \Rightarrow you will multiple different return paths \Rightarrow not really good way for a shared reference
- Reference may be implicit (i.e., ground/supply)
- Mismatch between shared and individual lines
- TX: generates large variations on power supply
 - SSO - simultaneous switching outputs
 - No XTALK immunity

have a big bus of signals each

one have a Far End

To Drive 30m Imagine

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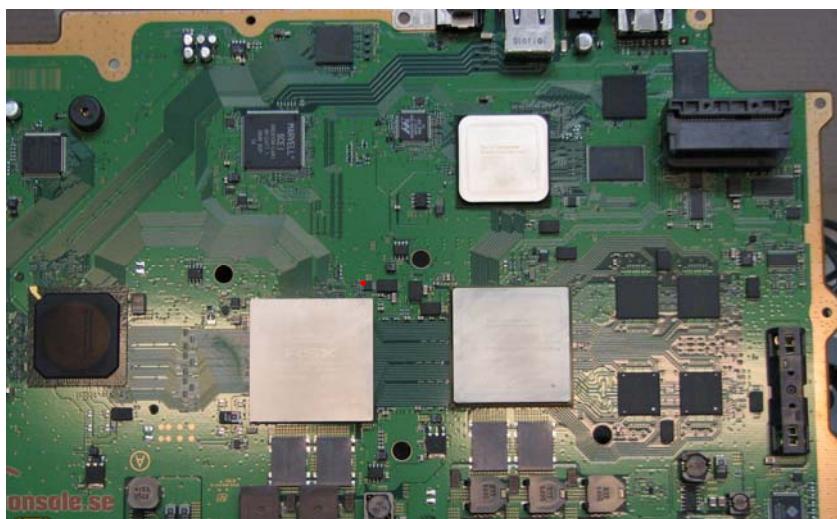
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If they all had Transition at the same time \Rightarrow inductor T \Rightarrow many glitches of currents \Rightarrow all chip signals will change relative to ground

Those changes won't get discarded
as CM this is signals ended

So Why Even Mention This?



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Single-ended signaling is still being used because we can reduce the number of pins

Classic Debate

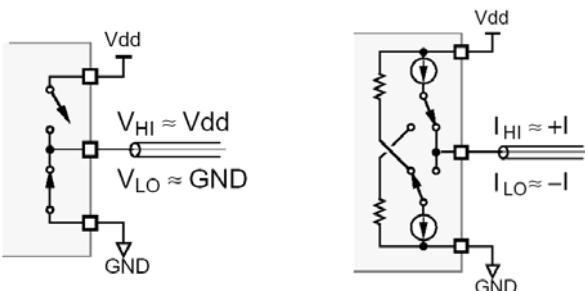
- "Differential must be twice as fast as single-ended in order to win" → *single ended argument*
- Reality more complicated
 - E.g., power supply to signaling pin ratio higher in S.E.
- Short "answer"
 - Differential a lot easier to build and get right the first time
 - Can make S.E. work – *but often a lot more painful*

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"Voltage-Mode" vs. "Current-Mode"



- Transmission line has both voltage and current...
- Terminology unfortunately heavily overloaded
 - Whether or not Z_0 of driver is high
 - How Z_0 of driver is set
 - What sets output swing

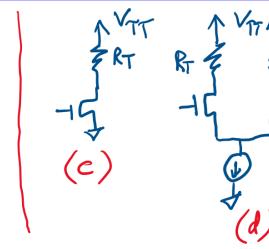
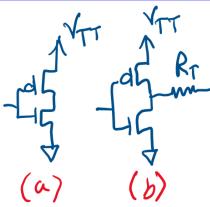
well in this case voltage mode mean that the line has low impedance & The inverse for current mode.

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"Voltage-Mode" vs. "Current-Mode"

V_{TT} means a separate supply
Transistors are in triode



Transistors are in SAT

(a) "Voltage": Z_0 set by devices, swing set by V_{TT}

(b) "Voltage": Z_0 set by R_T , swing set by V_{TT}

(c) & (d) "Current": Z_0 set by R_T , swing set by I_{bias}

$$\hookrightarrow v_{out} = \frac{R_T / r_o}{V_{TT} - I_{bias} \times R_T} \approx 1 \text{ mV}$$

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Depend on Devices
but DAC said otherwise
This Termination
is made I_T sets
by R_T most by

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Another View

voltage mode current

	"Low Impedance"	"High Impedance"
Single Ended		
Differential		

but reflector

- RX opposite of TX

• Signal integrity implications?

low impedance To Take all current

To get all voltage why I only terminate one side ??
assume $\Omega = Z_T$
a Hand will get the meaning
that For the same amount
of current less swing

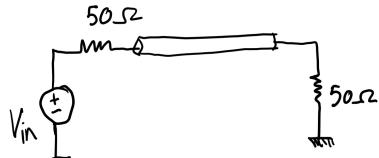
Basically, if I only have termination at one side only, I would get double the swing I would get if I terminated on both sides.

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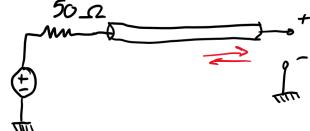
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Why Terminate?



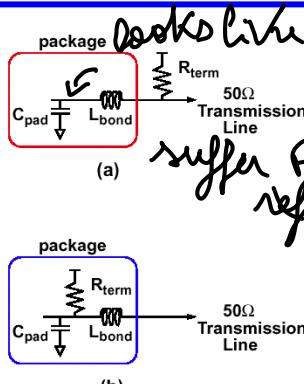
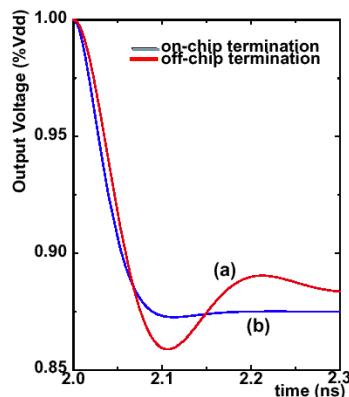
We terminate on both sides, so our system would be more robust in terms of signal integrity



Here, We get 2x swing for the same Power
But we get a lot of reflections back & forth

DC at least #

External vs. Internal Termination



looks like high impedance
suffer from reflections but IT's a lot easier to get accurate external resistor
IT suffer from PVT internally

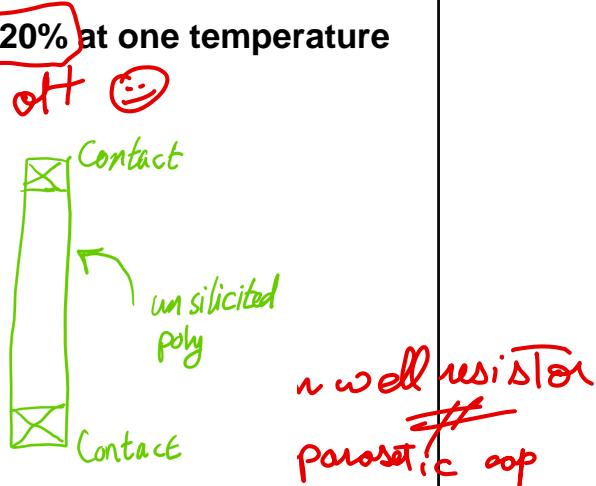
- Internal: makes package L, pad C part of T-line
- External: chip/package become a stub
 - If want on-die term need to control its value...

Internal termination (on-die) need value control because the on-die resistor's variation with PVT

Untrimmed Poly Termination

- Main issue is variation: $\pm 20\%$ at one temperature
- But
 - It's relatively linear
 - ESD robust
 - Low parasitics...

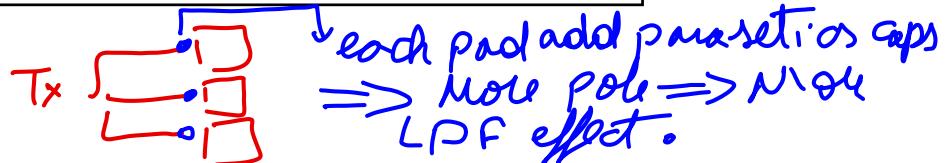
\rightarrow electro static discharge \neq fluctuation causing circuit failure



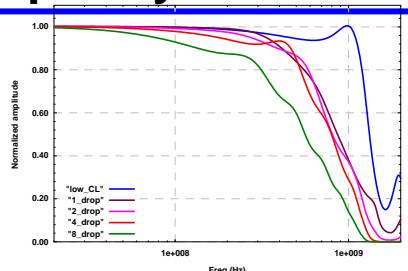
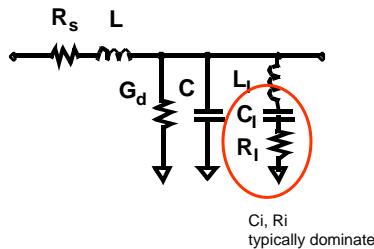
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R_i, C_i, and Pad Complexity



- LPF at pad can dominate overall channel
- Example: 500fF ESD, 500fF driver, 500fF wire \Rightarrow very wide \Rightarrow They carry a lot of current
- Even worse in busses (or if add big series R)... Those parasitics

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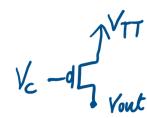
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more ESD protection, also create a zero Tolerance
path from parasitic cap, Resistor all more

controlled that trans is to less dynamic range.

Active Terminations

$0 \rightarrow V_{DD}$ sw: T_A
A can be more linear region



(+) Tunable
But need loop to tune it

- (-) Non linear vs V_{DS}
- (-) Not ESD robust
- (-) More parasitics

slightly less non linear

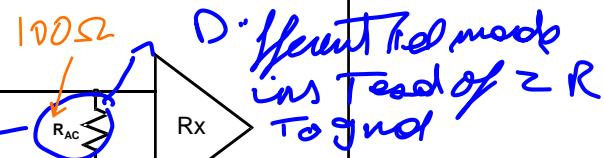
less non linear

less parasitics

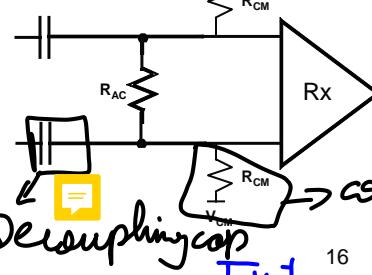
→ instead of being completely tunable well set only extra para.
Tune around a certain value to get desired values

AC vs. DC Termination

- With diff. can terminate to complement
 - High Z → lower power
 - See more shortly
- TX sets common-mode
 - Can be inconvenient
 - May need wide CM range
 - ↳ multi. ph. Rx
- AC-coupled + AC-term
 - Places some requirements on data though



what about common mode? Higher swing for same current V_{CM} ⇒ less power needed

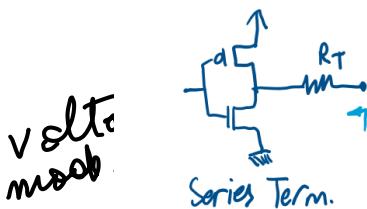


how to Deal with CM

get me out of here
Now con Tx
mean
That V_{CM} must be $T_x^+ + T_x^-$
at freq where cap is sc
 C_M / R_P is good

~~Supply Difference~~ \Rightarrow TX VDD is Different
 \Rightarrow Then $R_T \Rightarrow$ could cause this problem

TX Design: Series vs. Parallel Termination



For precise term. value:
 R_{ON} should be 0
 (of devices)



Parallel Term.
 (+) more precise term. value
 For precise term. value:
 r_o should be ∞
 (of devices)

nt
db

series to get higher
 R_{out}

(-) Less swing
 Since I always need some V_{DSAT}
 on my device for it to work in
 saturation

\Rightarrow more power consumption

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In the Series Termination:

To decrease R_{ON} , Increase W of devices,
 Resulting in more parasitic caps & more
 power dissipation

Very
 High
 Swings

Alphabet Soup

- LVDS, CML
- GTL, GTL+, RSL, ...

- VM, CM
- HCM, LCM

General
 Purpose IO
 Interface.

- All same basic principles
 - Look at two representative circuits to understand some of the more fundamental tradeoffs

Due to different termination schemes, we get different IO standards, like:

(Associated with signaling standards)

LVDS	= low-voltage differential signaling
CML	= current-mode logic
GTL	= Gunning transceiver logic (high-swing IO)
RSL	= Rambus signal logic

(Different implementation styles)

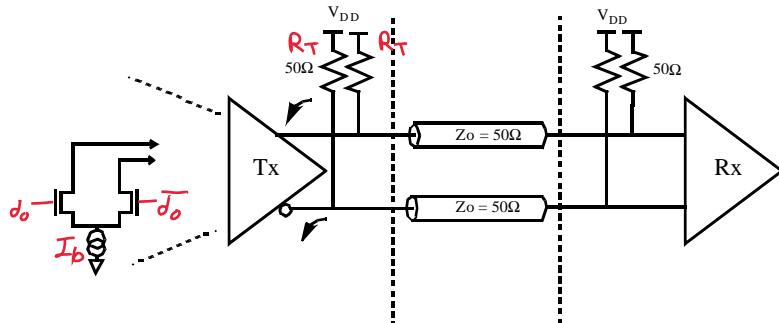
VM & CM	= Voltage-mode & Current-mode
HCM & LCM	= High-common-mode & Low-common-mode

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CML TX + RX Term



$$\checkmark V_{\text{swing, PP, diff}} = \left(I_b \frac{R_T}{2} \right) 2 \\ = I_b R_T$$

when current is limited to one Si Di
Double-terminated on-chip
 $V_{\text{swing}} = [I_b \times \frac{R_T}{2}] \times 2$

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Differential Peak To Peak

$$R_T / 50\Omega$$

$$50\Omega$$

① when one Si Di is Driven for a long Time

$$V_x = V_{DD} - V_{TH} - V_{STAR}$$

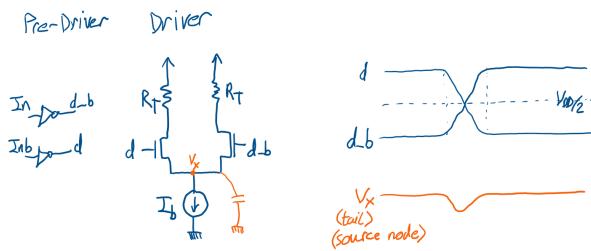
$$\text{When } D = D_{\text{on}} = \frac{V_{DD}}{2}$$

$$V_x = \frac{V_{DD}}{2} - V_{TH} - V_{STAR}$$

S should be lower so the driver's current I isn't off

& to get $\frac{I_b}{2}$ in both & large cap in node x cause long time to be just

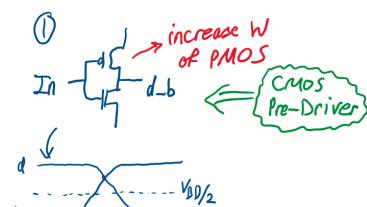
Side Note: Pre-Driver



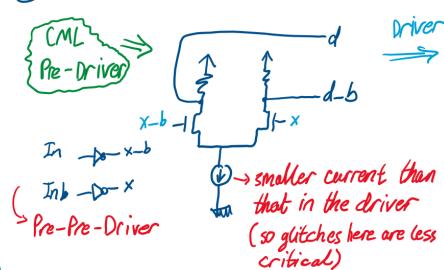
When both d & $d-b$ are switching, the input transistors of the driver may be less ON, which causes a glitch on V_x .

This glitch can cause
 ① CM error
 ② glitches on the supply → This is bad if I have many switching drivers

Some ideas for Pre-Driver:
(to adjust the input common mode, so the transistors won't be OFF together)



① increase W of PMOS

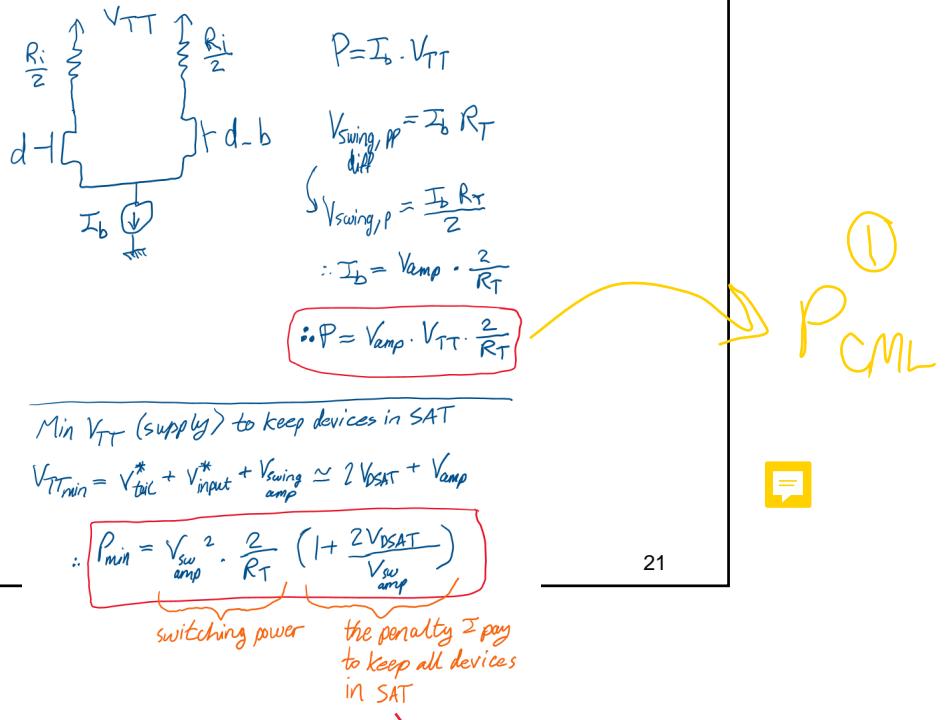


② decrease the input swing

③ smaller current than that in the driver
(so glitches here are less critical)

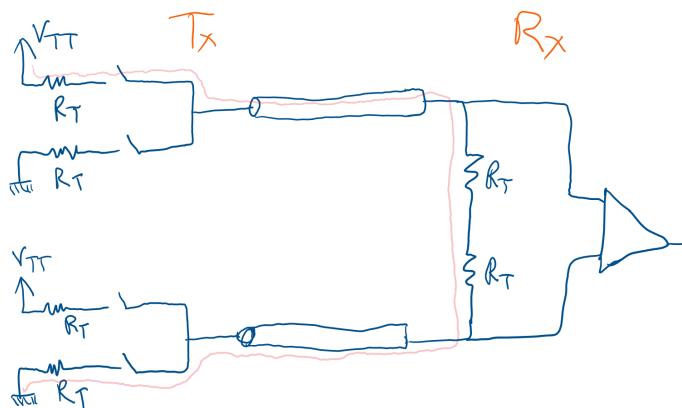
② V_x glitch may cause glitches in current flowing to Supply which will cause every thing electric to modulate.

CML Power Consumption

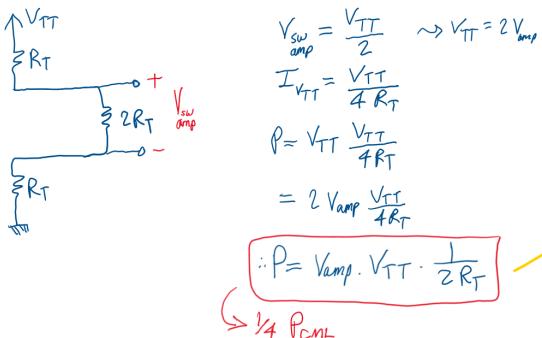


Differential VM TX + RX

- Main motivation: can reduce power for same swing/supply



Simplified Model And Power



(2)
 P_{VM}

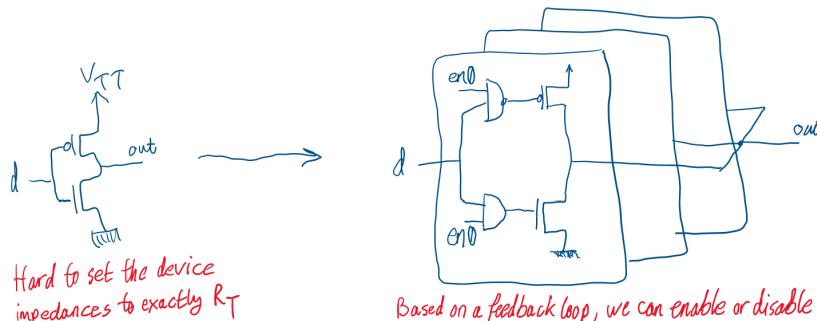
$$V_{TT_{min}} = 2V_{SW_amp}$$

$$\therefore P_{min} = \frac{V_{SW_amp}^2}{R_T}$$

There's no V_{OSAT} penalty as in CML case

Bad News: Extra Complexity

- Driver impedance (termination) now set totally by devices
 - Some sort of impedance control is critical
- “High-swing” driver:

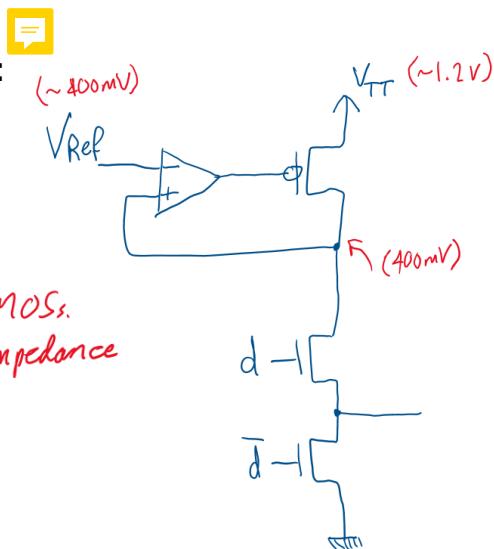


Low-Swing VM Driver

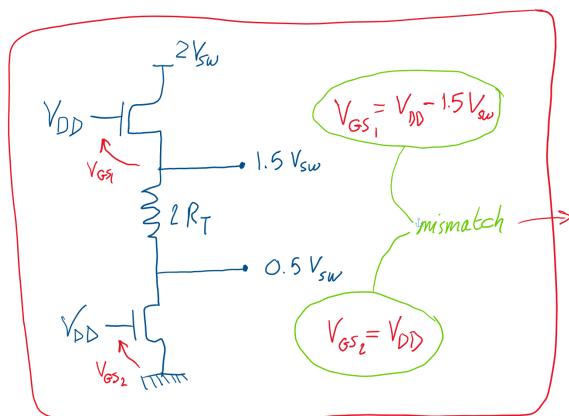
- Old standards often required large swings (>1V diff. p2p)
 - More modern designs use much lower swings (~200-400mV diff. p2p) to save power

- Low-swing VM driver:

Both the pullup & pulldown are NMOSs.
There will be asymmetry in their impedance values. (V_{gs} 's are different)

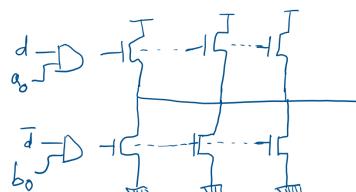


Impedance Control



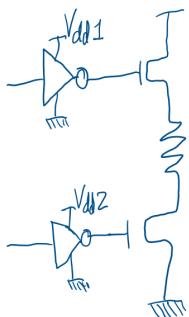
① Digital Approach:

A feed back loop for each of the pullup & the pulldown will digitally control the pullup & pulldown impedances

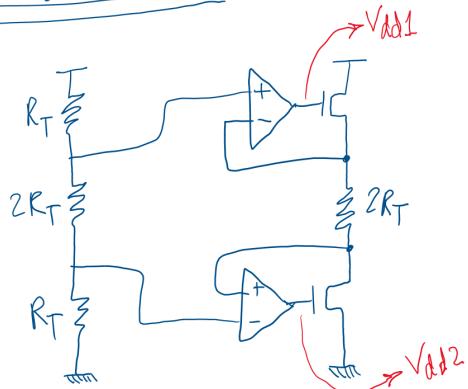


Another Approach

① Different Supplies



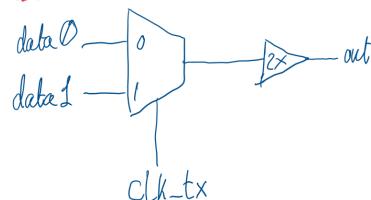
③ Analog Approach:



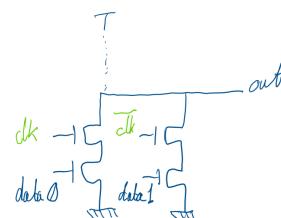
Serialization: Input vs. Output

- On-chip clocks often slower than off-chip data-rates
 - Need to take a set of parallel on-chip data and serialize it
- Can serialize either at input of TX or at final output

parallel
data

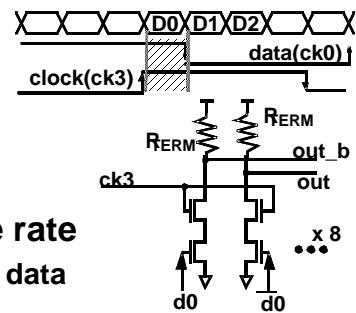


Serialization pushed
to the output driver



Serialization: Input vs. Output

- Input ser. requires on-chip circuitry to run at full line rate
 - May lead to high power consumption
 - In older technologies (0.35um) was hard to support high-freq. clocks
- Output ser. moved burden at pad
 - At the time was highest BW
- Limit in both designs: edge rate
 - Either for the clock or for the data



Basic TX Final Notes

- Usually need many peripheral controls
 - Z_0 , edge-rate, etc.
- Keep tuning out of the high-speed signal path
 - $P(\text{High-speed, low res. + low-speed, high-res.}) \ll P(\text{high-speed, high-res.})$

Basic TX Final Notes

- Lots of research focused on reduced signaling power
 - I.e., power spent by actual final driver
- Watch out for “overhead” (pre-drivers)
 - Especially with emerging low-swing designs, overhead can actually dominate
 - P_{sig} (400mV diff. p2p):
 - $P_{digital}$ (100 min. sized inverters @ 10GHz): → More
- More on this later

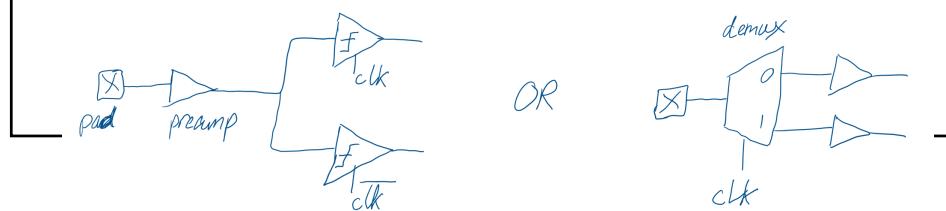
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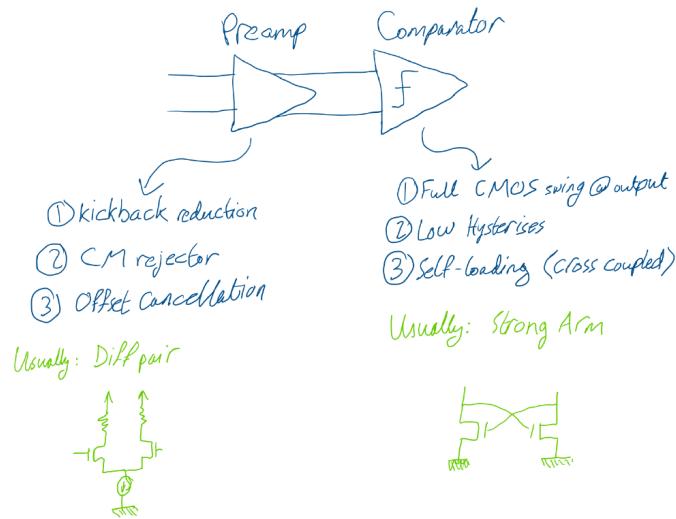
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Basic RX

- Simplest: RX is just a comparator @ f_{bit}
 - (Clocking later)
- Key things to watch out for:
 - High sensitivity (low noise, low offset/hysteresis)
 - Common-mode input range
 - Supply/common-mode rejection
 - Max. clock rate
 - Power consumption



Typical Design

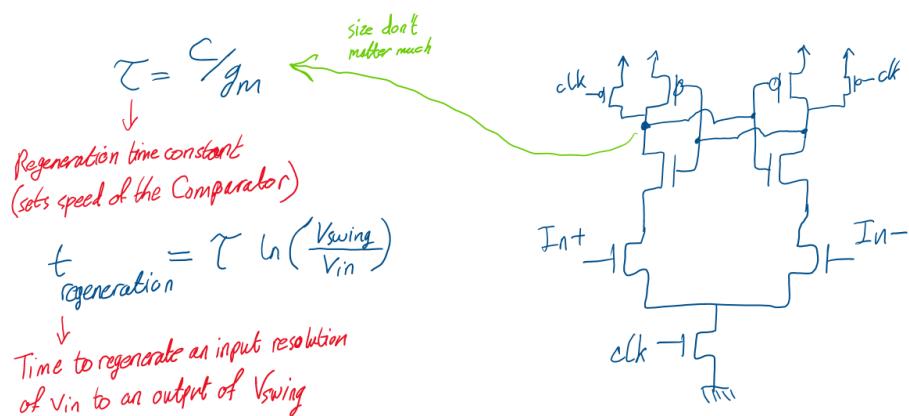


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StrongArm Review



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Higher Speeds

ex/ $V_{swing} = 1V$ (rail-to-rail)

$V_{in} = 100mV$

$$\therefore t_{reg} = 2.3\tau$$

min clk Resolution
 $2.3\tau \rightarrow 100mV$
 $4.3\tau \rightarrow 18mV$
 $6.4\tau \rightarrow 1mV$

* τ can be smaller in CML comparators.