# EE290C – Spring 2011

## Lecture 2: High-Speed Link Overview and Environment


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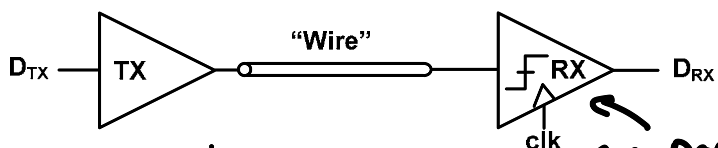
## Most Basic "Link"




comparator with a clk???

assuming we are only dealing with sa

we only need to compare with a Threshold

- Keep in mind that your goal is to receive the same bits that were sent…



what is Timing error or clock jitter => well IT'S like amp To phase conversion => I understand nothing => The error in or noise voltage signal is causing uncertainty in Time which because we could Tell The Time from voltage signal, They are basically the same Thing, only Different mechanism is causing error.

## Why Wouldn't You Get What You Sent?

(1) Noise: → @Rx, the received signal amplitude should be large in comparison to the voltage noise

A- in Voltage

B- in Timing ← need to check bit value at right time.

(2) Distortion Ex ISI

(3) Interference (more prominent in Wireless systems)

A- From Other signals => coupling between links
less a problem than in wireless

B- Power supply

* Noise is random (has statistical distributions associated with it),
While Interference is more deterministic. but you end up modeling as statistically

more generalized

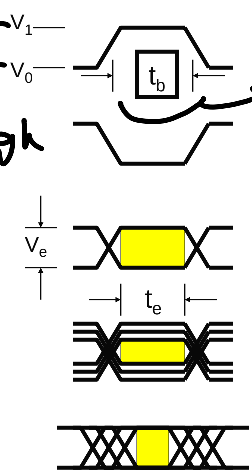
# intersymbol interference => like having a LPF that smooth the signal ⎍ => ∩



→ Reflection due to unmatched impedance are considered a type of distortion

## Eye Diagrams

space between low & High level




This is a "1"

Time to correctly capture the bit.

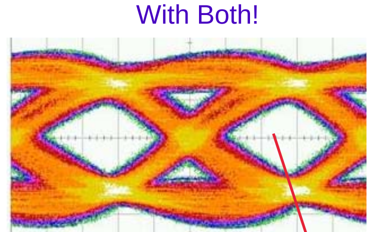
This is a "0"

Eye Opening - space between 1 and 0 => Took an arbitrary nb of bit & put on top of each other & look at it one at a time.

With Both!

With voltage noise

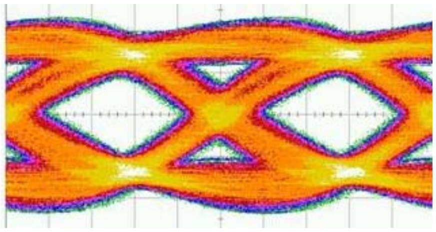
With timing noise
Jitter

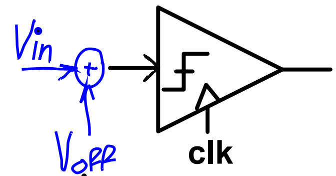




The bigger the eye opening is, the better => clean transition in term of transition & time

# BER






The erfc Func is related To The CDF = P[noise <= a certain value]
φ(x)
so erfc is P[ noise > certain value ]

- BER = Bit Error Rate
  - Average # of wrong received bits / total transmitted bits
- Simplified example: (voltage only)

$$BER = \frac{1}{2} erfc\left(\frac{V_{in,ampl} - V_{off}}{\sqrt{2}\sigma_{noise}}\right)$$

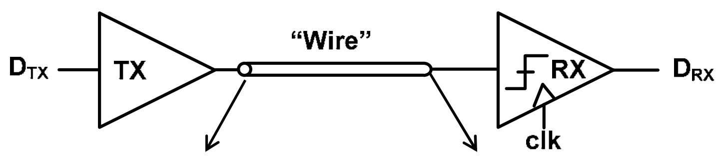
Assuming the noise follows a Gaussian Distribution

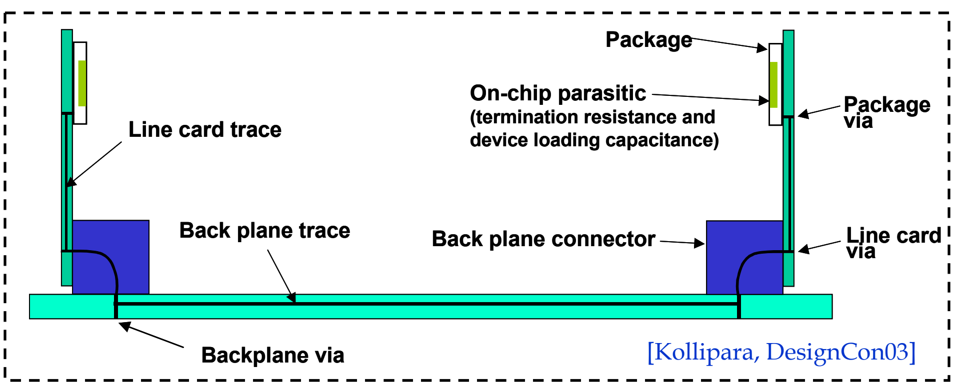
- BER = $10^{-12}$: $(V_{in,ampl} - V_{off}) = 7\sigma_n$
- BER = $10^{-20}$: $(V_{in,ampl} - V_{off}) = 9.25\sigma_n$



→ why is This range important ⇒ how D: D we Decide that ⇒ well the answer that how much we need To Tolerate error ⇒ For a 10 Gb/S → how many error bit ⇒ 1 For every 100S

# What About That "Wire"




[Kollipara, DesignCon03]

## "Wire" Models

- ICs: usually use lumped models for wires
  - Capacitance almost always matters
  - Sometimes resistance
  - Less often inductance
- Works because dimensions << λ "Wavelength (of interest)"
  - Let's look at some example λ and size numbers for links

$$c = \lambda f$$



## Links and Lengths

1
- Chip to chip on a PCB → Some
  - "Short" and relatively well controlled
  - Packaging usually limits speed ⇒ will be Discussed #
- Distance: 3-6" inches #
- Data-rate: 1-12Gb/s #
  - Wavelength in free space = 2" - 24" → $\varepsilon_0$ of FR4 is 4,2 #
  - Wavelength on PCB (FR4) = 1" - 12" → well we Know That The speed gets ... of the Dielectric $\sqrt{\varepsilon_0}$ $\lambda = \frac{c}{f}$

can I have a lumped element well actually NO ☹ ⇒ λ ↓ by an order of magnitude & IT will be further discussed in the future

1/6GHz

1/12GHz

For 12Gb/s

Assuming frequency = 6 GHz = $6\times10^9$ Hz

(assume NRZ)

1 bit

$\therefore \lambda = \frac{c}{f} = \frac{3\times10^8}{6\times10^9} = 0.05m \simeq 2''$ (inches)

0.3 m

×2

inches

So can we treat things in wire as lumped when λ is smaller ???

## Links and Lengths

2

- Cables connecting chips on two different PCBs ⇒ Different PCB Ex USB, between PC & some router
  - Cables are lossy, but relatively clean if coax
  - Connector transitions usually the bad part ⇒ Tough to keep good signal integrity.
- Distance: ~0.5m up to ~10's of m (Ethernet) ↑ multi level signaling #
- Data-rate: 1-10Gb/s
  - Wavelength in free space = 0.6m - 6m
  - Wavelength on PCB (FR4) = 0.3m - 3m



## Links and Lengths

3

If Backbone board is master then the other board is Back Board

- High-speed board-to-board connectors links
  - Daughtercard (mezzanine-type)
  - Backplane connectors
- Distance: 8" up to ~40"
- Data-rate: 5-20Gb/s
  - Wavelength in free space = ... - 5" ⇒ λ are small
  - Wavelength on PCB (FR4) =

So ... We need to go to transmission lines

# Transmission Lines Quick Review

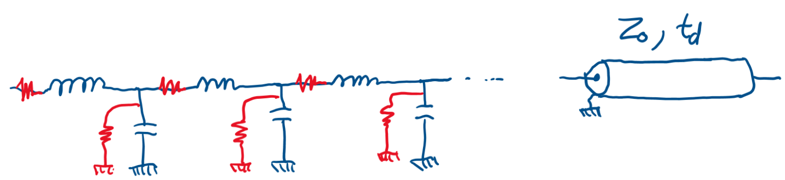
→ physical length

- **Delay** ← length, $\sqrt{\varepsilon_r}$ → dielectric constant
- **Characteristic Impedance** ← $\sqrt{L/C}$
- **Reflections**
- **Loss**

Parasitic conductance

Characteristic Impedance

Depend on freq.



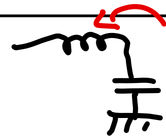

in

Parasitic Resistance

model a Transmission line



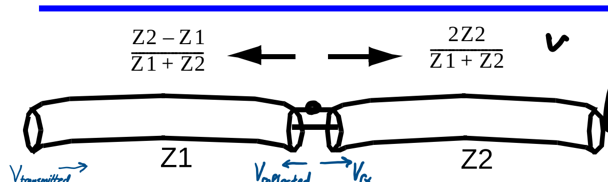
LC Model



energy stored as magnetic field $E=\frac{1}{2}LI^2$

& Then transferred as an electric field $\Rightarrow E=\frac{1}{2}CV^2$ #

# Reflections




(1) Energy conserved

(2) Voltages equal

$V_{transmitted} = V_{reflected} + V_{rx}$

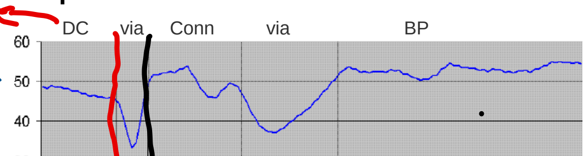
- **Sources of Reflections** : **Z - Discontinuities** ?
  - **PCB Z mismatch**
  - **Connector Z mismatch**
  - **Vias (through) Z mismatch**
  - **Device parasitics - effective Z mismatch**

$V_{transmitted} = V_{reflect} + V_{Rx}$

Different c/cs of TL causes Reflection

Daughter card

50Ω impedance →




→ Distance

$Z_0$,

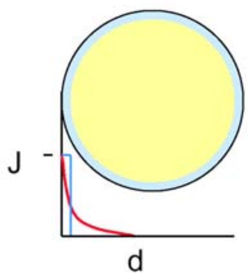
↳ Discontinuity #

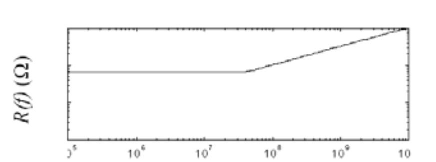
1

# Skin Effect ⇒ First Type of loss mechanism

- At high $f$, current crowds along the surface of the conductor ⇒
- Skin depth proportional to $f^{-1/2}$
- Model as if skin is $\delta$ thick
- Starts when skin depth equals conductor radius ($f_s$)

$$\delta = (\pi f \mu \sigma)^{-1/2}$$




$$J = \exp\left(-\frac{d}{\delta}\right)$$

Figure © 2001 Bill Dally

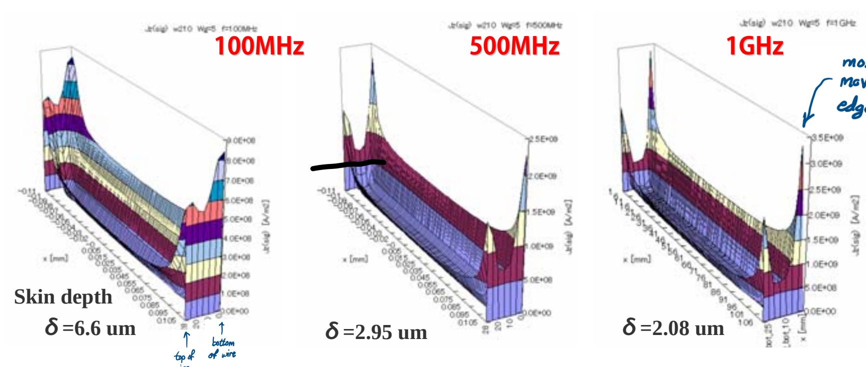


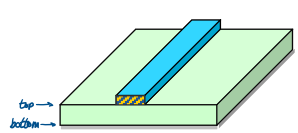
R (or the loss) increases as frequency increases

Current tends to move along the edge of the conductor as frequency increases. [Skin Effect]

→ less inductance instead of moving from the middle with more inductance in the way current tends to move in lower imp ⇒ lower effective thickness R↑ loss↑

# Skin Effect cont'd




W=210um、t=28um

cause I want that low inductance return path

1

2

## Dielectric Loss ⇒ second Type of loss in TL

- **High frequency signals jiggle molecules in the insulator**
  - **Insulator absorbs energy**
- **Effect is approximately linear with frequency**
  - **Modeled as conductance term in transmission line equations**
- **Dielectric loss often specified in terms of loss tangent**
  - **Transfer function =** $e^{-\alpha_D Length}$

$$\tan\delta = \frac{G}{\omega C}$$

$$\alpha_D = \frac{GZ_0}{2} = \pi f \tan\delta\sqrt{LC} = \frac{\pi\sqrt{\varepsilon_r} f \tan\delta}{c}$$

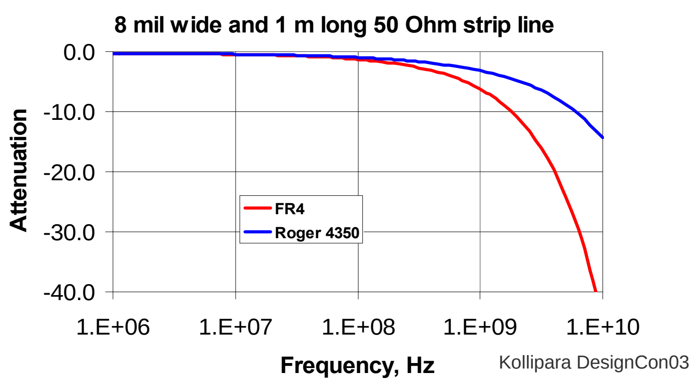
| material | tan δ |
|---|---|
| FR4 | 0.035 |
| Polyimide | 0.025 |
| GETEK | 0.010 |
| Teflon | 0.001 |

Table © 2001 Bill Dally



The molecule gets rotated by electric field of The signal & part of signal gets absorbed & Dissipated as Heat as
as frequency ↑↑ rotation ↑ absorbtion ↑ loss ↑

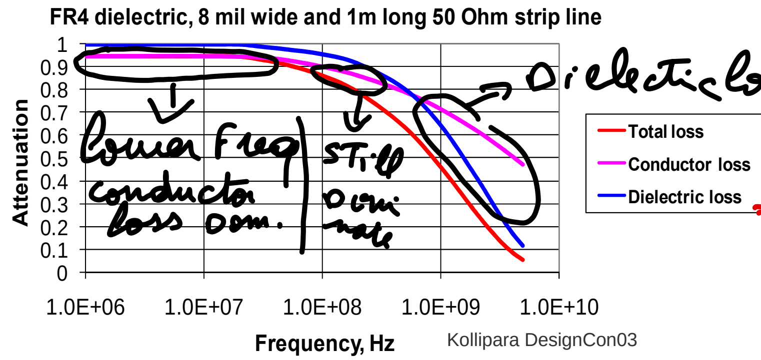
## Dielectric Loss cont'd




Kollipara DesignCon03

- **FR4 cheapest – most widely used**
- **Rogers is most expensive –high-end systems**
  - **May not matter that much due to surface roughness**

# Skin + Dielectric Losses

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Dielectric loss Dominates

⇒ Skin loss $\propto \sqrt{f}$

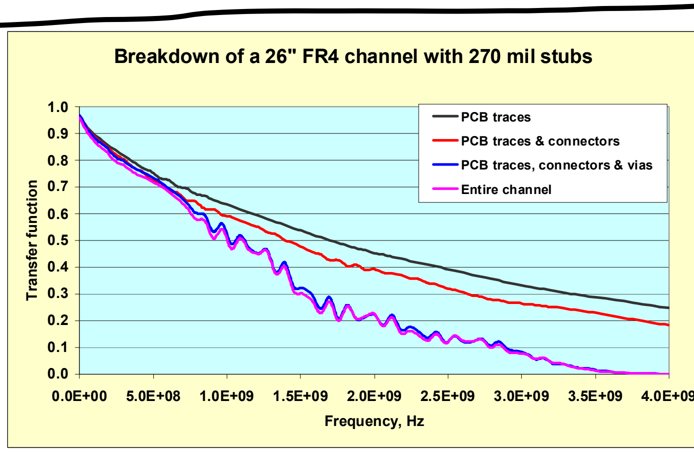
⇒ $\propto f$

- Skin Loss $\propto \sqrt{f}$
- Dielectric loss $\propto f$ : bigger issue at high $f$

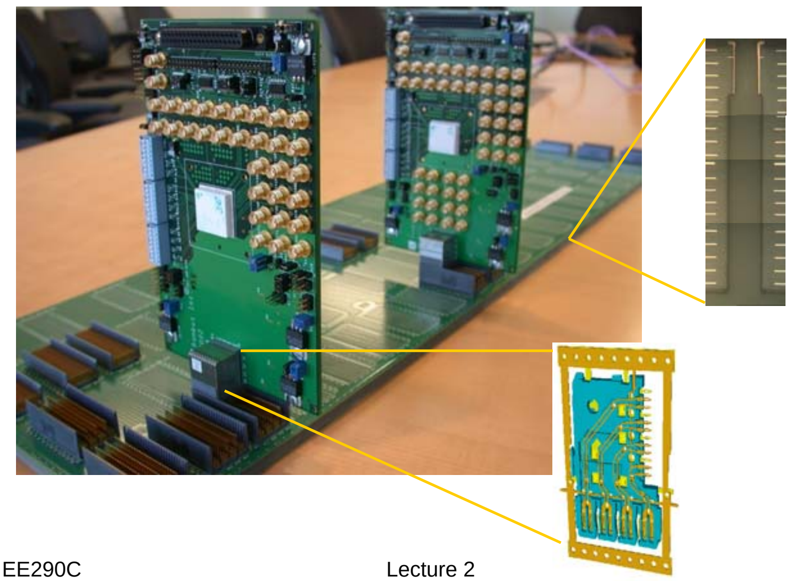


# Everything Together: S21

- S21: ratio of received vs. transmitted signals



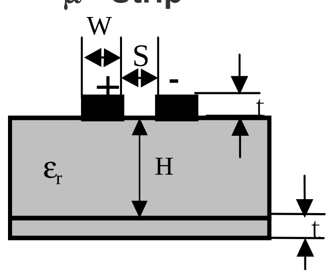
## Real Backplane



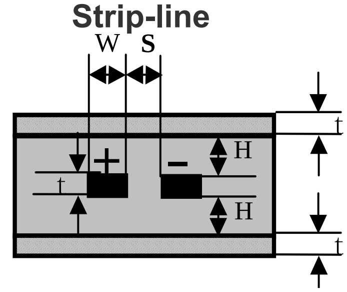


## Practical PCB Differential Lines

μ - Strip




Strip-line

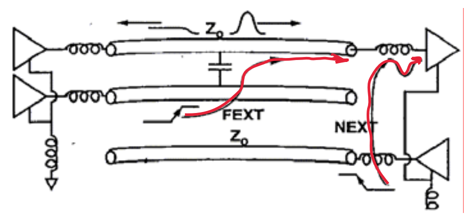



- **Differential signaling has nice properties**
  - **Many sources of noise can be made common-mode**
  - **Differential impedance raised as f(mutuals) between wires** ≡ have sTrong coupling beTween The 2 Different signal That wants To be Differential & less couple with The rest of The world
  - **Strong mutual L, C can improve immunity**

i will give an example and answer me if i am right i have a tx that will send a signal an let's assume there is some discontinutiy in the channel so ofcourse there will reflected signal that will couple into another wire that have a signal moving towrds the rx while the reflcted will move towrds the tx and will add di=estructvly as noise to the victim signale
20:07

3

## Coupling → Crosstalk…



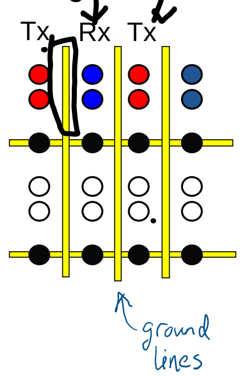

- "Near-end" xtalk: NEXT (reverse wave)
- "Far-end" xtalk: FEXT (forward wave) Same IDea but The agressor signal is in the same Direction as Victim
- NEXT in particular can be very destructive
  - Full swing TX vs. attenuated RX signal
- Good news: can control through design
  - NEXT typically 3-6%, FEXT typically 1-3%

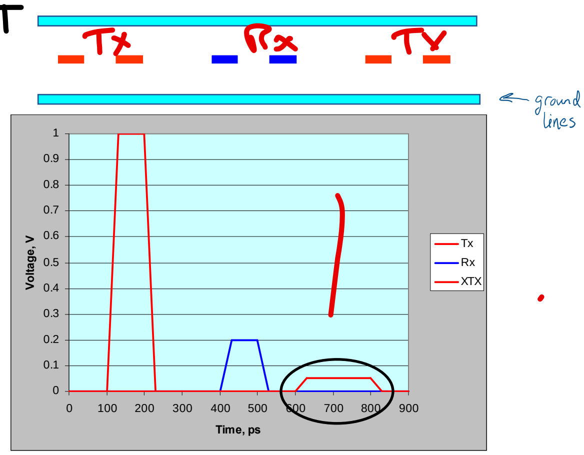


## NEXT: What Not To Do

Doc said That gnd may not escisT

For The vertical side so

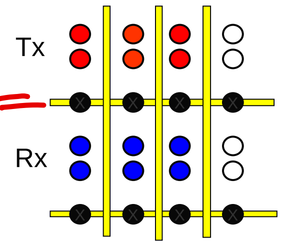


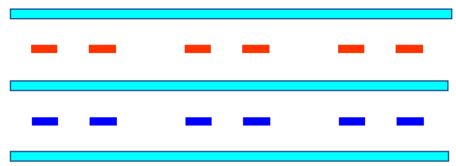


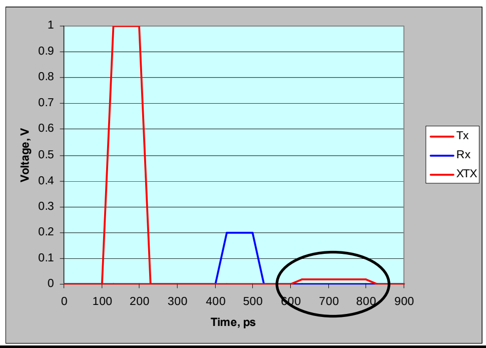

This Design is bad → High crossTalk → There Will be Discontinuity

# NEXT: Better Design



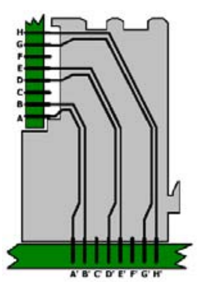

gnd shield which will absorb most of crossTalk #








# Connectors Particularly Tough




| HSD 8 Propagation Delay<br>Calculated from length | |
|---|---|
| H → H' | 200ps |
| G → G' | 194ps |
| E → E' | 151ps |
| D → D' | 145ps |
| B → B' | 108ps |
| A → A' | 99ps |

| | NEXT | FEXT |
|---|---|---|
| | 55 ps (20-80%) | 55 ps (20-80%) |
| | 80ps (10-90%) | 80ps (10-90%) |
| AB | 4.4% | 3.7% |
| DF | 3.3% | 2.6% |
| GH | 3.3% | 2.6% |
| JK | 4.3% | 3.5% |

how much Diff signal aren't aligned

- **Tight footprint constraints**
- **Hard to match pairs and even individual lines**
  - **May compensate skew on line card**
- **Also big source of impedance discontinuities**

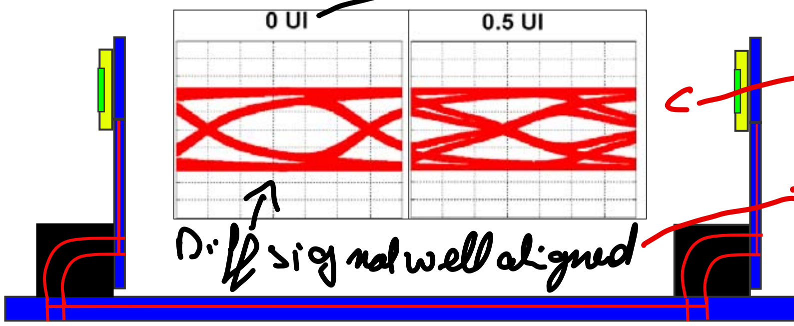
skew

+

−

## Skew Within Link

unit interval = bit Time




Diff signal well aligned

result

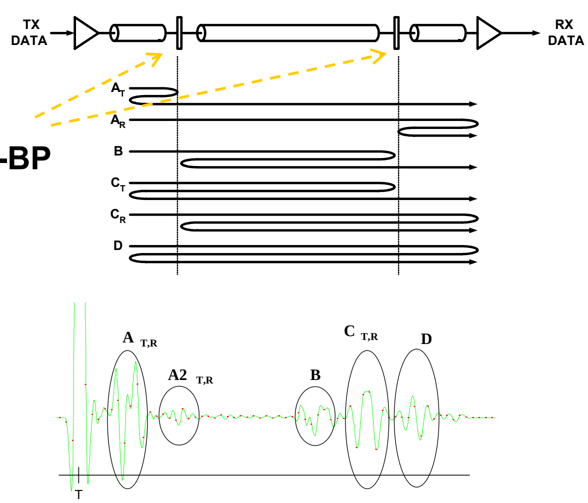
like shifting one bit from each other

- Need very tight control to maintain constant % of bit time => must be smaller than this
- 1% skew on 30” line → 50ps $\boxed{\text{skew}}$ => Time offset
  - Half of a bit time at 10Gb/s
- Good news: connectors relatively “short” (~200ps)

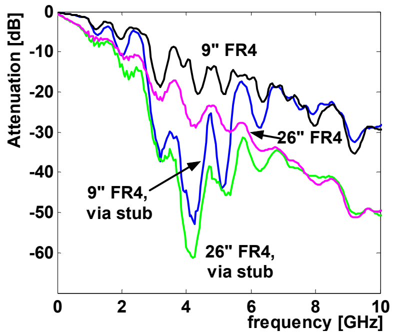


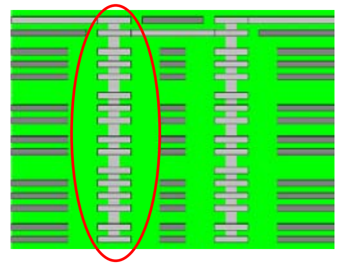
## Reflections Revisited

Connector-BP transitions



# Reflections Due To Via Stub → floated TL



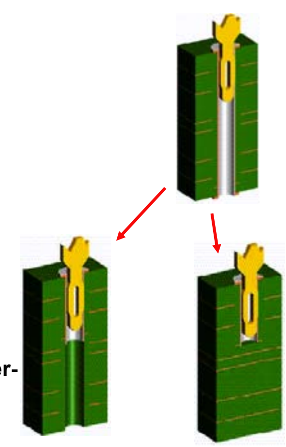
- "Stub": extra piece of T-line hanging off main path
- Usually leads to resonance (notch)
  - Especially on thick backplanes, vias are a big culprit



# Minimizing Via Stubs

- Thinner PCB?


- Better vias?

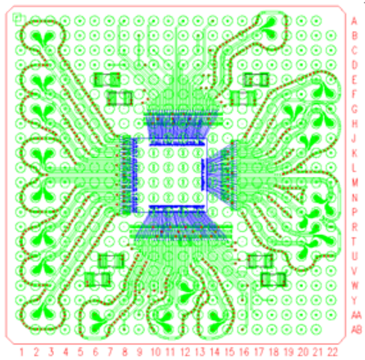


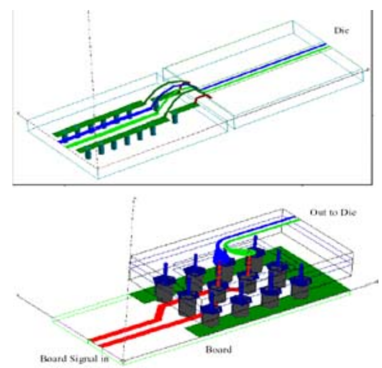
counter-bored

blind via

- All expensive: 1.1-2x

## Summary

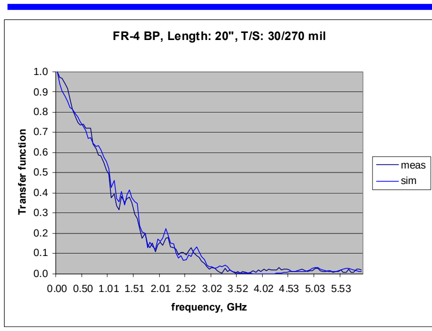


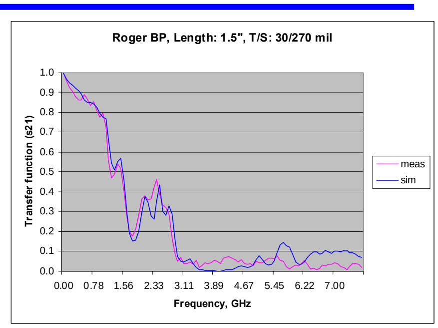



- **Packaging, chip connection, etc. can all have an effect…**
  - **Entire conferences dedicated to "signal integrity" (SI)**



## Implications




- **Need to know range of channels you will face**
  - **Drives design of the link circuitry**
  - **Start diving in to that next lecture**
- **Don't be a pure "circuit weenie"**
  - **Simple fixes to channel may go a long way…**