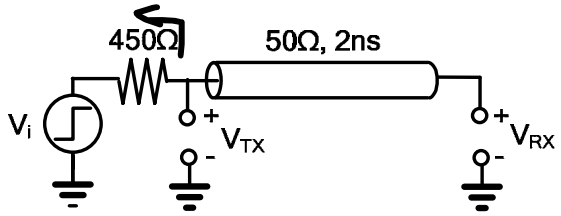
UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

E. Alon **Homework #1** **EE 290C**
Due Thursday, February 3, 2011

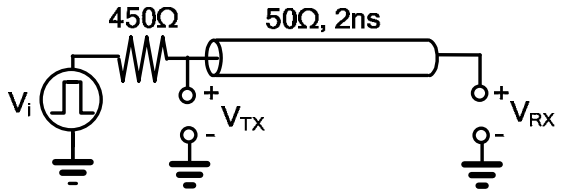
1. This problem will examine the a common situation where (relatively small) inverters are used to drive and receive off-chip signals.

   a. As shown below, the TX inverter's output resistance is assumed to be 450Ω, while the receiver is assumed to present an open circuit at its input.



   Assuming that the input voltage V_i is a step from 0V to 1V, sketch a plot of V_{TX} and V_{RX} vs. time.

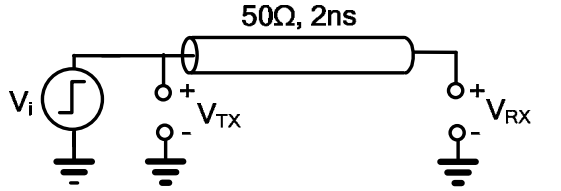
   b. Now let's look at what happens if we send a pulse (0V to 1V back to 0V) of width T_{bit} down the line. Sketch V_{TX} and V_{RX} for T_{bit} = 80ns and for T_{bit} = 10ns.



   c. Assuming that the receiver's threshold is set at exactly 0.5V (and that the receiver is infinitely sensitive – i.e., it switches from 0 to 1 at exactly the threshold), approximately what is the maximum bit-rate (i.e., $1/T_{bit}$) that you could operate this link?

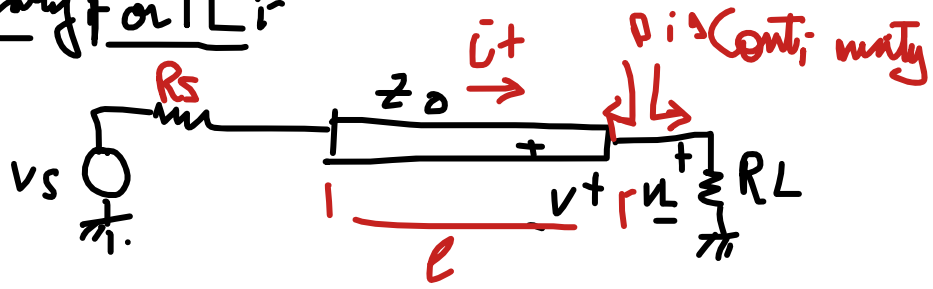
   d. Assuming that the ε_r of the transmission line's dielectric is 4 and under the same conditions as part c., what is the maximum distance this link can operate over at 1Gb/s?

   e. Interestingly, decreasing the output impedance of the inverter driver too much can have even more detrimental effects from the standpoint of the ability of the link to communicate correctly



   Shown above is a new model of the link where it is assumed that the output impedance of the inverter is zero. Sketch a plot of V_{TX} and V_{RX} vs. time for a step input voltage V_i from 0V to 1V.

Summary For TL ir



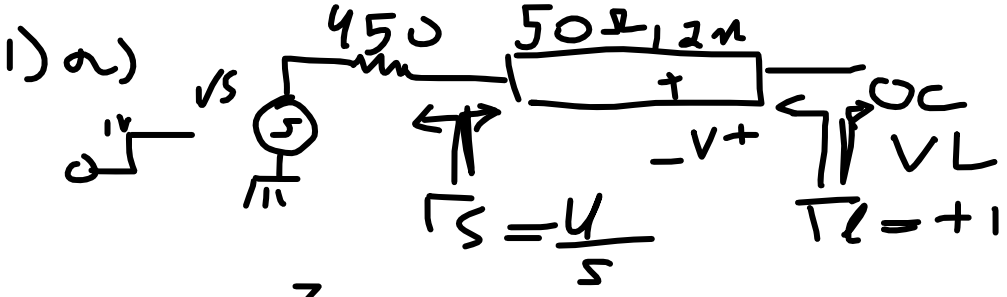
$$i+ = \frac{V_1^+}{Z_0} = \frac{V_S}{Z_0+R_S} \qquad i_L = \frac{V_L}{R_L}$$

$$V_L = V^+_{(l,t)} + V^-(l,t)$$

$$i_L = \frac{V^+(l,t)}{Z_0} - \frac{V^-(l,t)}{Z_0} = \frac{V_L}{R_L}$$

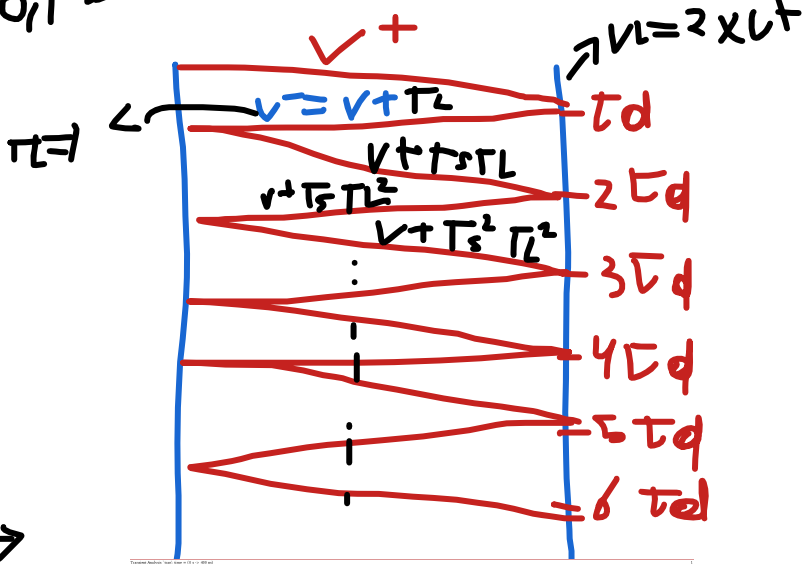
$$\text{Solve} \Rightarrow V_L = \frac{2V^+}{\left[1+\frac{Z_0}{R_L}\right]} = \frac{2V^-}{\left[1+\frac{Z_0}{R_L}\right]}$$

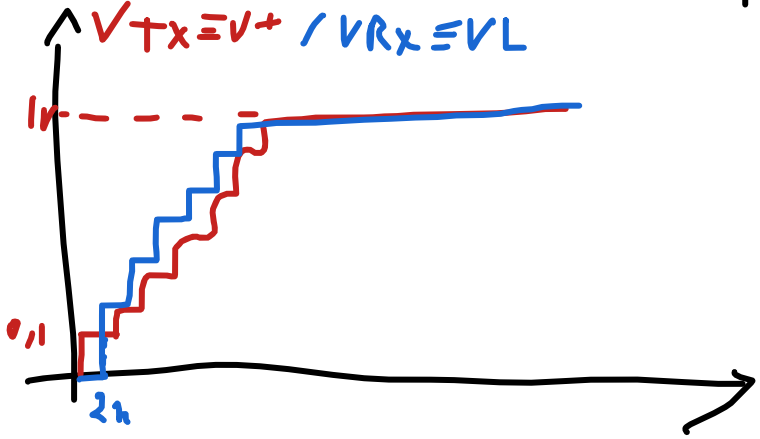
1) a)

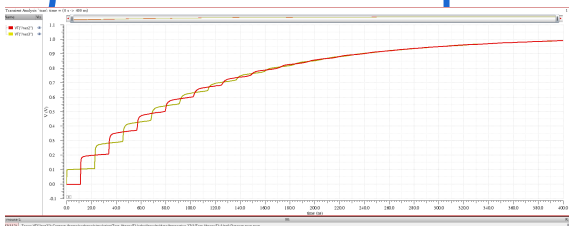


$$V^+ = \frac{Z_0}{Z_0+R_S} V_S = \frac{1}{5} V_S = 0{,}1\,V$$

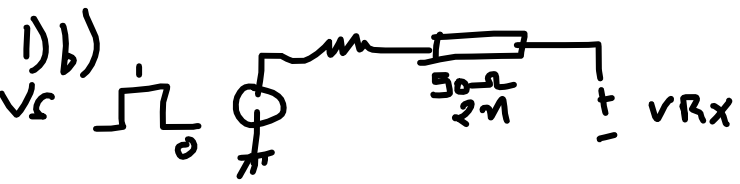
$$V_L = 2V^+ = 0{,}2\,V$$







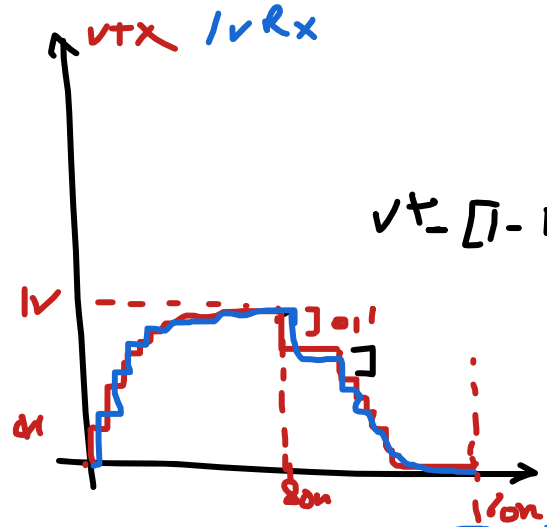
1) b)



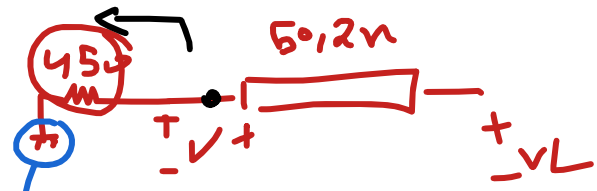
@ A cst 80n same as last

$T_{bit} = 80n$

$\Gamma_s = \frac{450 - 50}{500}$



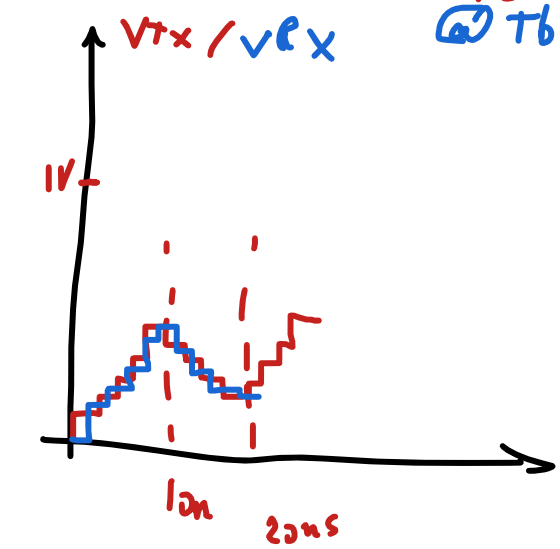
$V^+ - [1 - \Gamma_s] V^+$



$\Gamma_s = \frac{450 - 50}{500} = \frac{4}{5}$

$\Gamma_l = -1$

@ $T_{bit} = 10ns$



VRX

1) c) when $V_L \Rightarrow 0,5V \Rightarrow$ IT switches to 1V

↳ at 2n $\Rightarrow V_L = 0,2$

at 6n $\Rightarrow V_L = 0,2 + 2 \times V^+ \times \Gamma_s \times \Gamma_l$

$= 0,36$

at 10n $\Rightarrow 0,36 + 2 \times V^+ \times \Gamma_s^2 \times \Gamma_l^2$

$= 0,488$

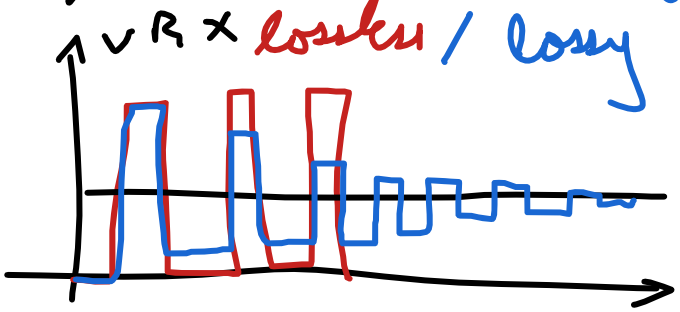
at 14n $\Rightarrow 0,488 + 2 \times V^+ \times \Gamma_l^3 \Gamma_s^3$

$= 0,590 \Longrightarrow 14n = T_{bit}$

d) $\lambda = \frac{c}{f} = \frac{3 \times 10^8}{10^9} = \boxed{0{,}3\ m}$

$\varepsilon_r = 4 \Rightarrow \lambda' = 0{,}15\ m$

e) if TL was lossless/lossy

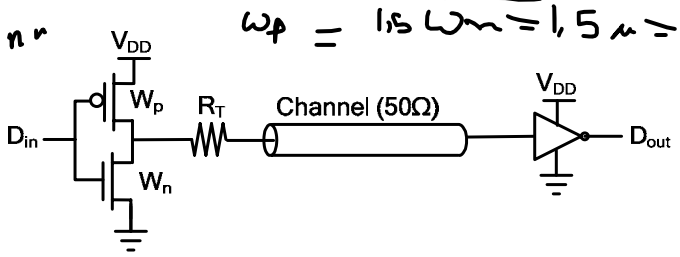


I tested on Cadence with L=65nm

2. In this problem we look at the design of the basic link shown below. Throughout the problem, you can use the simple switch model (from EE141) for the transistors with the following parameters: C_G = 2fF/µm, C_D = 1fF/µm, $R_{sq,n}$ = 25kΩ/□, $R_{sq,p}$ = 37.5kΩ/□, L=40nm, and V_{DD} = 1V.

① $R_{on} = R_{\square} \times \frac{40nm}{W_n}$; $R_{\square}$ = 25K, W_n = 1µm ; assume 1K

$W_p = 1.5 W_n = 1.5\mu = \frac{R_{Dp}}{R_{Dn}}$



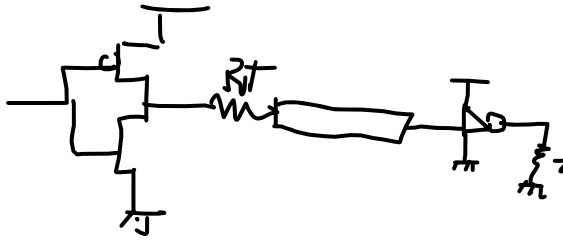
a. Show how you would modify the basic link schematic shown above in order to terminate the channel at the receiver end with 50Ω. You should also assume that the switching point of the receiver's inverter is $V_{DD}/2$ (i.e., 0.5V) and ensure that your termination provides an appropriate bias point for the inverter.

b. Assuming that we'd like the transmitter to be matched to the channel (i.e., how have a total output impedance of 50Ω), and that k_{active} represents the percentage of the transmitter's output impedance that is due to the transistors (and not due to the explicit resistor R_T), provide an expression for W_p and W_n as a function of k_{active}.

c. Based on your expression in part b., assuming that this link operates at 5Gb/s, what is the average total power consumed by the driver? You should ignore the parasitics of the receiver's inverter, but you should include the dynamic power consumed by driving the gate inputs of the transmitter.

d. Next we will look at actually constructing the receiver's termination resistor. For simplicity we will assume that the transistor characteristics don't vary, but that any explicit (unsilicided poly) resistors we use vary +/-20%, and that we'd like to control the termination to be accurate to within 5% (i.e., the resistance should be equal to 50Ω +/- 2.5Ω). Draw a design that achieves this goal; you don't need to worry about showing the loop that controls the resistance, but you should provide values for the components (e.g., transistor widths, resistor nominal values, etc.).

2) a)



→ pull down mist of but must take inverter Ron Impin Cons.

2) b) $R_{out} = R_{on} + R_T$ when input is high ⇒ Ron is Ronn

↳ 50 Ω ↳ $\frac{R_{sin}}{2}$ = 50K " " " " low ⇒ Ron is Ronp

at switching both are conducting so we can assume $R_{on} = \frac{R_{single}}{2}$

but remember $W_{nP} = W_{nn} \times 1.5$

if we assume that $R_{single} = 50 \times k_{active} \times 2$

$R_T + 50K = R_{out}$ (50)

from equ ①&② → $R_T = 50[1-K]$ ②

↳ $W_n = \frac{500}{K}$ $W_p = \frac{750}{K}$

(c) $Poly = f \cdot C_{in} \cdot VD^2D$

$= 5G \quad [wn + wp]CG \cdot 1$

Dynamic power $= 5 \times 10^9 \times \frac{1}{K} \times 2F = \frac{12,5m}{K}$ #