NEURAL REPEATER
Analog Circuit Design to Bridge Spinal Breaks

Melissa Alvarez, Dan Buscaglia, Aratrika Ghatak, Kirsten Scheller
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ABSTRACT

There are a number of promising solutions aimed at bridging full or partial breaks in the spinal cord. These range from tissue engineering and cell regeneration to robotics and circuit-assisted solutions. Brain Computer Interfaces and direct electrical stimulation are among modern solutions to observe and replicate functional neural circuits.[1] Here we propose an analog circuit for use as a neural repeater. This consists of a low power, low noise amplifier which amplifies neural circuits above a break. This is followed by a comparator to filter out neural spikes and a stimulation circuit to output pulses below the break. An external clock keeps the system synchronized in real time. We discuss each of these circuits in detail and outline how the circuit's performance was simulated. The final design is able to significantly amplify inputted signals so that they can be filtered and replicated to downstream neurons. Applications include addressing full or partial paralysis and diseases which affect neural circuits for motor control of movement.

INTRODUCTION

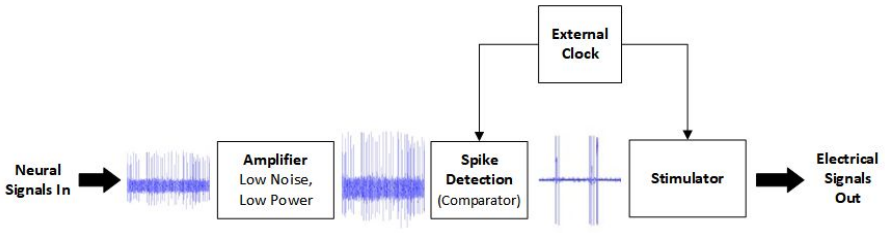


Figure 1. Full System Block Diagram

Processing neural signals through analog circuit design presents a number of challenges. In order to minimize adverse response from the host, devices for implantation must be small in size and have low power consumption. Here we design analog circuits for each of the components needed to bridge a break in the spinal cord. A full top-level design and schematics for each stage are shown on the spec sheet, included at the end of this report.

[1] Yang, B., Zhang, F., Cheng, F. *et al.* Strategies and prospects of effective neural circuits reconstruction after spinal cord injury. *Cell Death Dis* 11, 439. June 2020.

Neural signals in the body are typically on the order of less than 100 microvolts and stay within a 10kHz band. Therefore, our first stage consists of two amplifiers. The role of these amplifiers is to set a low noise level, filter out high frequency noise, and significantly amplify inputted neural spikes. In the second stage we include a spike detector. This is a real time comparator that determines if the neuron is “on” or “off.” Lastly, this information is fed into a spike simulator, which outputs electrical spikes after the spinal break. This activity of the full circuit was observed by inducing a current at the amplifier’s input and observing a resistor placed at the spike simulator’s output.

Neural signals typically have low signal-to-noise ratios, requiring low noise amplifiers to discern neural spikes. Even when not actively transmitting signals, neural membranes have a high level of activity, associated with resistive elements and ion channels across their membranes. Neurons are considered to spike when their membrane potential goes beyond a base threshold level.[2] Identifying these spikes and producing a high SNR is a key aspect of designing neural sensing devices. The activity of Na+ and K+ ion channels on neural membranes can be simulated using RC circuits with variable elements. We were able to simulate spiking activity with a high noise floor using a spike circuit and injecting noise at the input of our first amplifier. We then observed whether induced spikes were induced after the final stage of the design.

Across these three stages, a noisy sample of neural spikes is processed and replicated. Important specifications for our design include low overall power consumption and, for the amplifier, high gain and low noise. This report describes the design of each circuit in detail and provides simulation results. We provide the circuitry necessary to not only decipher when spinal neurons are activated, but also to replicate these signals to following neurons.

SPIKE SIMULATION[3]

In order to simulate a spike, we used a bitstream with an RC network in order to smooth the signal. We first sent a series of pulses into a high pass filter, which would generate positive and negative spikes. Since we only wanted positive spikes, we rectified the output of the high pass filter. We then passed the rectified signal through a band-pass filter in order to give the spike the 0.5-1 ms width we desired, making it more into a triangular shape. Finally, we rectified the output once more since we were seeing discharging effects bring the voltage down to an unacceptable negative level. Thus, we were able to generate 100 μV spikes of approximately 0.5-1 ms in duration. An example

[2] Mithula Parangan, Chitra Aravind, Harilal Parasuraman, Krishnashree Achuthan, Bipin Nair,Shyam Diwakar, *Action Potential and Bursting Phenomena using Analog Electrical Neuron,* September 2010, pgs 1-7.

[3] Appendix II.

of the pulses are shown in Figure 2. Note that we ignored all measurements before 6.0 ms due to the startup state skewing the spike signals before that point.

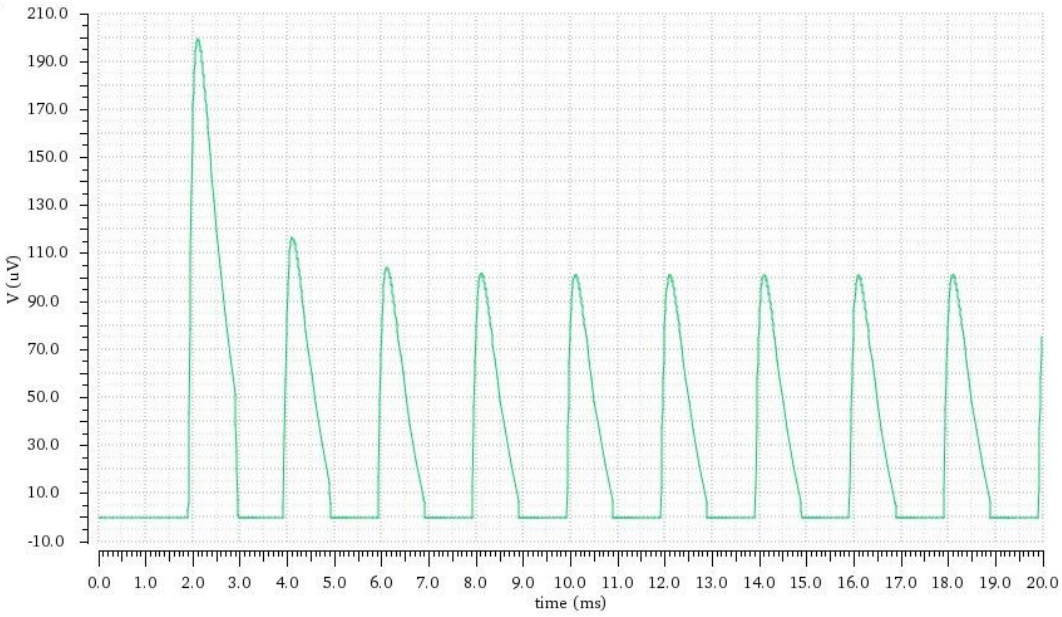


Figure 2. Input Neural Signals - 100 µV Spikes

AMPLIFIER[4]

For the first stage of our circuit, we use a fully differential amplifier. The role of this amplifier is to significantly amplify the inputted neural signals so that we can process them in later stages, while keeping low noise. We chose to use a single stage folded cascode design. This topography allows us to integrate a PMOS differential pair without sacrificing output range. The differential pair itself is biased by a PMOS current mirror. In the final design, we connected this amplifier in feedback, in an inverting configuration. The output of our spike simulator was connected to the Vin+ terminal, with the Vin- terminal set by a voltage divider from the amplifier's output.

During initial noise simulations, the amplifier had very high noise at low frequencies. This indicated that the noise figure was dominated by flicker noise from the transistors. Further analysis showed that the pmos differential pair and biasing mirror contributed to over 90% of the noise of the amplifier. To decrease flicker noise, we increased the size of the transistors, scaling up both width and length significantly. We also increased the bias current, which alleviated noise and increased overall gain. This resulted in a less noisy circuit. Lastly, two of the amplifiers were placed in series. The first amplifier sets the noise level. In the first amplifier, we added a capacitor to lower its pole. This lowered the break frequency and functioned to filter out noise at high frequencies.

[4] Appendix III.

Noise simulation results showed that the noise level was low enough as to not affect the operation or signal integrity of the circuit (Figure 3). The second amplifier provided the gain, amplifying the spikes to a workable level for the comparator. The output of each of these two stages is shown in Figures 4 and 5.

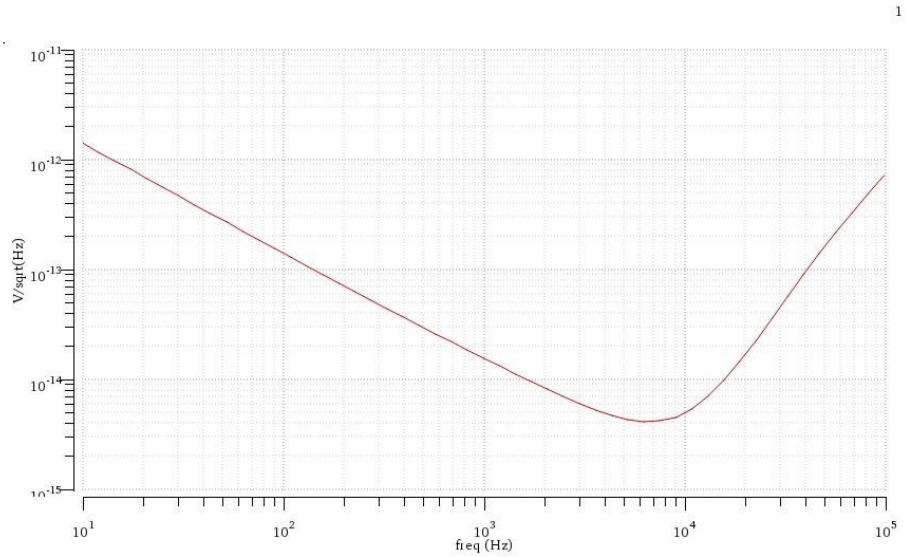


Figure 3. Noise Response of Folded Cascode

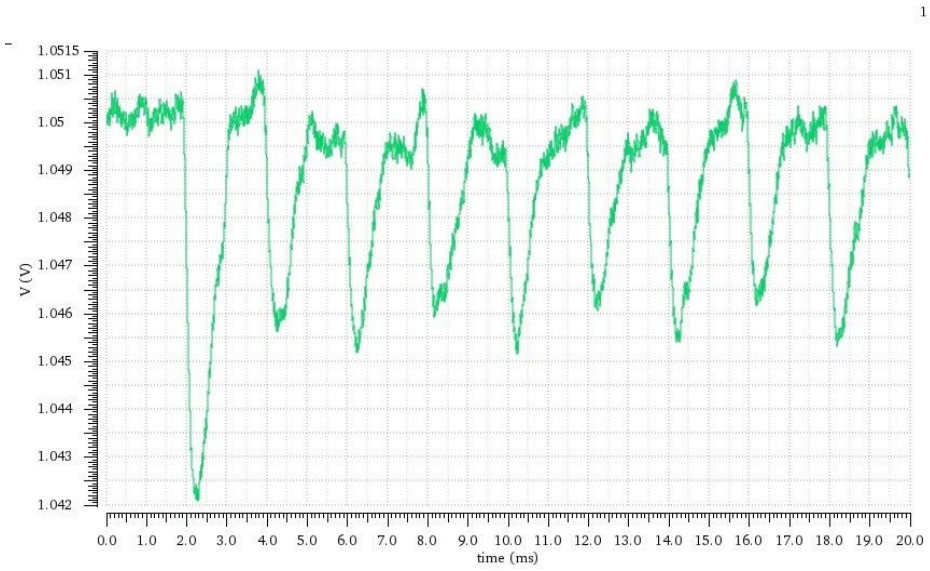


Figure 4. Output After First Folded Cascode

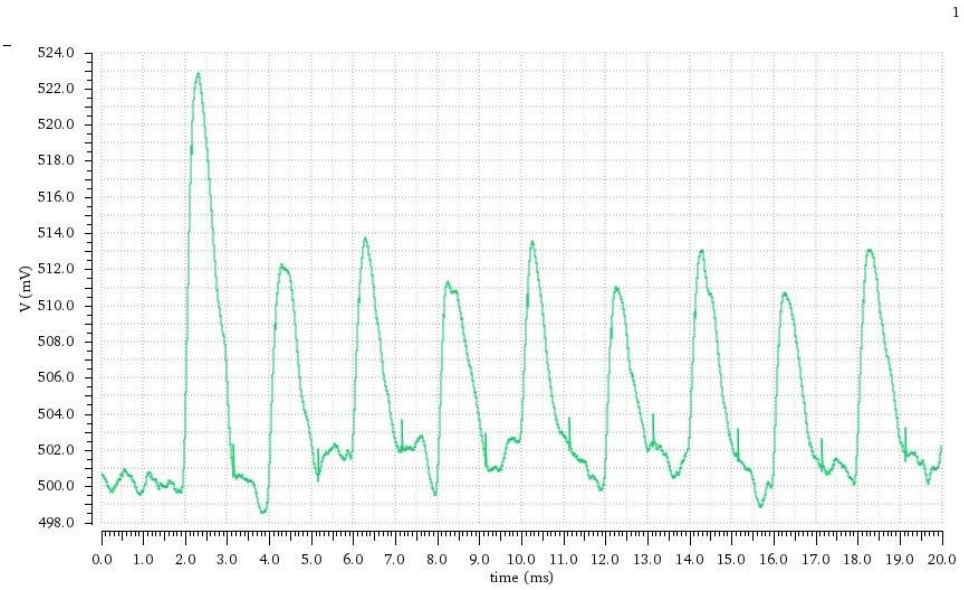


Figure 5. Total (2 Stage) Amplifier Output - 12mV spikes

COMPARATOR (SPIKE DETECTOR)[5]

The role of the comparator is its function as a spike detector. After the neural signal is passed through two amplifiers, the now amplified signal is sent into the comparator with a reference voltage of 506 millivolts. This the voltage threshold that was chosen so that any voltage above that threshold will be flagged as a spike. The comparator also takes in a clock signal, which is a V_{bit} source with a frequency of 1 ms. This makes the comparator synchronous with the stimulator circuit, which follows this stage, and makes the full processing of the signal faster and more accurate. The comparator works in a few steps; first, when the clock is low, this resets internal nodes to VDD-V_{GSp} and when it is high, it releases the internal nodes and biases the differential pair with I=Ibias. When the voltage at Vin+ is the same or higher than Vin-, this causes the comparator to output HIGH, in this case VDD, and outputs a LOW, or GND, when it is below the threshold voltage. This will then direct the stimulator on what signal to produce. The inputs and output can be seen in Figure 6.

The testing of this circuit in particular was difficult as it was first necessary to ensure that the voltage from the amplifier would be enough to turn on the transistors in order for the comparator to function properly. Once this issue was solved, we were able to change transistor sizing to reduce the power consumption of this circuit to nanowatts.

[5] Appendix IV.

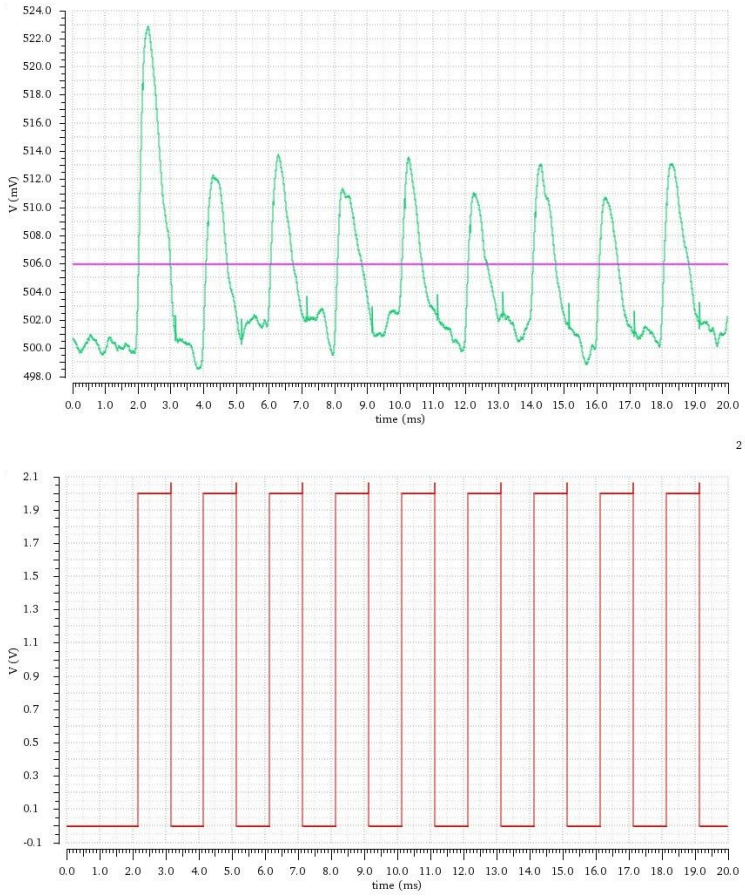


Figure 6. Output of Comparator, Overlaid with Input to Comparator
(Red is output, Green is output from amplifier, Pink is reference voltage)

STIMULATOR[6]

For the final stage of our design, we created a stimulator circuit, used to stimulate the downward movement of neurons whenever a spike is detected. The membrane is similar to a capacitor; the amount of charge can build up until it eventually burns out. Hence, it is important to have charge balance, meaning the summed area below each of the pulses of the output current should equate to 0. Figure 7 below illustrates this charge balance.

[6] Appendix V.

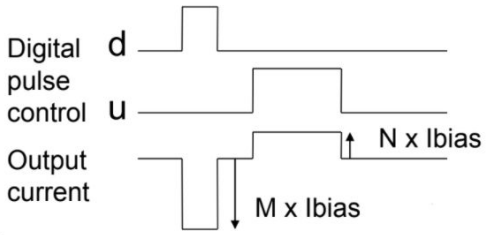


Figure 7. Charge Balance

The stimulator circuit consists of two inputs, pins, $\bar{U}$ and D, which are connected to gates of a PMOS and NMOS, respectively. Connected to the sources of the PMOS and NMOS transistors are DACs. The role of these DACs is to supply a variable output current for our stimulator circuit.

For the PMOS DAC, as seen on the schematic (Appendix V), the top level PMOS transistors are all carrying a current of 10uA. The row of transistors below these three transistors act as switches, allowing current to pass through them, depending on which transistors are switched on. In order to turn the PMOS transistors on, the gate is driven with a value of -1 V, and for the NMOS, with a value of 1 V. For purposes of this project, we hard-coded the values of the gates of these transistors by attaching DC voltage sources to the gates. To ensure that the same amount of current was flowing through each PMOS and NMOS DAC, we symmetrically drove the first gate of each DAC. The $\bar{U}$ and D signals were instantiated by flip flops, which stored the value of the comparator. As mentioned earlier, the comparator, either outputs a high value (Vdd, which is 2 V) or low (gnd). By this mechanism, the stimulator circuit could control which DAC's current could flow through.

In order to truly implement charge balance, instead of hardcoding the values of the DAC, it would be necessary to build a finite state machine. In our project we made the amplitude of the U and D signals the same, as shown in the transient plot below (Figure 8). A finite state machine would be able to broaden the range of amplitudes the output current could take, so that if signal was on for a longer amount of time, the amplitude of the next output current pulse would be higher to compensate for this, making sure the areas are equal to 0.

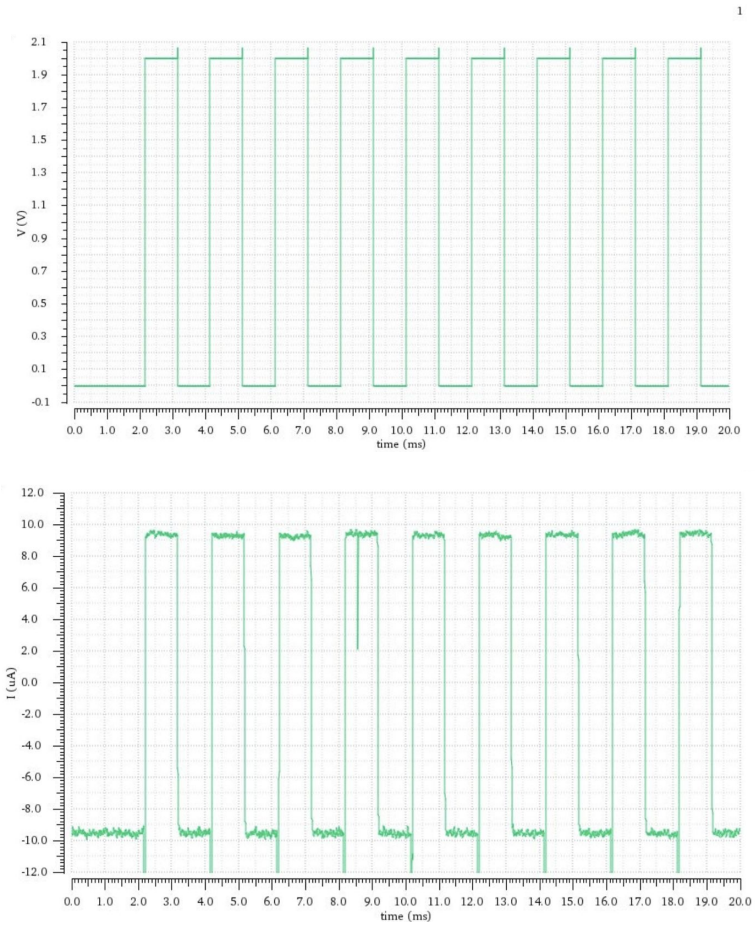


Figure 8. Input and Output of Stimulator Signal

FULL INTEGRATION[7]

In order to integrate everything, we first ensured that each individual component was working properly. Once we had everything working individually, we wired it all together and tested it. Because the amplifiers were now loaded, they didn't behave like they did individually. After some preliminary testing, we realized that the bias voltages on both non-inverting terminals were hitting the rails. To counteract this, we set up resistor bias networks, essentially using resistive voltage dividers between Vdd, ground, and the nodes to ensure the voltage was mid-rail. After this, our total gain from the spike generator to the output of the second amplifier still wasn't what we expected - we were still hitting Vdd on the second amp's output. To fix this, we adjusted the resistor value ratios to ensure we weren't getting too much gain. In addition, we made the resistor values on the order of hundreds of kilo-ohms so that we didn't draw too much current, effectively keeping our power consumption low.

[7] Appendix VI.

After the amplifiers were working, we had to adjust the reference voltage going into the comparator to ensure it accounted for the noise in the previous stages. Then, after getting some incorrect signals, we realized that our periodic spike generator was perfectly in sync with the clock, not taking into account the delay between the signal leaving the generator and reaching the comparator. Thus, adding in a small delay to the clock fixed the problem and we were able to move on to integrating the stimulating circuit. In order to maintain the charge balance of the output, we had to adjust the bias levels for both the control transistors and the transistors in the DACs to match the incoming signal. However, we were able to get it right and our circuit functioned as expected. The final top-level schematic is shown below in Figure 9.

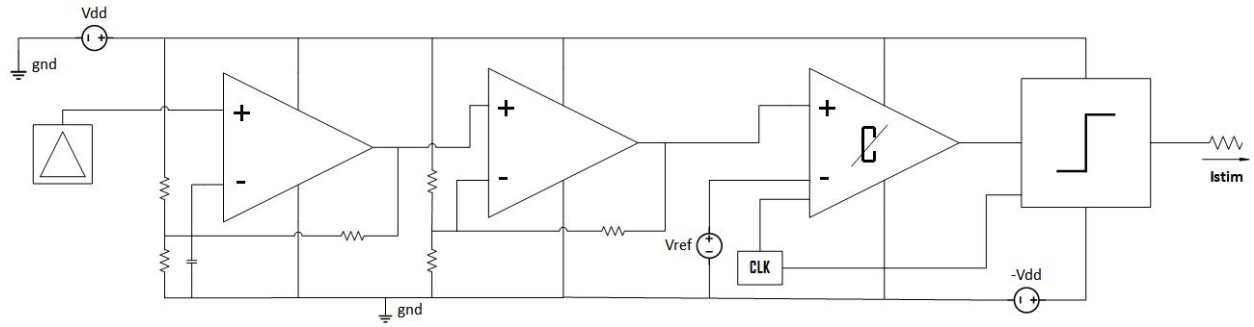


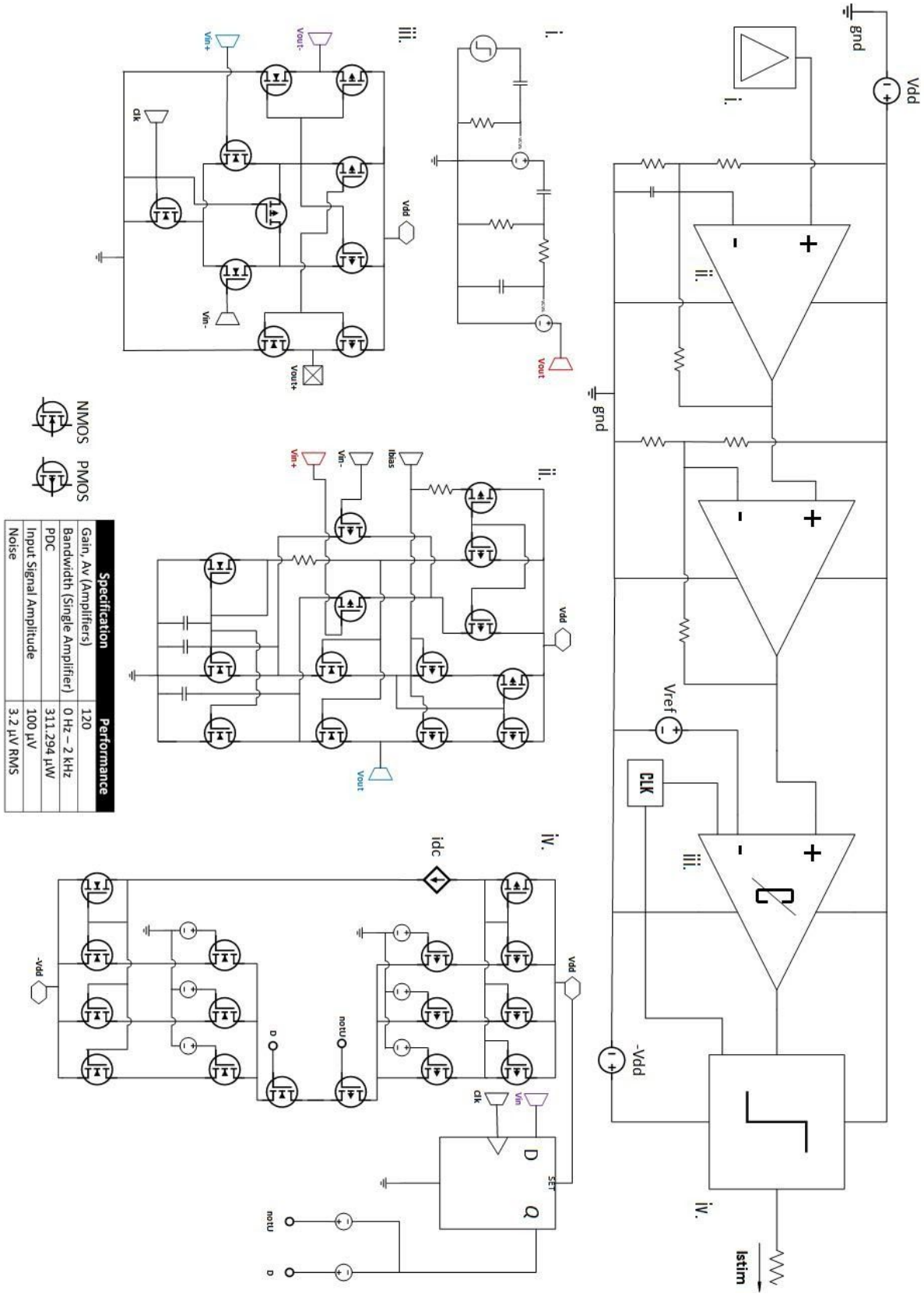
Figure 9. Top-Level Schematic (Without Bias Resistor Networks on Amplifiers)

Finally, it is worth mentioning that our power consumption with the fully integrated circuit was 311.294 µW. While this is slightly higher than what we would have liked, it ensured that our signal-to-noise ratio was excellent, making the rest of the integrated circuit work exactly as expected. The main consumer was the stimulator circuit. With a more advanced state machine, we believe the power consumption could be reduced significantly. The two amplifiers also consume a lot of power due to the high bias currents required to reduce noise.

CONCLUSION

As discussed earlier, the purpose of the neural repeater is to simulate neural signals in place of spinal cord injury. With today's technology, it is possible to replicate small and random signals from the body, even when they are no more than a few hundred microvolts. Additionally, the low consumption of power ensures that it will last a long time in the body, without need for replacement. In the same way that technology such as pacemakers have improved the cardiac health of many, this circuit has the potential to be used in countless cases of full or partial paralysis and other diseases affecting neural circuits and can drastically change the lives of anyone facing these issues.

SCHEMATIC AND SPEC SHEET



NMOS

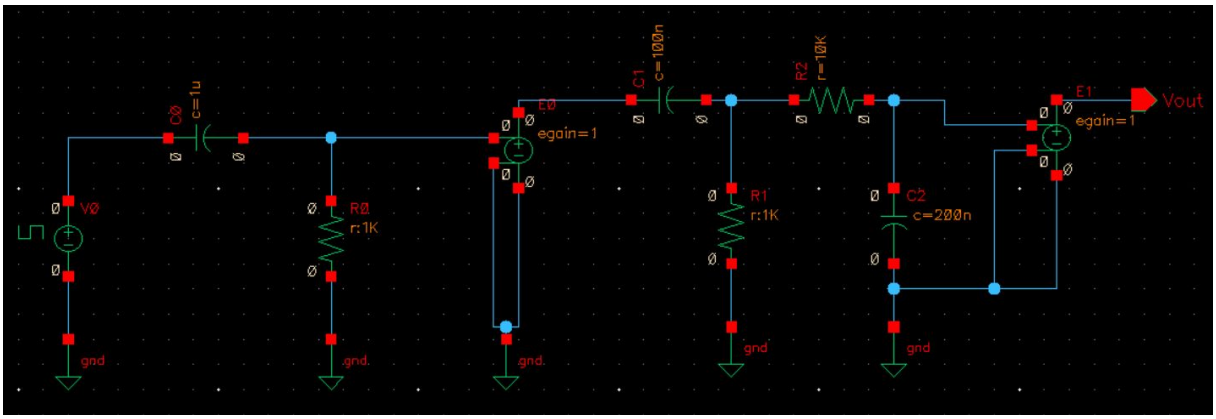
PMOS

Specification	Performance
Gain, Av (Amplifiers)	120
Bandwidth (Single Amplifier)	0 Hz – 2 kHz
PDC	311.294 µW
Input Signal Amplitude	100 µV
Noise	3.2 µV RMS

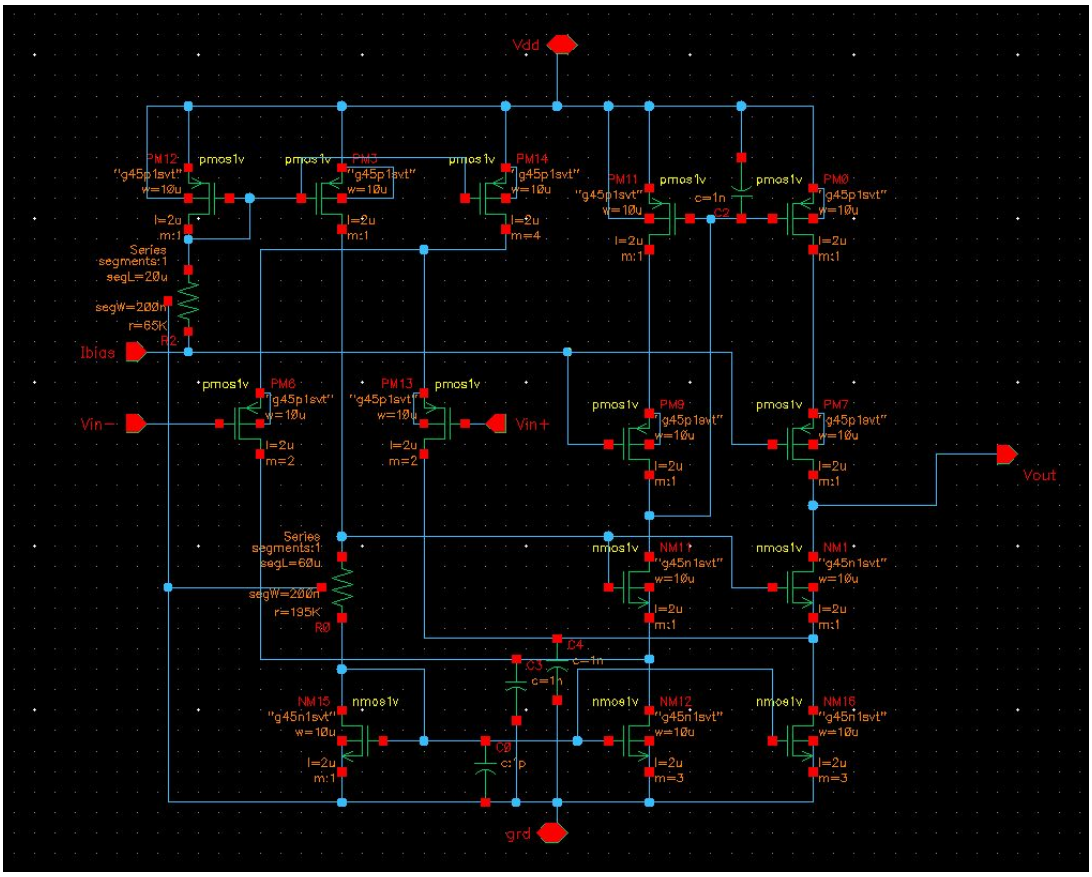
APPENDIX

Task	Person
Amplifier, Visio Schematics/Spec. Sheet	Kirsten
Comparator	Melissa
Spike Simulator	Aratrika
Full System Integration, Debugging, and Testing	Dan
Proposal, Design Review, Final Presentation, Final Report	All

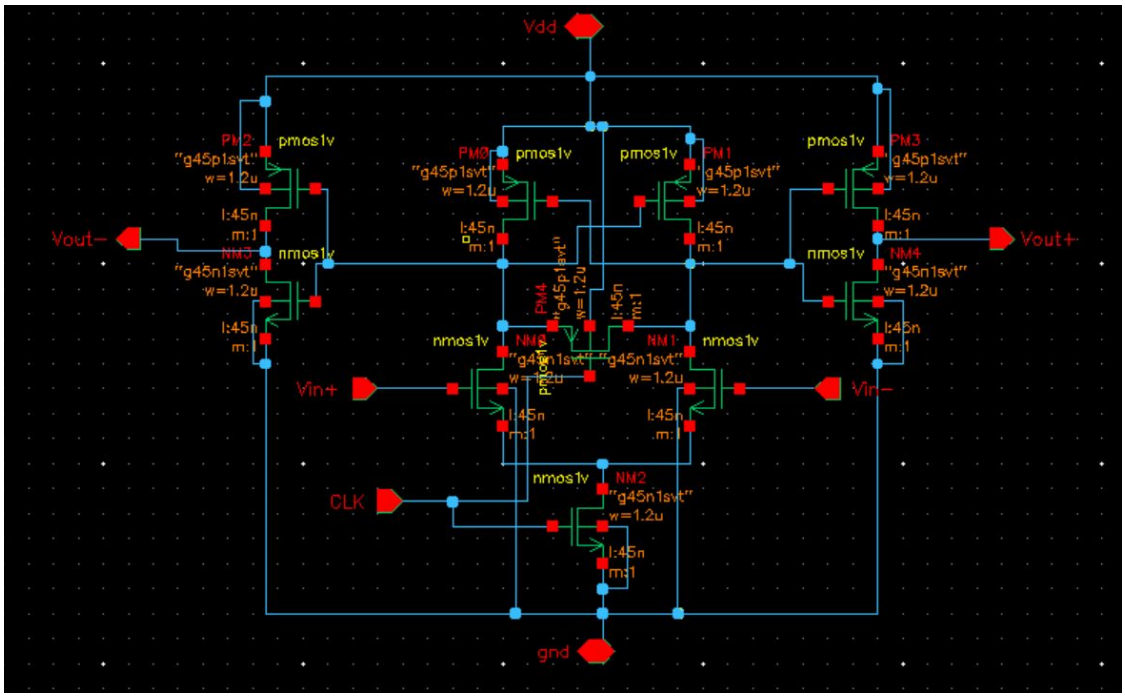
Appendix I. Division of Labor



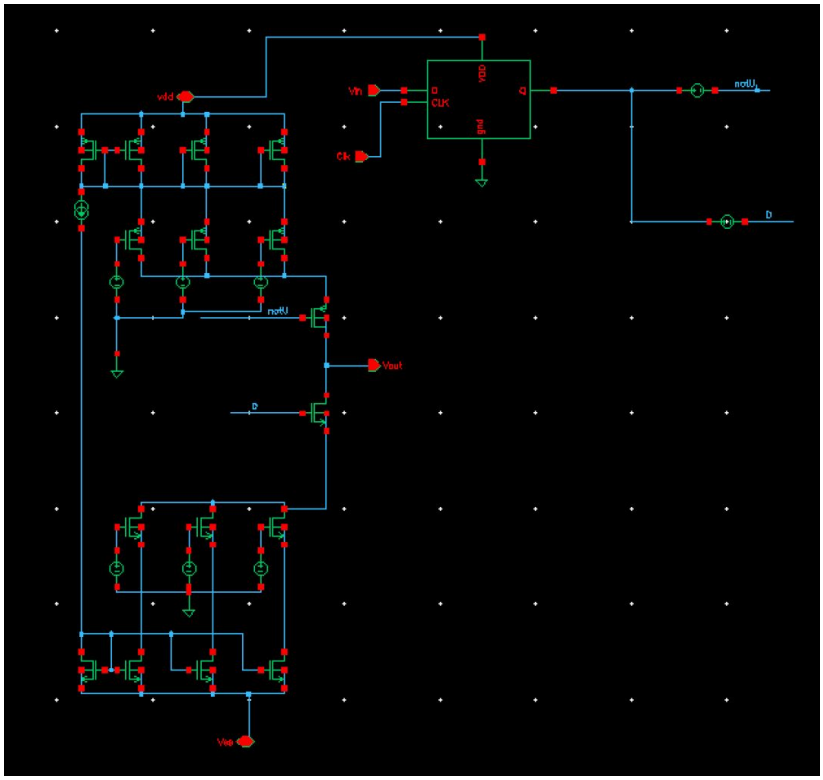
Appendix II. Spike Generator Schematic



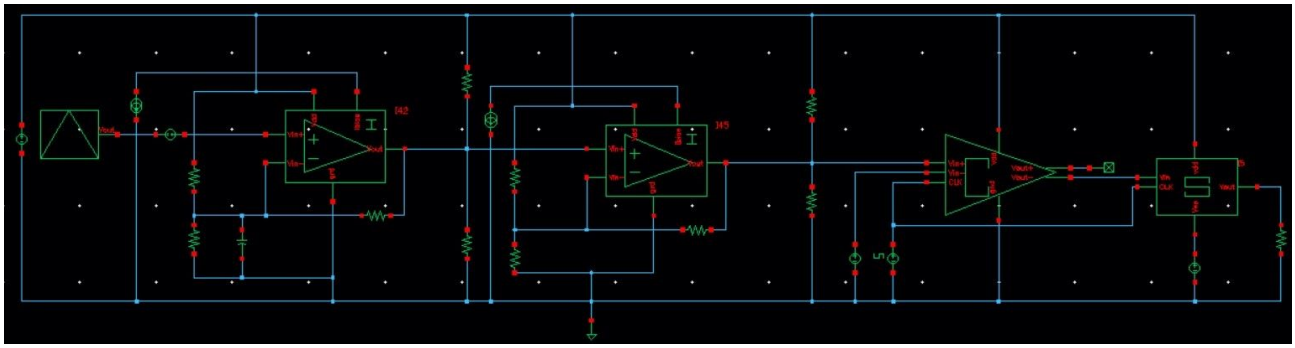
Appendix III. Folded Cascode Schematic



Appendix IV: Comparator Schematic



Appendix V: Stimulator Circuit Schematic



Appendix VI. Full Integration Schematic

REFERENCES

Mithula Parangan, Chitra Aravind, Harilal Parasuraman, Krishnashree Achuthan, Bipin Nair,Shyam Diwakar, *Action Potential and Bursting Phenomena using Analog Electrical Neuron,* September 2010, pgs 1-7

Virgínia Helena Varotto Baroncini, Oscar da Costa Gouveia-Filho, *Design of RF CMOS Low Noise Amplifiers Using a Current Based MOSFET Model,* September 2004, pgs 1-6

Alex Pappachen James, Aigerim Tankimanova, *Neural Network-Based Analog-to-Digital Converters,* December 2017, pgs 297-313

Hassan Jassim Motlakj, *Design of Low Voltage, Low Power (lF) Amplifier Based-On MOSFET Darlington Configuration,* January 2013, pgs 1-7

Matthew C. Tresch, Philippe Saltiel, Emilio Bizzi, *The construction of movement by the spinal cord,* February 1999, pgs 1-6

Yang, B., Zhang, F., Cheng, F. *et al.* Strategies and prospects of effective neural circuits reconstruction after spinal cord injury. *Cell Death Dis* 11, 439. June 2020. Pgs 1-14.

Alyosha Molnar, *ECE5040: Introduction to Neural Engineering,* Fall 2011