E3: 231 Digital Design with FPGA's

DESE, Indian Institute of Science, Bangalore

DSF Mini Project 2023

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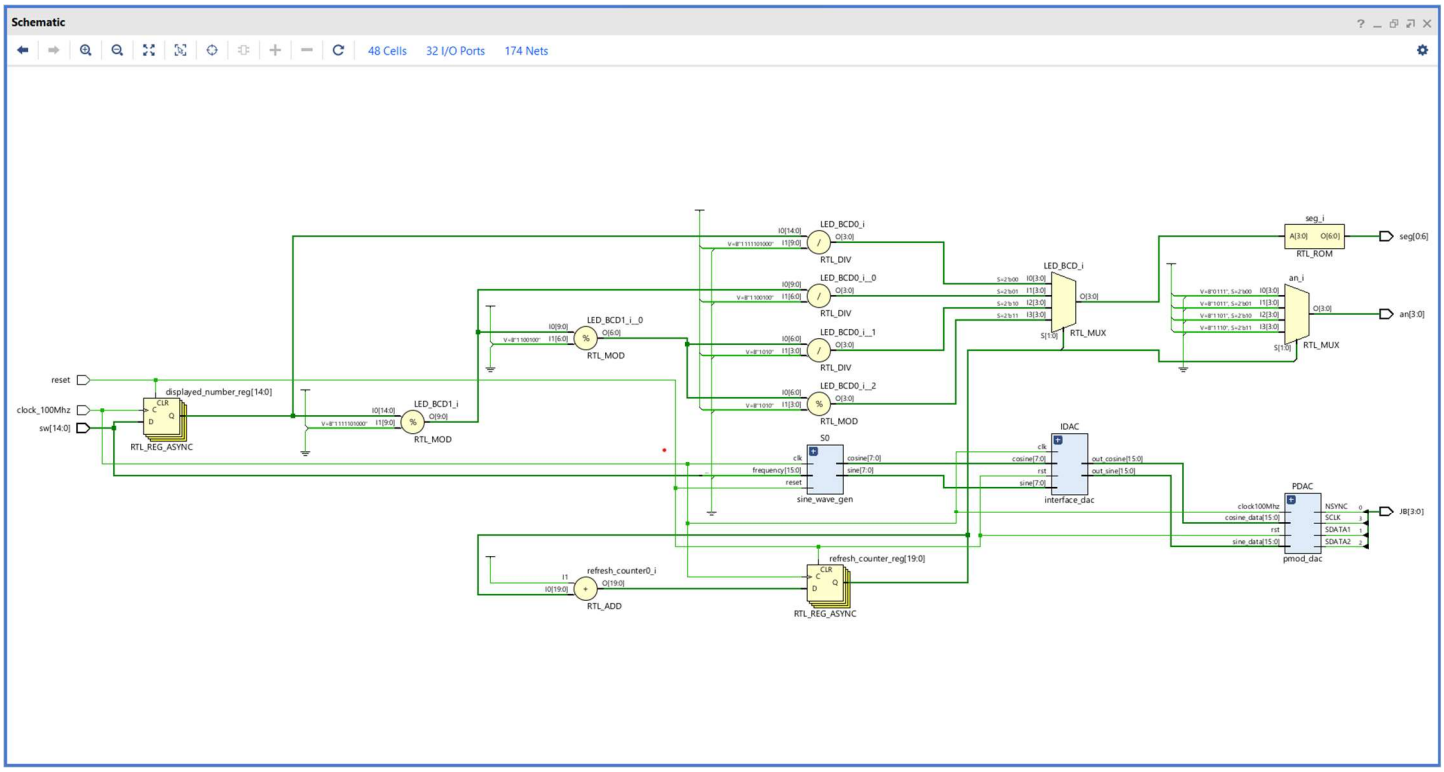
Electronic Product Design

Problem Statement:

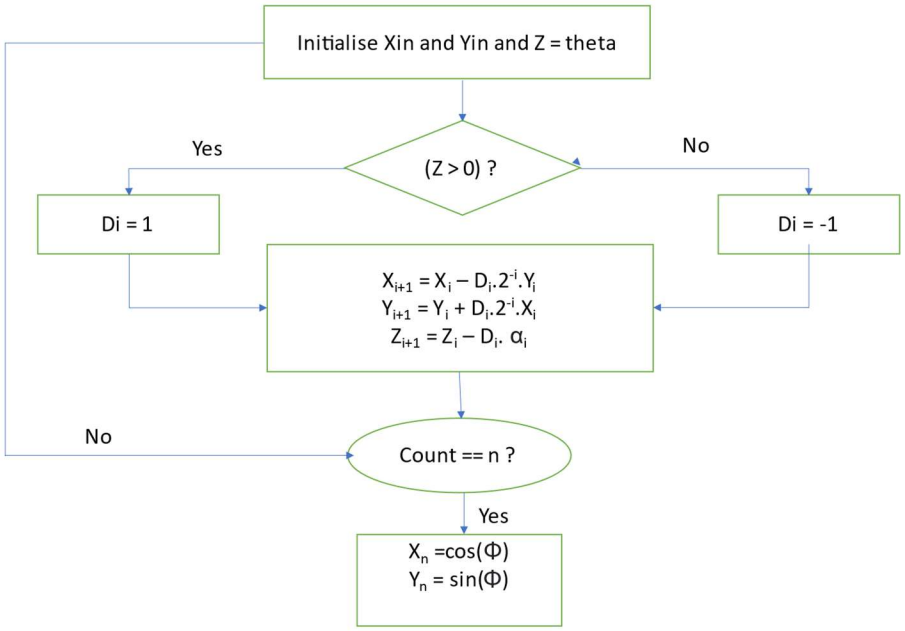
Objective of this Project is to design architecture for a given algorithm and to design in detail the Datapath and the control path of that architecture, using minimum resources and demonstrate it on BASYS3 Board Note: Target Device is Xilinx Artix-7 XC7A35T-ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1). Submit the Block diagram, State diagram, Verilog code and a brief report with utilization and timing parameters. Design a Sine waveform generator using CORDIC algorithm. You can choose the architecture you want and decide on constraints(E.g., Min Resources/ Max frequency of waveform etc).Implement the design on the BASYS3FPGA Board. Input the Desired frequency using Slide switches. You can use Pmod DAC2 to display the waveform on a Digital Oscilloscope.

Implementation

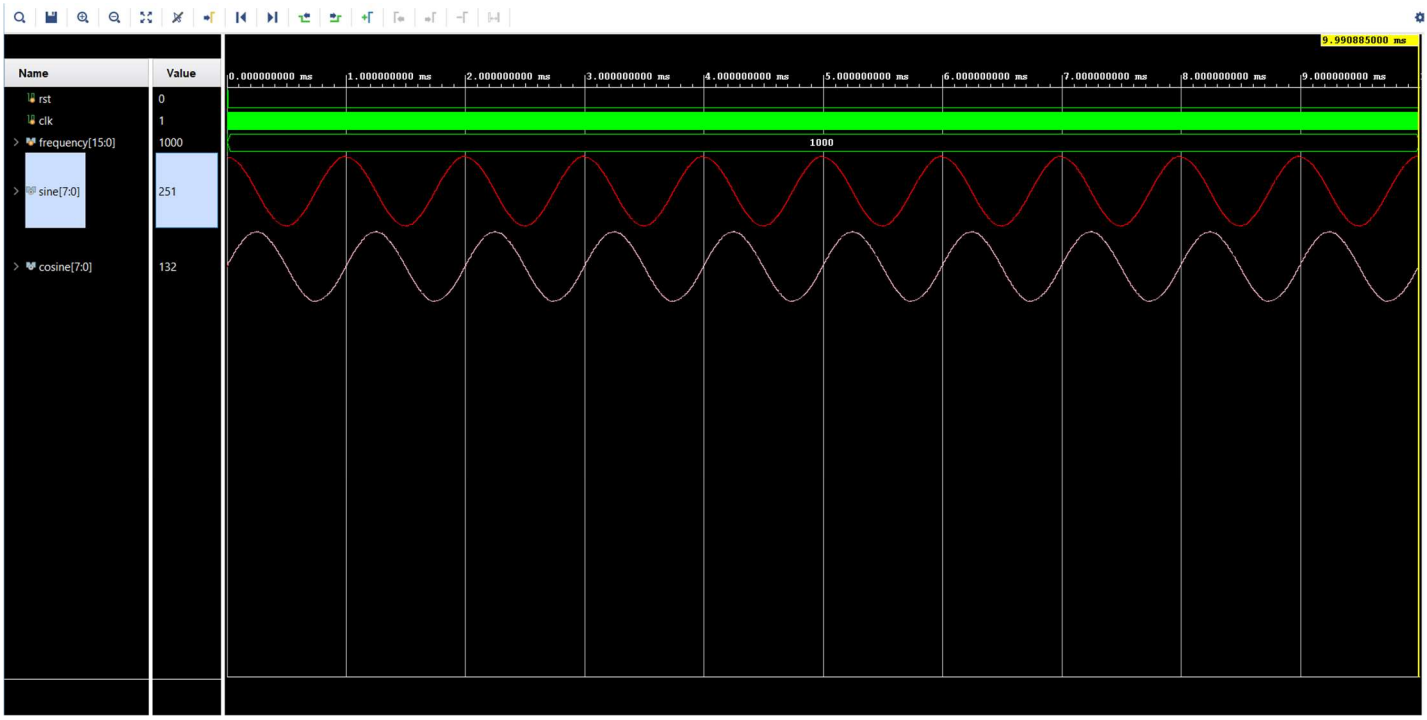
A) RTL Block Diagram:



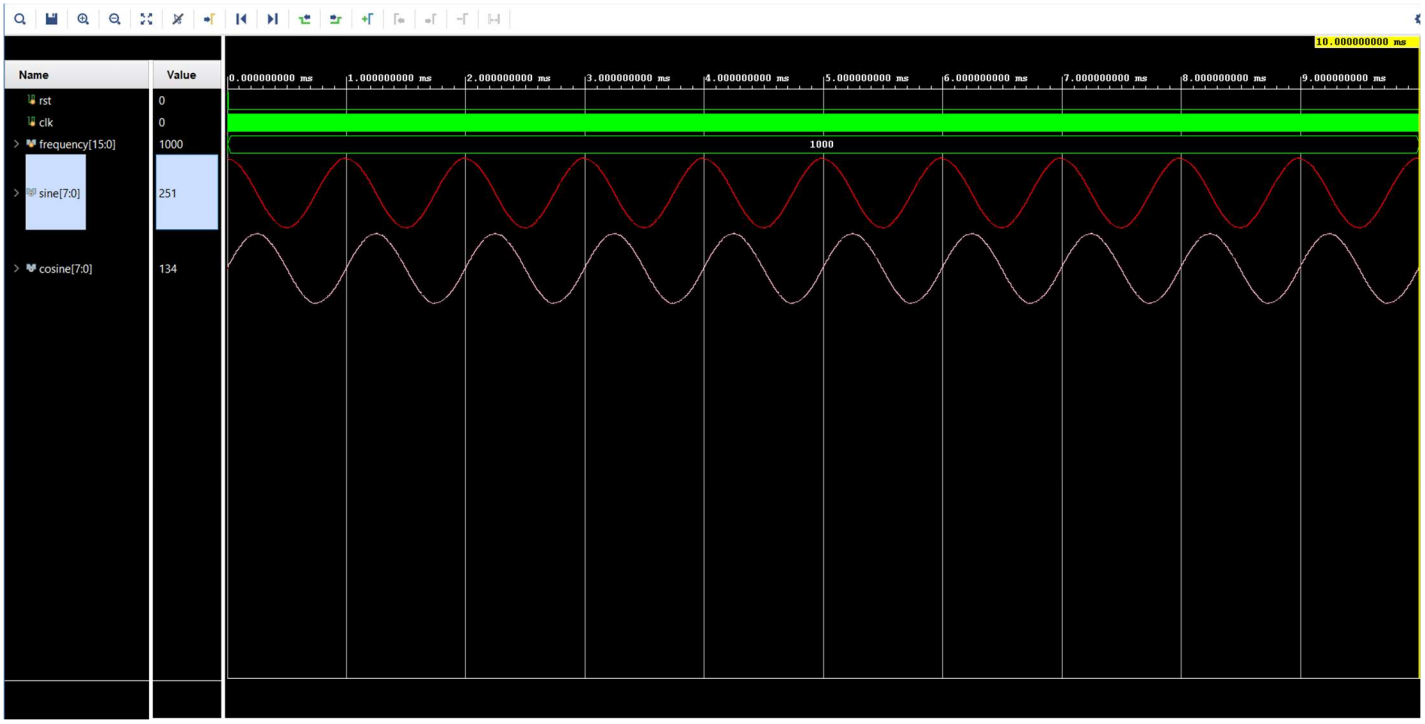
B) Block Diagram:



C) Behavioral Waveform:



D) Post Implementation Timing Waveform:



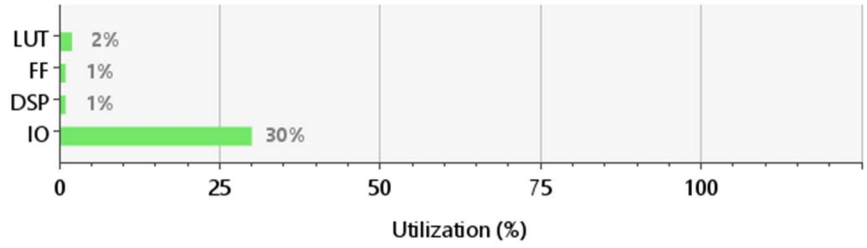
E) Report Utilization:

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	DSPs (90)	Bonded IOB (106)	BUFGCTRL (32)
board_interface	466	454	172	466	1	32	1
IDAC (interface_dac)	8	23	5	8	0	0	0
PDAC (pmod_dac)	15	27	8	15	0	0	0
S0 (sine_wave_gen)	317	369	113	317	1	0	0
S1 (sine)	12	32	13	12	1	0	0
S2 (sine_gen)	305	337	102	305	0	0	0

Summary

Resource	Utilization	Available	Utilization %
LUT	466	20800	2.24
FF	454	41600	1.09
DSP	1	90	1.11
IO	32	106	30.19



F) Design Timing Summary:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.377 ns	Worst Hold Slack (WHS):	0.155 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	513	Total Number of Endpoints:	513	Total Number of Endpoints:	456

All user specified timing constraints are met.

G) Power Report:

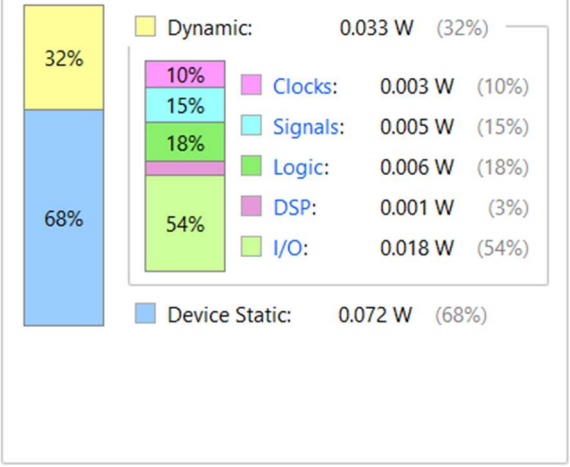
Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.105 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.5°C**
Thermal Margin:	59.5°C (11.8 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

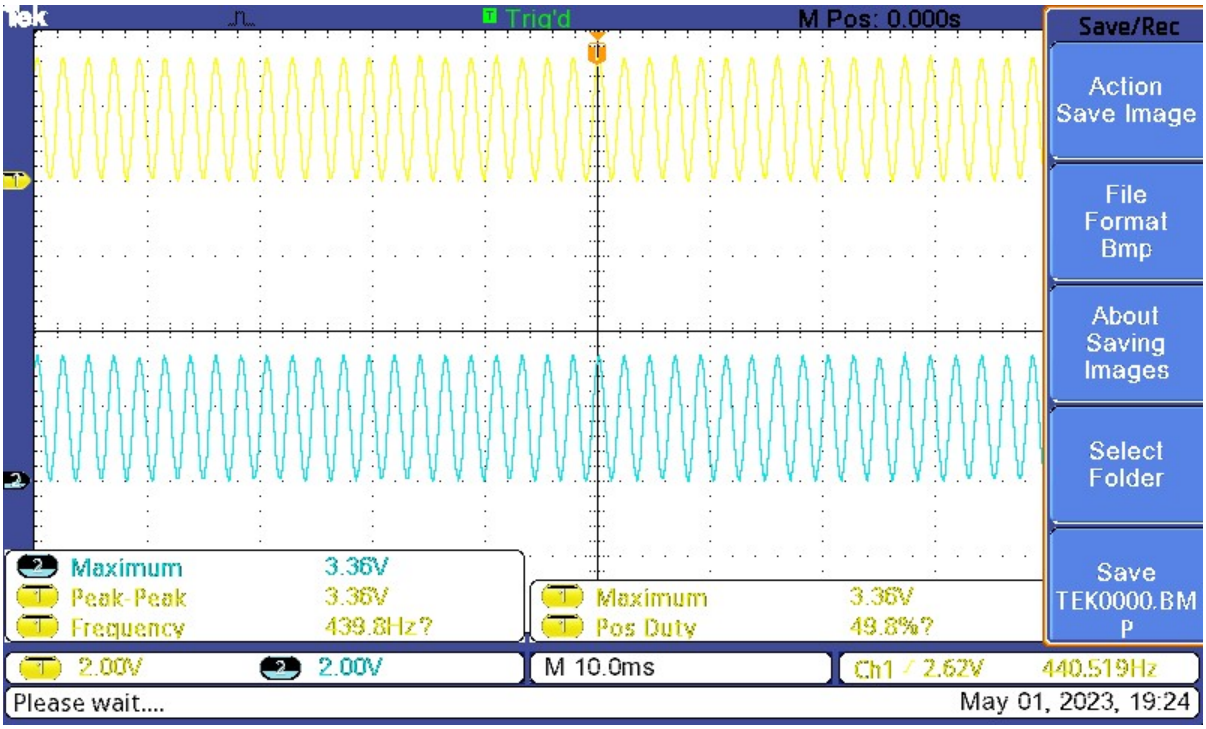
Launch Power Constraint Advisor to find and fix invalid switching activity

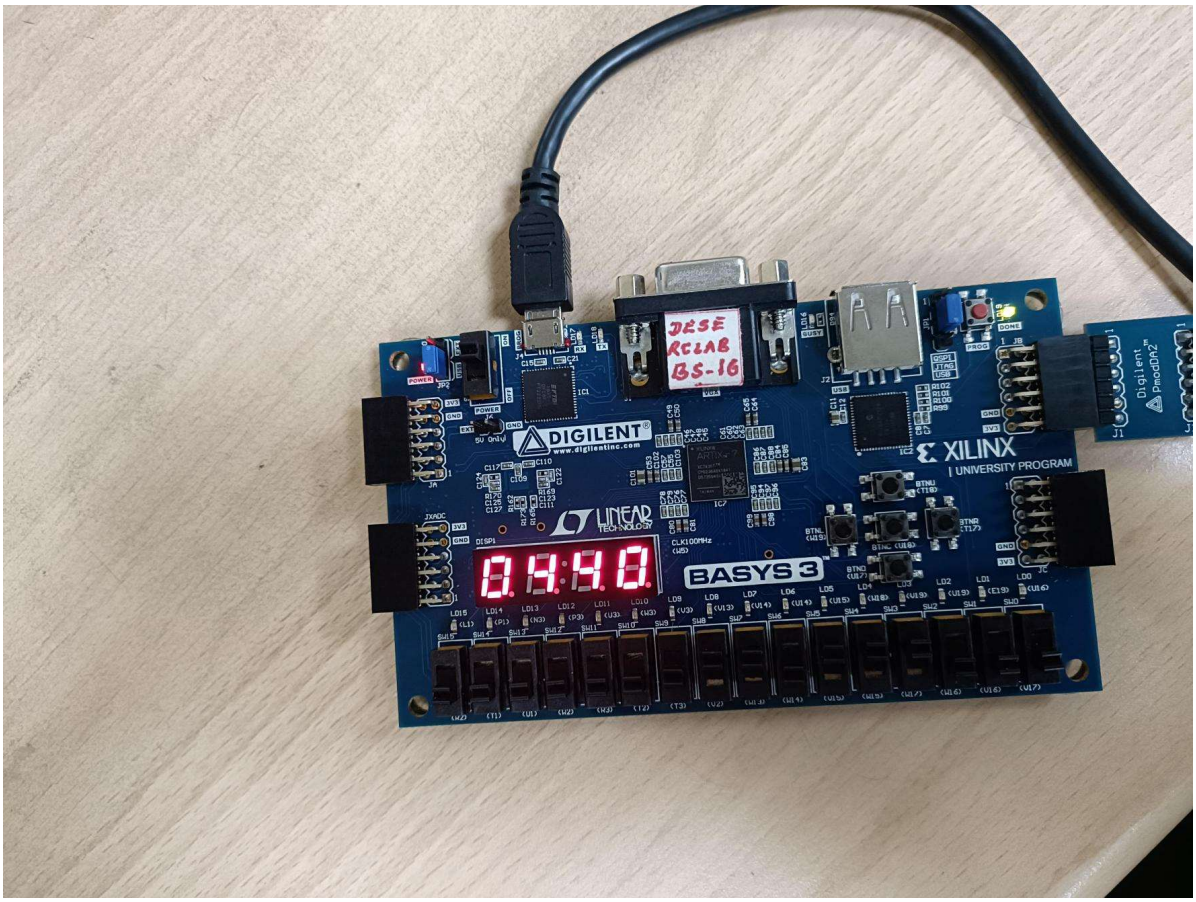
On-Chip Power



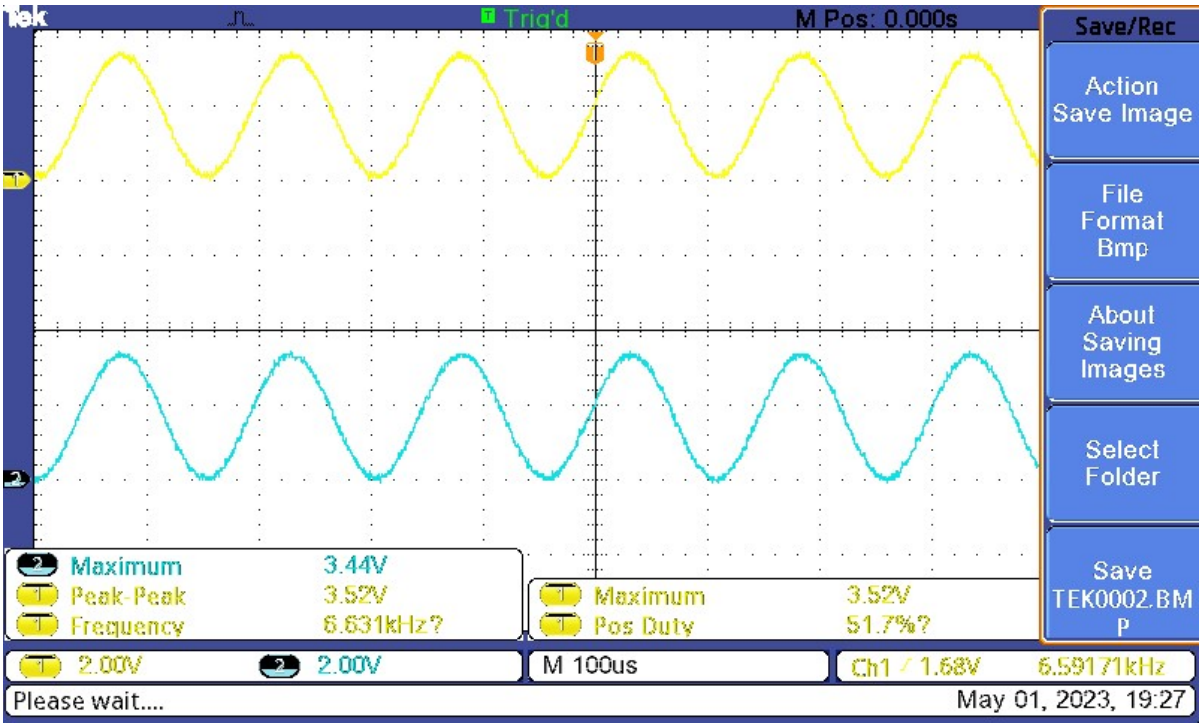
FPGA Implementation

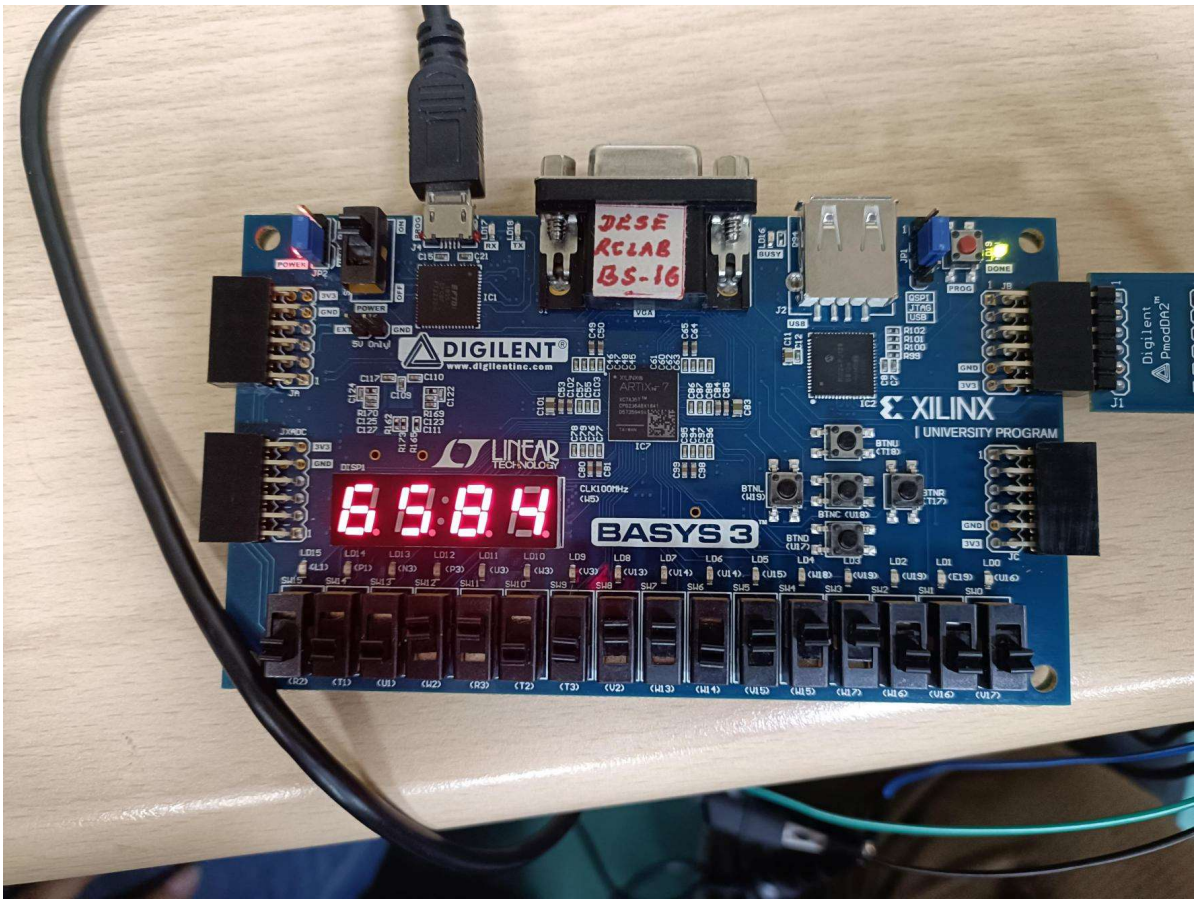
(A) 440 Hz Sine and Cosine wave



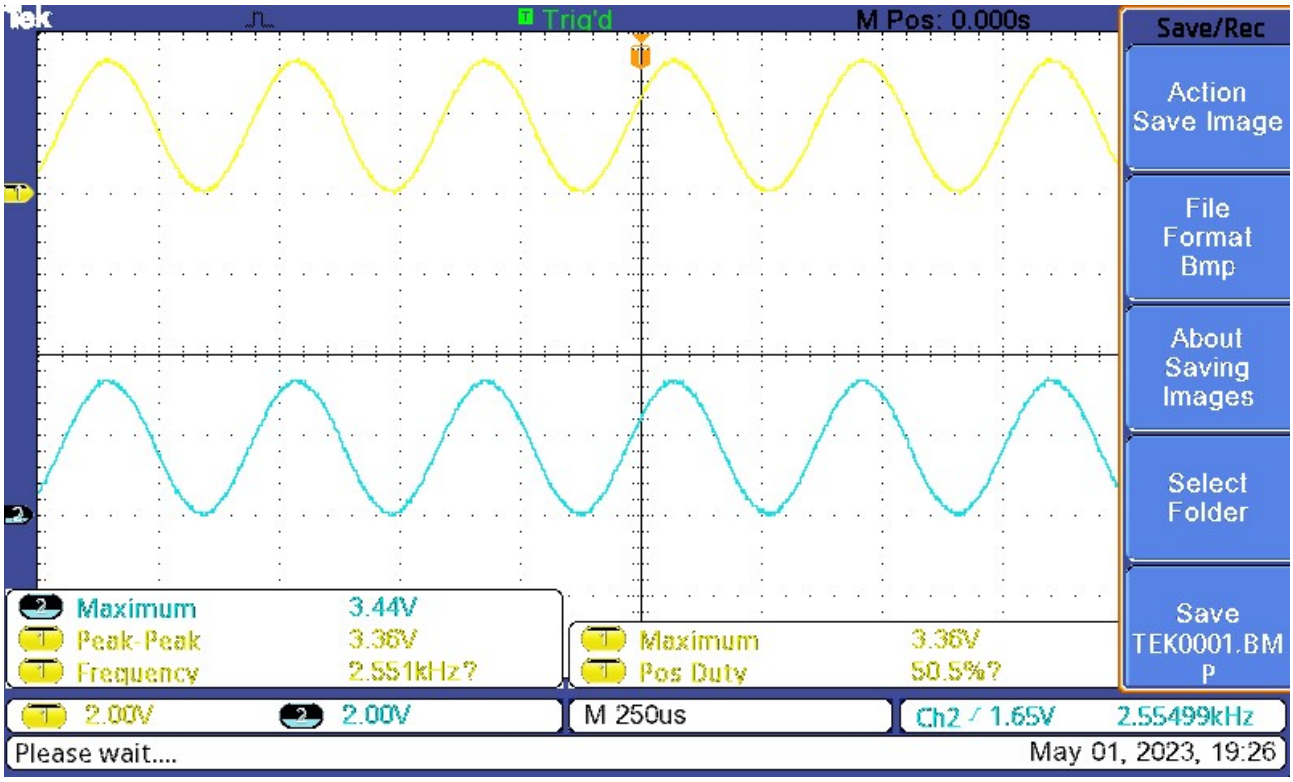


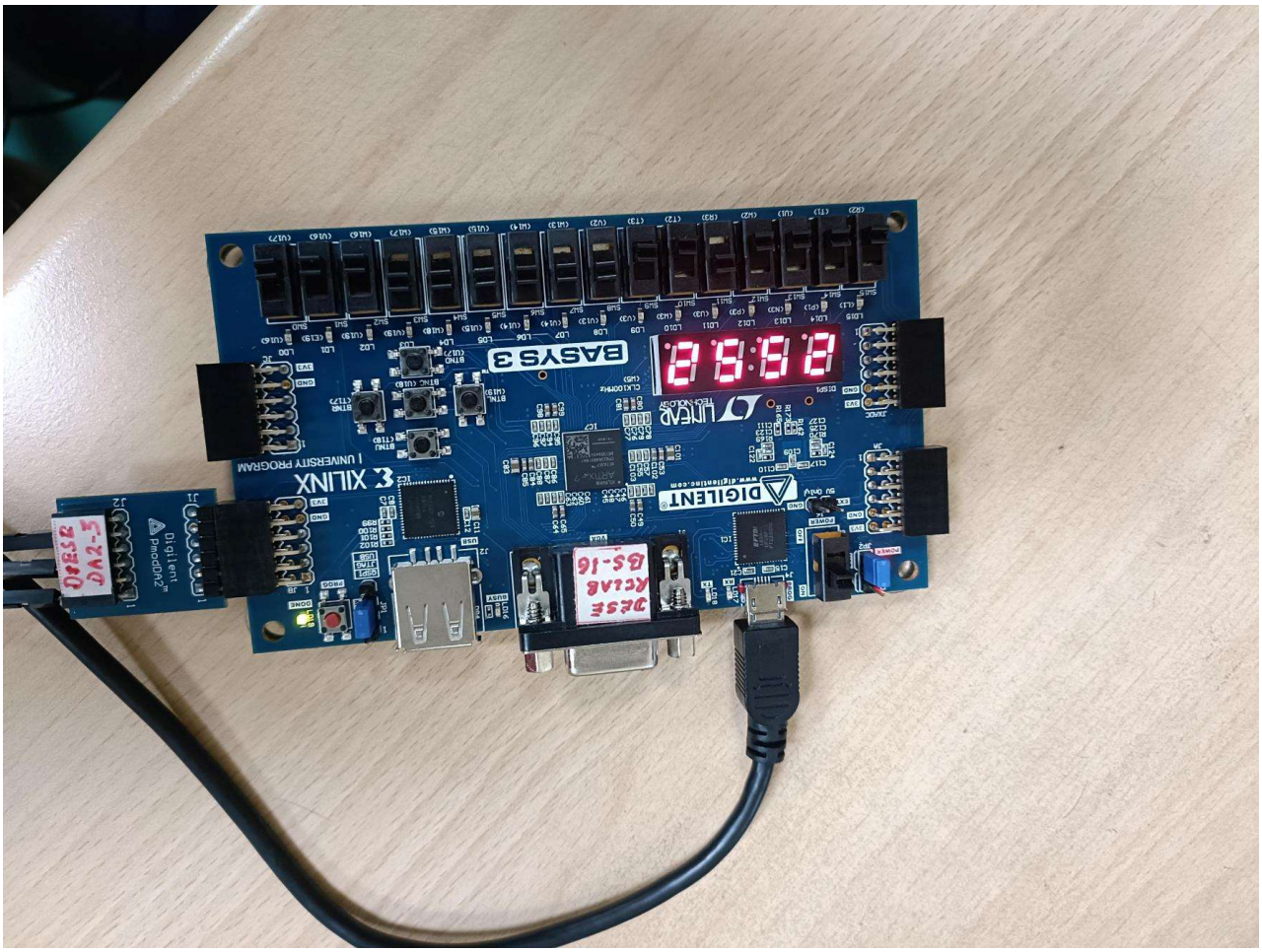
(B) 6.584 KHz Sine and Cosine wave

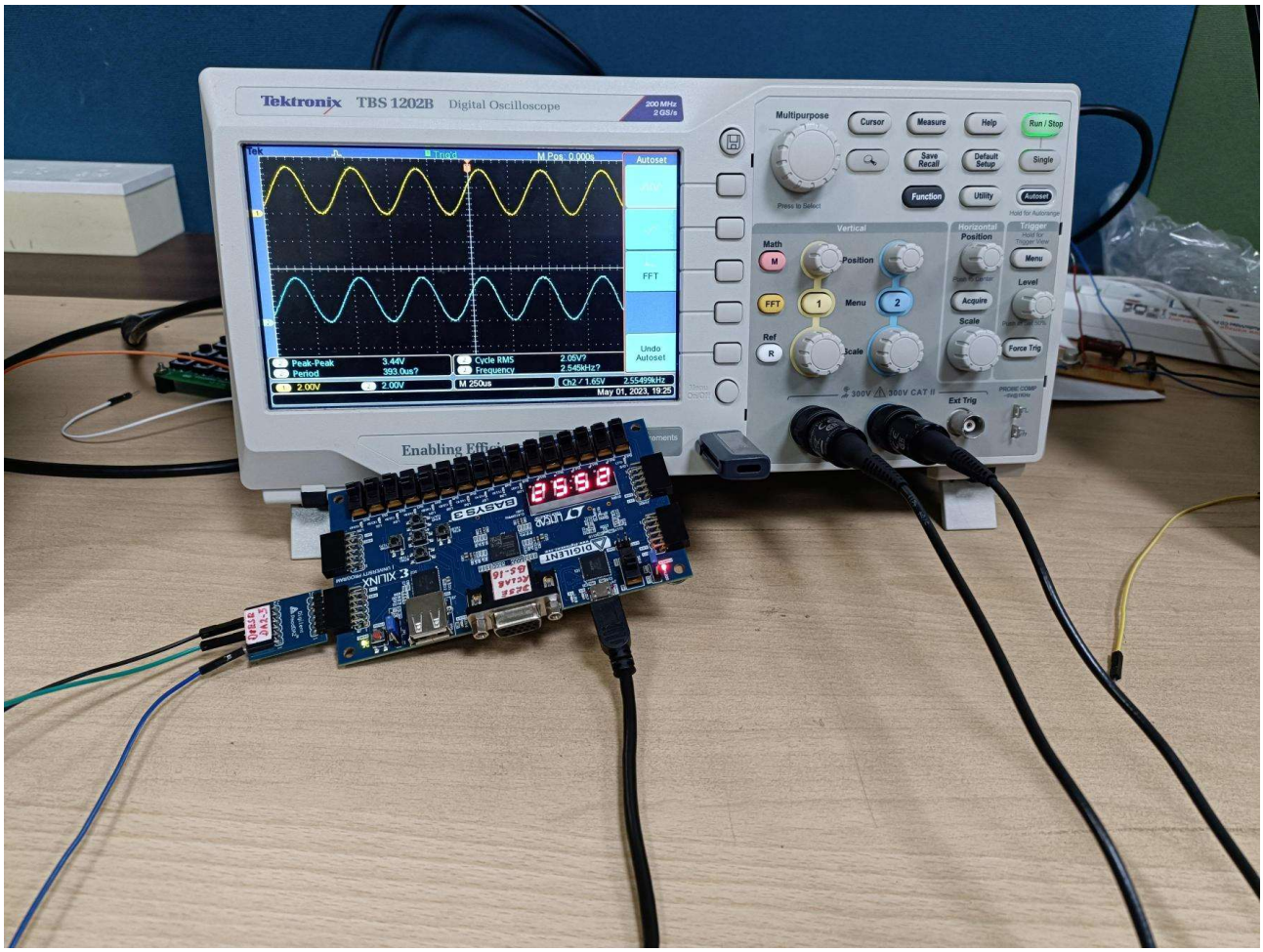




(C) 2.552 KHz Sine and Cosine wave







CONCLUSION:

In conclusion, the pipelined waveform generator successfully generated sine and cosine waves. The frequency of the waves can be adjusted using 16 input switches, allowing for a maximum input of 62 kHz. The CORDIC algorithm implemented in the generator can produce output at up to 100 MHz, enabling it to generate frequencies of up to 50 MHz, which is the Nyquist frequency. However, the bottleneck for generating an analog signal at the output port is the SPI-connected DAC, which has a maximum sample rate of 1 Mbps and a slew rate of 1 V/µs. This poses a limitation on the maximum frequency that can be generated, which is much lower than the output of the CORDIC block.