Laboratory Exercise 0

Getting Started

This is an introductory exercise that is intended to prepare you for Lab Exercises 1 and 2.

1. Perform the provided tutorial called "Using the ModelSim-Intel FPGA Simulator with Verilog Testbenches". This tutorial is included as part of the *Design Files* for this exercise. You will need to know how to use the ModelSim simulator for Laboratory Exercises 1 and 2.

2. This part is optional. It is relevant only if you have *your own* DE1-SoC (or DE10-Lite) board, and want to use your board at home for this course. If you do not have your own board (probably most of you do not), then skip to item 3, below.

   To re-familiarize yourself with the Quartus Prime software tools, which you have used previously in ECE241, read through the provided tutorial called "Quartus Prime Introduction Using Verilog Designs". This tutorial is included as part of the *Design Files* for this exercise. You can use the Quartus Prime software in Laboratory Exercises 1 and 2.

3. As a "replacement" for the DE1-SoC (or DE10-Lite) board, we are providing a GUI-based tool that connects to the ModelSim simulator. This tool, which is called *DESim*, is similar to the *fake_fpga* tool that you were given for ece241. You can continue to use the *fake_fpga* tool if you wish, or you can use DESim. An advantage of DESim is that it is easier to install in comparison to *fake_fpga*, and it comes with some simple-to-understand example (*demos*) Verilog projects.

   We have not finalized the method that we will use to provide DESim for your use, so please look for an announcement about this on Quercus during the first week of class.