Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of the participant : S Sai Venkata Kishan Kumar

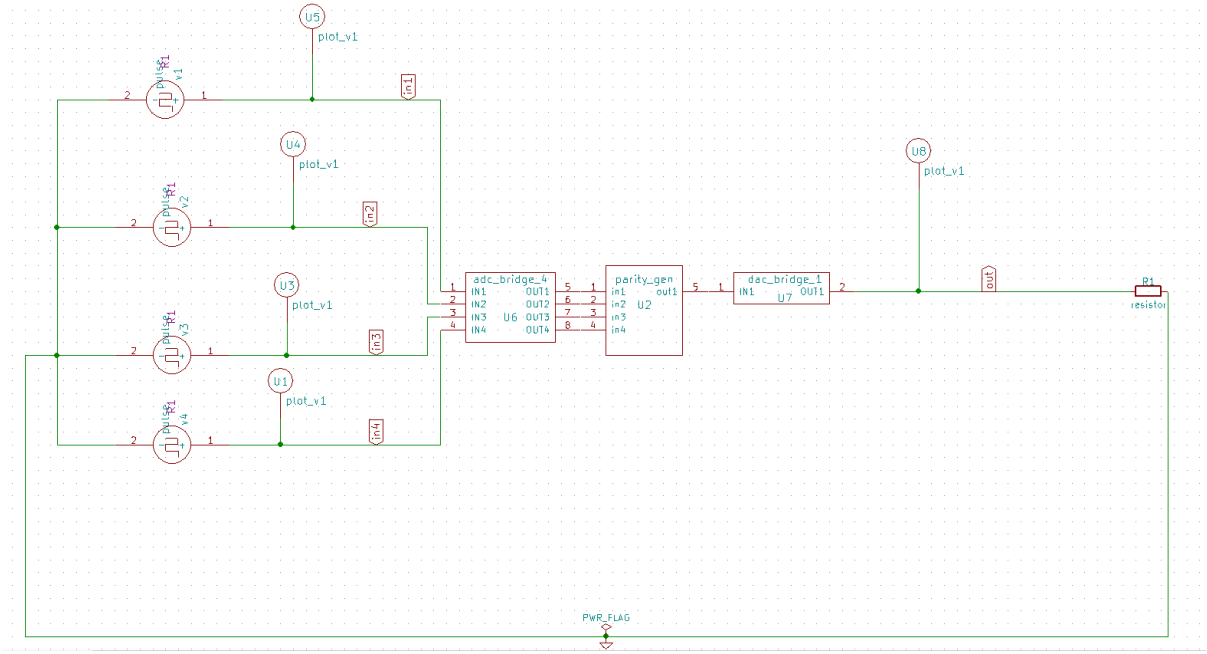
Title of the circuit : Parity Generator

Theory/Description : It is combinational circuit that accepts an n-1 bit stream data and generates the additional bit that is to be transmitted with the bit stream. This additional or extra bit is termed as a parity bit. In even parity bit scheme, the parity bit is '0' if there are even number of 1s in the data stream and the parity bit is '1' if there are odd number of 1s in the data stream. In odd parity bit scheme, the parity bit is '1' if there are even number of 1s in the data stream and the parity bit is '0' if there are odd number of 1s in the data stream.

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity parity_gen is
    port ( B0 : IN STD_LOGIC;
           B1 : IN STD_LOGIC;
           B2: IN STD_LOGIC;
           B3 : IN STD_LOGIC;
           p : OUT STD_LOGIC);
end parity_gen;
architecture parity_gen_arch of parity_gen is
    begin
        p <= B0 xor (B1 xor (B2 xor B3));
end parity_gen_arch;
```

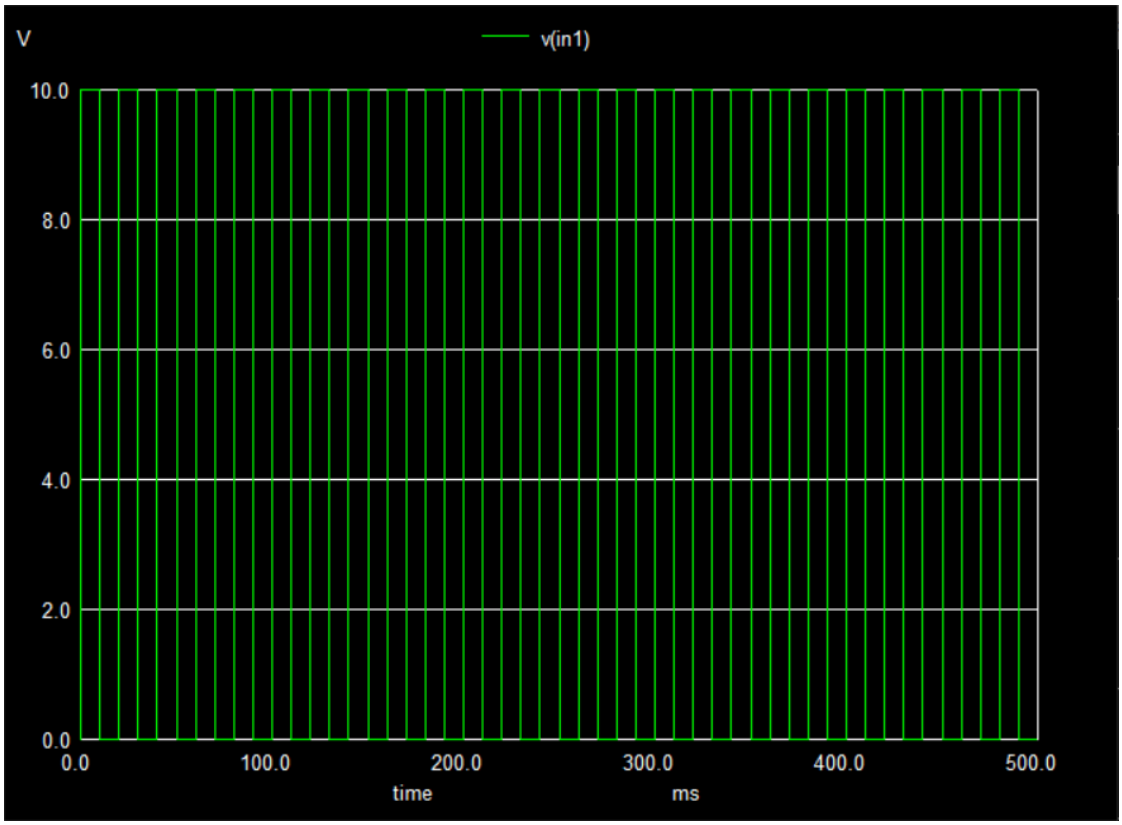
Circuit Diagram(s) :



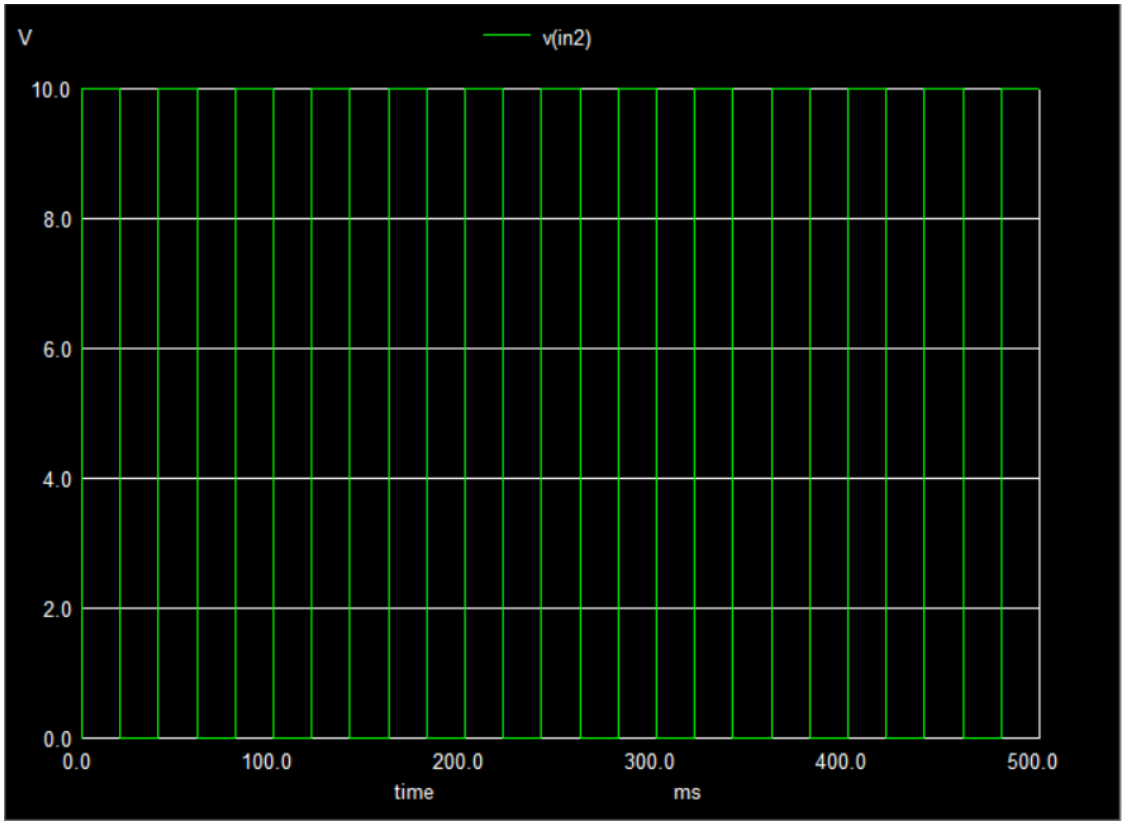
Results (Input, Output waveforms and/or Multimeter readings) :

NGSPICE PLOTS:-

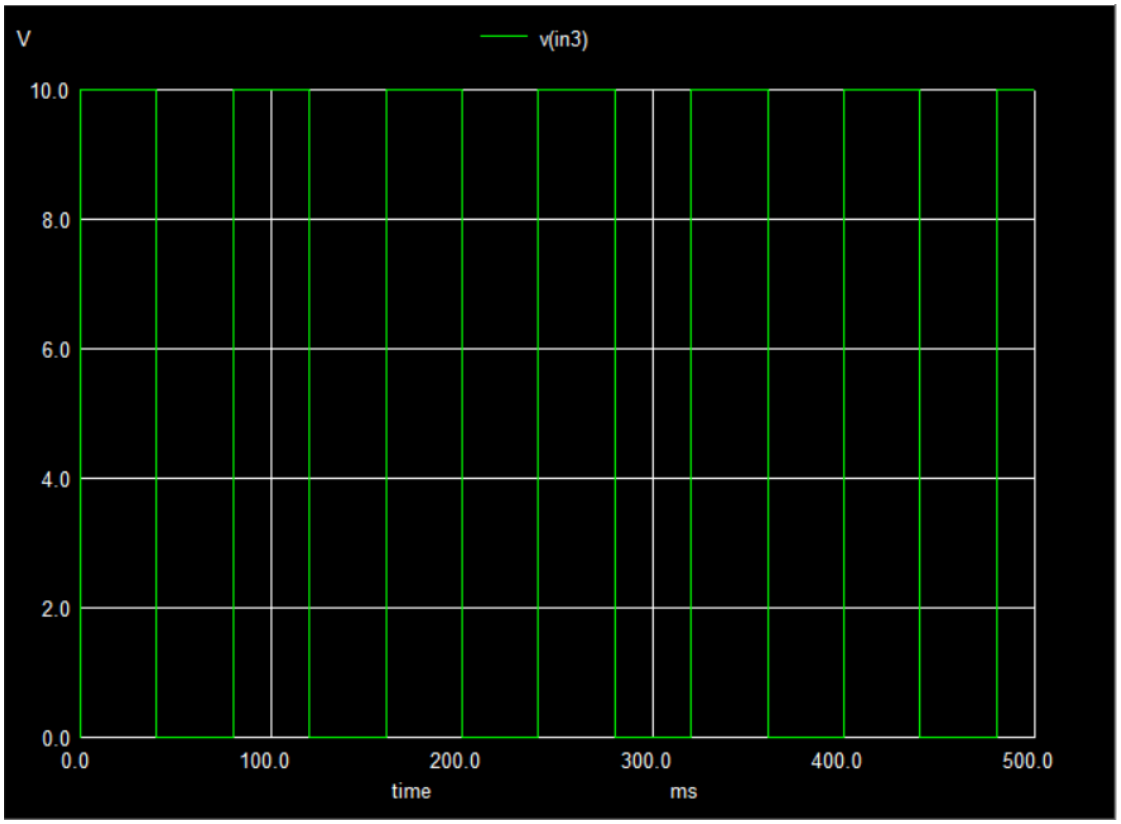
1) Plot(in(0)):-



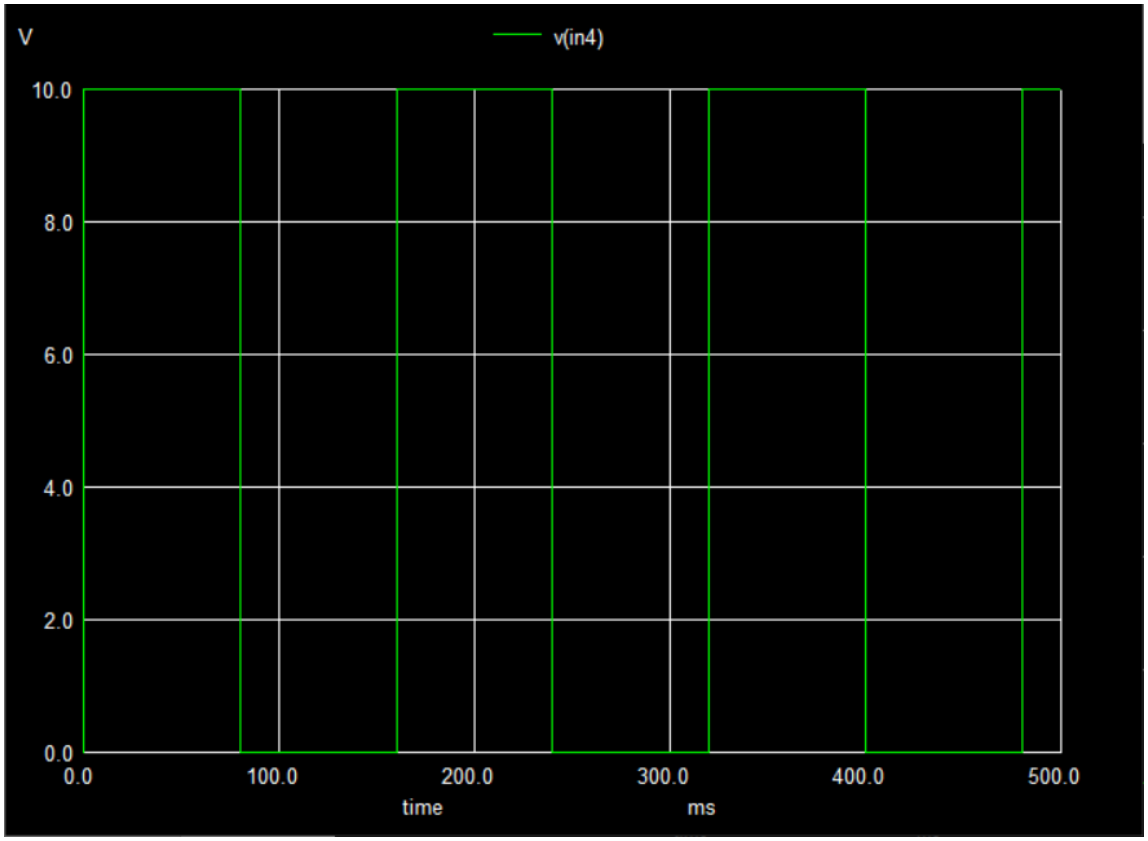
2) Plot(in(1)):-



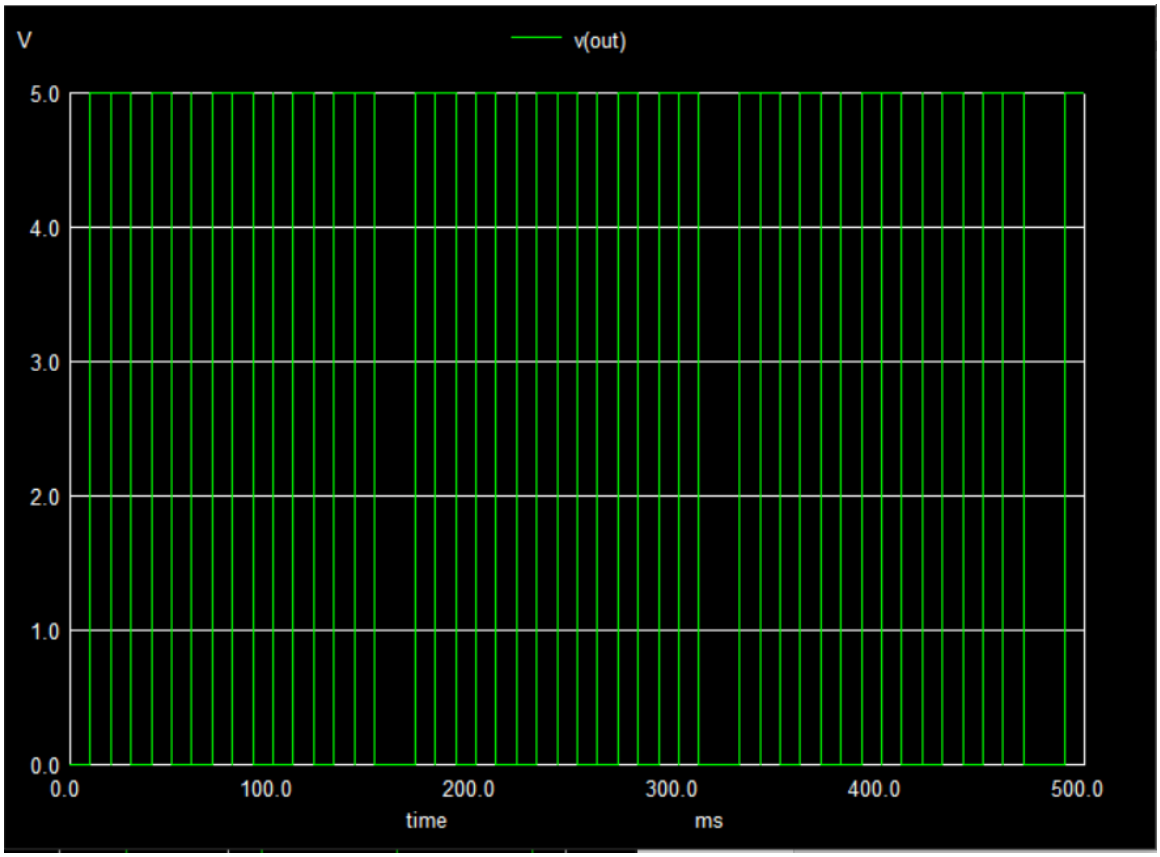
3) Plot(in(2)):-



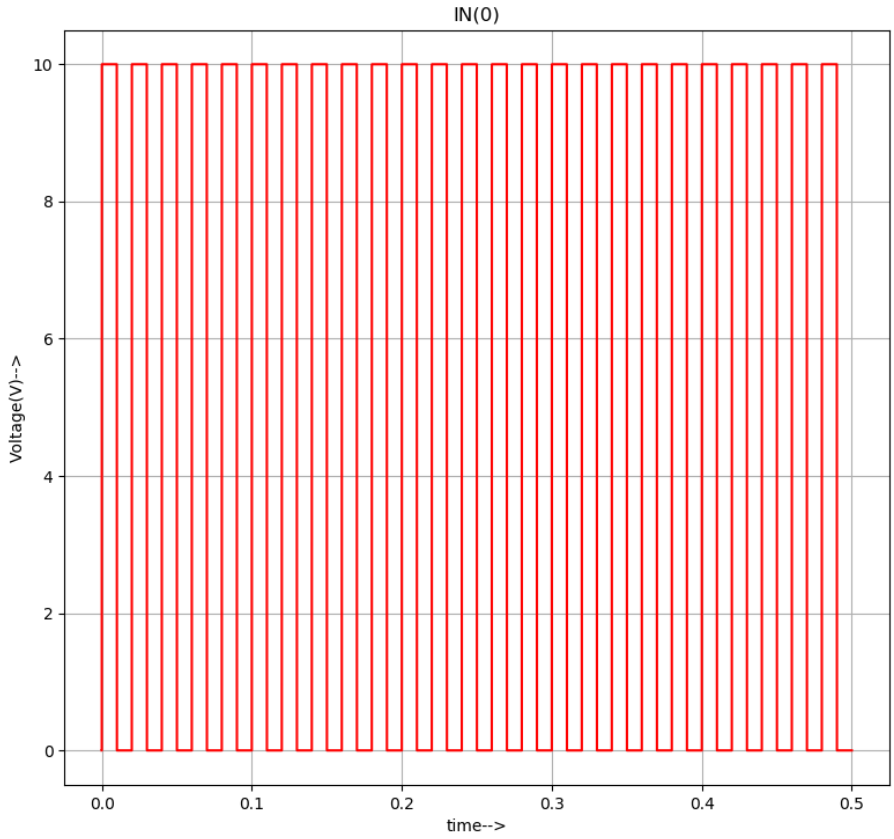
4) Plot(in(3)):-

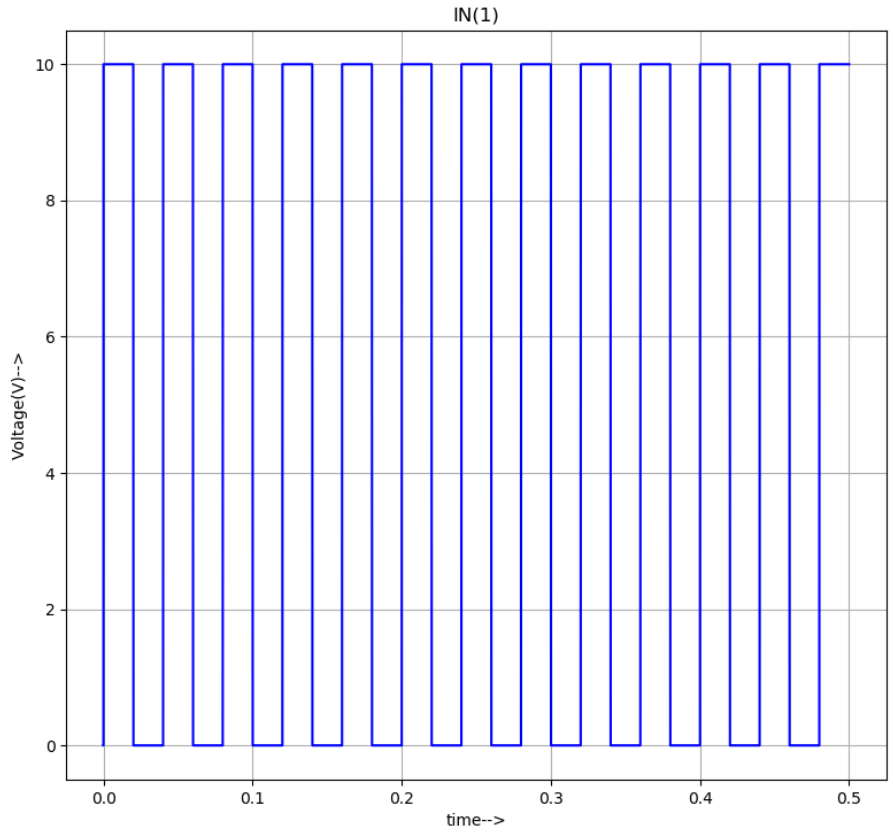


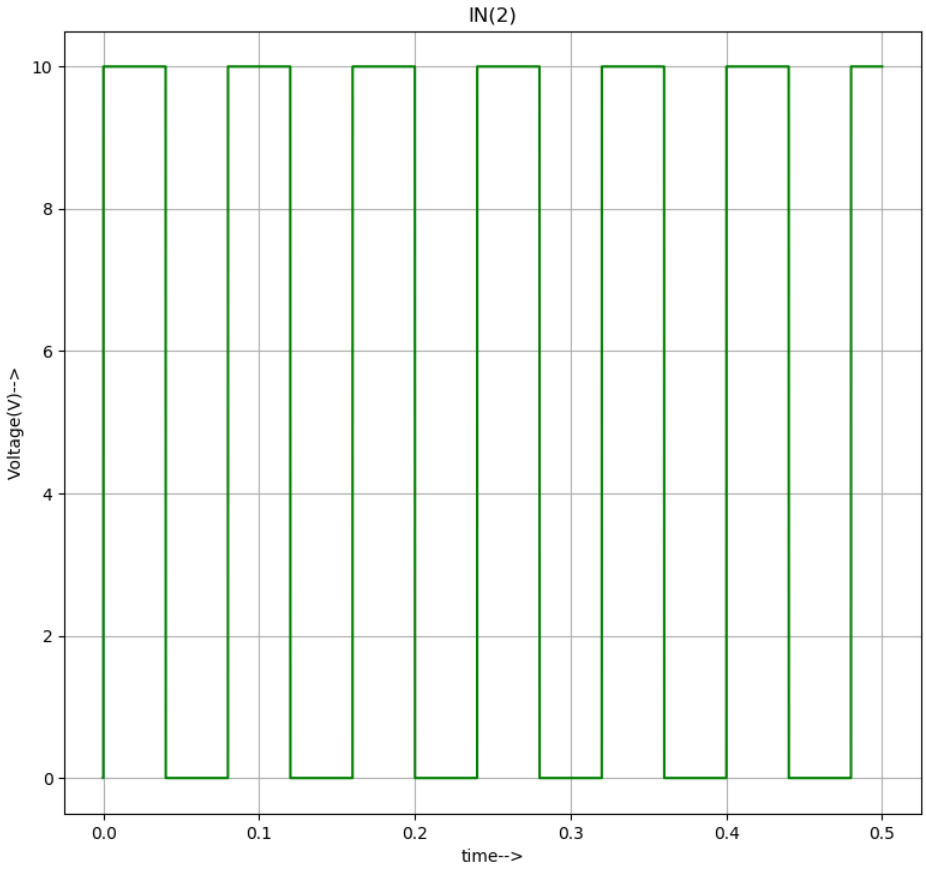
5) Plot(out):-



Python Plots:






IN(2)
Voltage(V)-->
time-->
0
2
4
6
8
10
0.0
0.1
0.2
0.3
0.4
0.5

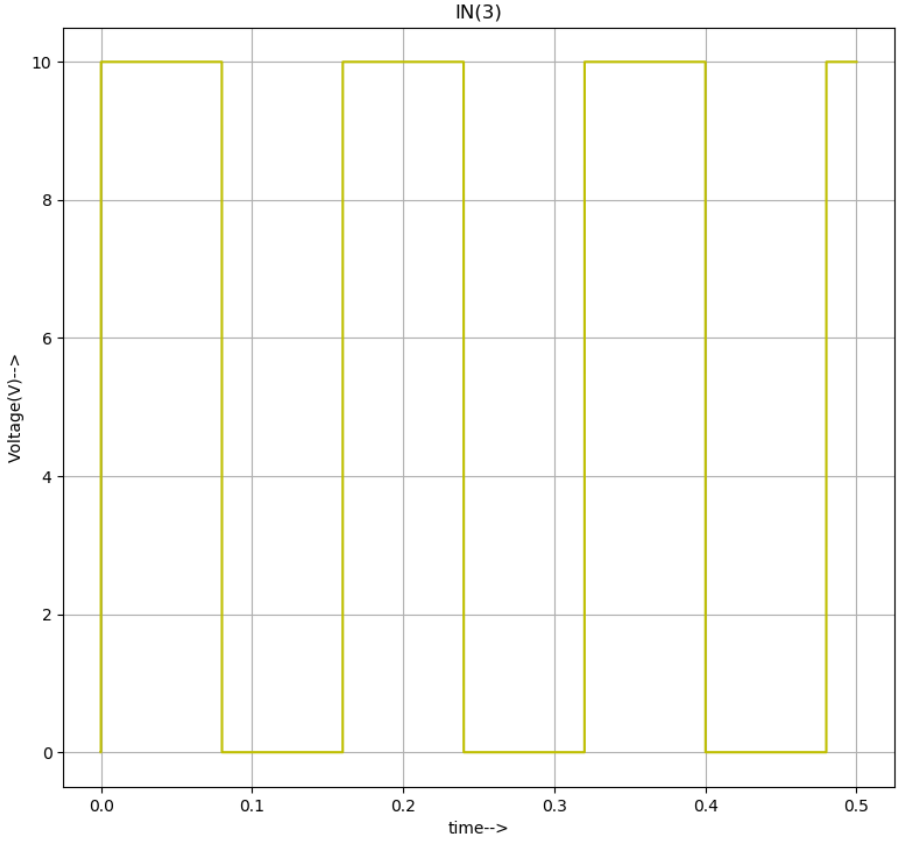

IN(3)
Voltage(V)-->
time-->
0
2
4
6
8
10
0.0
0.1
0.2
0.3
0.4
0.5

Table:

IN(3)	IN(2)	IN(1)	IN(0)	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Source/Reference(s) :

https://old.amu.ac.in/emp/studym/100006525.pdf

https://www.engineersgarage.com/vhdl/vhdl-tutorial-2-vhdl-programs/