JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
HYDERABAD - 500 085, TELANGANA STATE, INDIA.

CONSOLIDATED MARKS MEMO / CREDIT SHEET

M.Tech. EMBEDDED SYSTEMS & VLSI DESIGN

CMM. No. : C 0683284

Serial No. : 20224014975

Name : RANGA REDDY GARU KISHAN KUMAR RE

Hall Ticket No. : 13Q96D7717

Year of Admission : 2013-2014

Name of the College : CMEC,DHULAPALLI

Month & Year of Final Exam : February, 2016

Class Awarded : FIRST CLASS WITH DISTINCTION

S.No	SUBJECT TITLE	INT MARKS	EXT MARKS	Total Marks	Pass(P)/ Fail(F)
	Maximum Marks in Theory	40	60	100	
	Maximum Marks in Lab	40	60	100	
	I SEMESTER				
1	MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN	32	43	75	P
2	VLSI TECHNOLOGY AND DESIGN	38	33	71	P
3	CPLD AND FPGA ARCHITECTURES AND APPLICATIONS	35	28	63	P
4	CMOS ANALOG INTEGRATED CIRCUIT DESIGN	37	29	66	P
5	DIGITAL SYSTEM DESIGN	35	43	78	P
6	CMOS DIGITAL INTEGRATED CIRCUIT DESIGN	36	31	67	P
7	VLSI LABORATORY	39	57	96	P
8	SEMINAR	46	-	46	P
	II SEMESTER				
1	EMBEDDED C	36	31	67	P
2	CMOS MIXED SIGNAL CIRCUIT DESIGN	34	39	73	P
3	EMBEDDED REAL TIME OPERATING SYSTEMS	34	24	58	P
4	DESIGN FOR TESTABILITY	35	25	60	P
5	SYSTEM ON CHIP ARCHITECTURE	37	30	67	P
6	LOW POWER VLSI DESIGN	35	32	67	P
7	EMBEDDED SYSTEMS LABORATORY	35	52	87	P
8	SEMINAR	44	-	44	P
	III SEMESTER				
1	COMPREHENSIVE VIVA (Comprehensive VIVA External= 100)	-	95	95	P
	IV SEMESTER				
1	PROJECT WORK*	-	C	-	P
	(* A - Excellent, B - Good, C - Satisfactory, D - Un Satisfactory)				

Aggregate Marks Secured 1180 OUT OF 1600 (73.75%)

Date of Issue : April 16, 2016

(see overleaf for Rules concerned to award of class)

(*Courses registered but not counted for calculation of aggregate)

CONTROLLER OF EXAMINATIONS