

$(A \oplus B) C + AB$

MCA 113

Roll No.

MCA

2 0 2 2 1 0 4 0 2 7

ODD SEMESTER

Minor Test 2022 - 2023

Computer Organization & Architecture

Time: 02 Hrs

Max. Marks: 30

Note: Attempt ALL questions. Each question carries equal Marks.

Q.1 Attempt any **Three parts** of the following. Q. 1(a) is compulsory

a Find the value of x in the following:

$$\begin{array}{ll} \text{(i)} \quad (746003)_9 = (x)_{10} & \text{(ii)} \quad x = 11^{\text{th}} \text{ complement of } (9779)_{12} \quad (24442) \\ \text{(iii)} \quad (346)_9 \times (658)_9 = (x)_7 & \text{(iv)} \quad x = (10001)_2 - (1101)_2 \text{ subtract using } 2^{\text{'s}} \\ & \text{complement.} \end{array}$$

b (i) Simplify following Boolean function F together with the don't care conditions d in (i) sum of products and (ii) product of sums.

$$F(A, B, C, D) = \sum m(1, 4, 7, 8, 9, 11) + d(0, 3, 5)$$

(ii) Implement the Boolean function $F(A, B, C) = A'B'C' + ABC + B'C' + A'B'$ with NAND gate only.

c Simplify the following expressions to (I) sum-of-products and (II) products-or-sums: (3)

$$\begin{array}{ll} \text{(i)} \quad (A' + B' + D')(A + B' + C')(A' + B + D')(B + C' + D') & \\ \text{(ii)} \quad C'D + ABC' + ABD' + A'B'D & \end{array}$$

d (i) Find the minimum number of literals for the following function using 2 variable Karnaugh Map. $F = \sum m(1) + d(3)$. (3)

(ii) Implement the function $F = \sum m(0, 2)$ using a 2×4 decoder.

Q.2 Attempt any **Three parts** of the following. Q. 2 (a) is compulsory

a What is the disadvantage of binary adder? Explain how a look ahead adder speeds up the addition process. Clearly show the derivations of equations (4)

b Design a BCD to Excess-3 code converter using minimum number of NAND gates. (3)

c Implement the following function using 16:1 MUX, 8:1MUX and 4:1 MUX.

$$F(A, B, C, D) = \sum(0, 1, 2, 4, 5, 7, 10, 15) \quad (3)$$

d Design an Quad-to-binary priority encoder. Provide an output V to indicate that at least one of the inputs is a 1. The input with the lowest subscript number has the highest priority. What will be the value of four outputs if inputs D5 and D3 are 1 and the other inputs are all 0's? (4)

Q.3 Attempt any **Three parts** of the following. Q. 3(a) is compulsory

a Draw the logic diagram of a 4-bit binary ripple counter using flip-flops that trigger on the positive-edge transition.

b Design a synchronous counter which steers through the following states: S7-S6-S5-S2-S0 using J-K Flip flop.

c i Explain race around condition in JK flip-flop. Explain how a master slave flip flop avoids race around condition. (3)

ii Explain the procedure to convert JK flip flop into T flip flop.

d With the help of timing diagram and logic diagram, explain the working of Serial In Serial Out shift register and Parallel In Serial Out shift register using an example. (3)

propogate
propogate

$$\begin{array}{r}
 10001 \\
 168421 \\
 \hline
 17 \quad \longrightarrow \quad 13 \\
 & \quad \quad \quad 1101 \\
 & \quad \quad \quad 0421 \\
 & \quad \quad \quad 4 \\
 & \quad \quad \quad 12 \\
 & \quad \quad \quad 1100 \\
 & \quad \quad \quad 0421 \\
 & \quad \quad \quad 12 \\
 & \quad \quad \quad P \oplus B + C
 \end{array}$$

MCA
ODD SEMESTER
Minor Examination 2021 – 2022
Computer Organization & Architecture

Time: 02 Hrs

Max. Marks: 30

Note: Attempt ALL questions. Each question carries equal Marks.

Q.1 Attempt any Three parts of the following. Q. 1(a) is compulsory

- a. Design a BCD to decimal decoder using the unused combinations of the BCD code as don't care conditions. (4)
- b. Find the value of x in the following: (3)
- (i) $(74246.25)_8 = (x)_{10}$ (30 88 6 . 32) (ii) $x = 10^{\text{th}}$ complement of $(978)_{11}$ $(156)_{10} / (132)_{11}$
 (iii) $(345)_6 \times (523)_6 = (x)_6$ (32 34 0 3) (iv) $x = (11010)_2 - (1101)_2$ subtract using 2's complement. (1101)
- c. Simplify the following expressions to (I) sum-of-products and (II) products-or-sums: (3)

(i) $(A + C' + D')(A' + B' + D')(A' + B + D')(A' + B + C')$

(ii) Convert the expression $Y = (A+B)(A+C)(B+C')$ into standard POS form.

d. What is a multiplexer? Implement the following function using 16:1 MUX, 8:1MUX and 4:1 MUX: ✓

$$F(A,B,C,D) = \sum(0,1,2,3,4,5,7,10,14,15) \quad (3)$$

Q.2 Attempt any Three parts of the following. Q. 2 (a) is compulsory

- a. (i) Show the three different representations for a negative decimal number $N = -25$ in binary. (4)
 (ii) Give the truth table, characteristics table, excitation table and characteristic equation of SR flip-flop. ↗ S0P ↗ POS

- b. (i) Obtain the two canonical forms of the Boolean function $F(A,B,C) = A'B + BC' + BC + AB'C'$ (3)
 (ii) Simplify the Boolean function $F = AB' + AB + BC$. Draw the circuit using basic gates. How many logic gates do you save by simplification? ↗ A + BC ↗ B = D ↗ Y

- c. Design a combinational circuit that converts a four-bit reflected code (gray code) number to a four bit binary number. Implement the circuit with exclusive-OR gates. (3)

- d. Minimize the following Boolean function using K-map and implement the simplified function using NAND gates only. (3)

$$F(A,B,C,D) = \sum(3,5,6,7) + d(10,11,12,13,14,15) \quad (3)$$

Q.3 Attempt any Three parts of the following. Q. 3(a) is compulsory

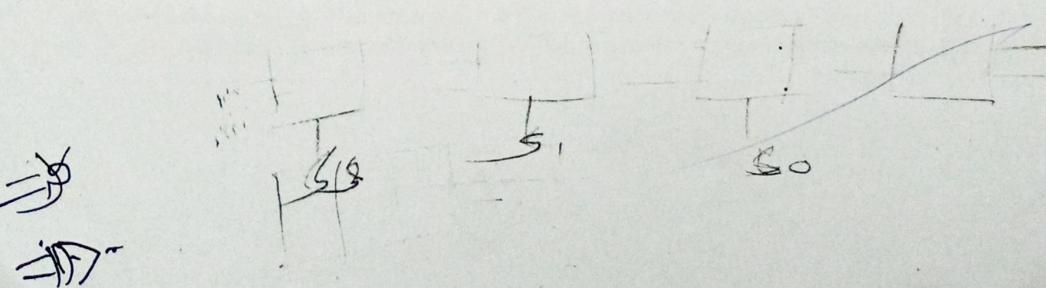
- a. Design a synchronous counter which steers through the following states: S0-S6-S2-S7-S5-S3 using J-K Flip flop. (4)

- b. Design a 4-line to 2-line priority encoder. Include an output E to indicate that at least one input is a 1. (3)

- c. Explain race around condition in JK flip-flop. Explain how a master slave flip flop avoids race around condition. (3)

- d. What is the disadvantage of binary parallel adder? Explain how a look ahead adder speeds up the addition process. Clearly show the derivations of equations. (3)

10101



ODD SEMESTER

Minor Test 2018 – 2019

Computer Organization & Architecture

Time: 02 Hrs

Max. Marks: 30

Note: Attempt ALL questions. Each question carries equal Marks.

Q.1 Attempt any **Three parts** of the following. Q. 1(a) is compulsory

a Find the value of x in the following:

- (i) $(746003)_8 = (x)_{10}$ (ii) $x = 11^{\text{th}}$ complement of $(9779)_{12}$
 (iii) $(3463)_7 \times (6523)_7 = (x)_7$ (iv) $x = (11010)_2 - (1101)_2$ subtract using 2's complement.

b (i) Minimize the following Boolean function using K-map and implement the simplified function using NAND gates only. (3)

$$F(A,B,C,D) = \sum m(0,1,2,3,7,8,10) + d(5,6,11,15)$$

(ii) Implement the Boolean function $F = A'B'C + A'BC' + A'C'$ with NAND gate only.

d Simplify the following expressions to (I) sum-of-products and (II) products-or-sums: (3)

- (i) $(A + C' + D')(A' + B' + D')(A' + B + D')(A' + B + C')$
 (ii) $C'D + ABC' + ABD' + A'B'D$

e Given the Boolean expression $F = x'y + xyz'$: (3)

- (i) Derive an algebraic expression for the complement F' .
 (ii) Show that $F \cdot F' = 0$
 (iii) Show that $F + F' = 1$

Q.2 Attempt any **Three parts** of the following. Q. 2 (a) is compulsory

Design a 4 bit carry look ahead generator with suitable diagram. (4)

Design a BCD to decimal decoder using the unused combinations of the BCD code as don't care conditions. (3)

c Draw the logic diagram of a 2 to 4 line decoder with only NAND gates. Include an enable input. (3)

d (i) Implement the following four Boolean expressions with three half adders: (3)

$$D = A'B'C + A'B'C' + AB'C + ABC$$

$$E = A'BC + A'B'C$$

$$F = AB'C + (A' + B')C$$

$$G = ABC$$

(ii) Construct a 32×1 multiplexer with only 2×1 multiplexers. Use block diagrams.Q.3 Attempt any **Three parts** of the following. Q. 3(a) is compulsory

Design a quad-to-binary priority encoder. Provide an output V to indicate that at least one of the inputs is 1. The input with the lowest subscript number has the highest priority. (4)

Implement the following function using 16:1 MUX, 8:1MUX and 4:1 MUX.

$$F(A,B,C,D) = \sum(2,4,5,7,10,15)$$

c Draw the schematic diagram of J-K flip flop and describe its working. Write down its truth table. (3)

d Design a 5-to-32-line decoder using a 3-to-8-line decoder, a 2-to-4-line decoder, and 32 2-input AND gates. (3)

(3)

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MCA (1st Sem)
QDD SEMESTER
 Minor Test 2017-2018

Computer Organization and Architecture

Time: 02 Hrs

Max. Marks: 30

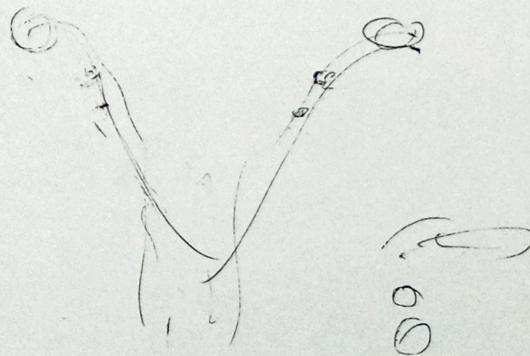
Q.1		Attempt any Three parts of the following Q. 1(c) is compulsory	
<u>a</u>		Find the value of x in the following:	
	*	(i) $(653)_7 \times (523)_7 = (x)_7$	(ii) $(D6C.5B)_{16} = (x)_4$
	*	(iii) $x = (11010)_2 - (1101)_2$ subtract using 2's complement.	(iv) $(21340)_5 = (x)_{10}$
<u>b</u>		<p>(i) Prove that $(A+B'+AB)(A+B')(A'B) = 0$.</p> <p>(ii) Implement the Boolean function $F = A'B'C + A'BC' + A'C'$ with NAND gate only.</p> <p>(iii) Reduce the following Boolean to required number of literals. $(w + y + z)(w + y + z')(w + y + z)(w + x')$ to four literals.</p>	
<u>c</u> *		Design a 4 bit carry look ahead generator with suitable diagram.	
<u>d</u> *		(i) Draw the logic diagram of a 2×4 line decoder with enable input	
		<p>(ii) A combinational circuit is defined by the following three functions:</p> $F_1 = x'y' + xyz'$ $F_2 = x' + y$ $F_3 = xy + x'y'$ <p>Design the circuit with a decoder and external gates.</p>	
Q.2		Attempt any Three parts of the following Q. 2(d) is compulsory	
<u>a</u>		Convert the decimal number 125.25 to base 3, base 4, base 6, base 7, base 8, base 9, base 11, base 16.	
<u>b</u>		Design a combinational circuit that accept a three bit number and generates an output binary number equal to the square of the input number.	
<u>c</u>		<p>(i) Implement a Full subtractor with two half subtractor and an OR gate.</p> <p>(ii) Minimize the given Boolean function using K-map and implement the simplified function using NAND gates only. $F(A,B,C,D) = \sum m(0,1,2,3,7,8,10) + d(5,6,11,15)$</p>	
<u>d</u>		<p>(i) Obtain the simplified expression in (i) Sum of products (ii) Product of sums: $(A' + B' + D)(A' + D')(A + B + D')(A + B' + C + D)$</p> <p>(ii) Simplify the Boolean function F using the don't care condition d. in (i) sum of products (ii) product of sums:</p> $F = w'(x'y' + x'y + xyz) + x'z'(y + w)$ $d = w'x(y'z + yz') + wyz$	
Q.3		Attempt any Three parts of the following Q. 3(a) is compulsory	
<u>a</u>		Design a BCD to decimal decoder using the unused combinations of the BCD code as don't care conditions.	
<u>b</u>		(i) Construct a 32×1 multiplexer with 4×1 multiplexers. Use block diagrams.	

	(ii)	Implement full adder with the help of (I) NAND gates (II) NOR gates.
c	(i)	Design a 4-line to 2-line priority encoder. Include an output E to indicate that at least one input is a 1.
	(ii)	Implement the following functions using a 4-to-16 line decoder $F(A, B, C, D) = \sum (1, 2, 4, 7, 8, 11, 12, 13)$
d		Implement the following functions with (I) 16:1 MUX (II) 8:1 MUX (III) 4:1 MUX :- $F(A, B, C, D) = \sum (0, 2, 3, 6, 8, 9, 11, 12, 14)$

P₃ P



full subtractor with Multiplexer
 with two Half subtractor
 4bit
 Convert grey code into binary number implementing ~~MUX OR~~?



Roll No.									
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MCA (SEMESTER I) 2022 – 2023
 ODD SEMESTER
 Major Examination

Subject Code: MCA 113

Subject: Computer Organization & Architecture

Time: 03 Hrs

Max. Marks: 50

Note: Attempt ALL questions. Each question carries equal Marks.

Q.1 Attempt any five parts of the following:

(5 * 2 = 10)

a Find the value of x in the following:

$$(i) (23412)_7 = (x)_{10} \quad (ii) (846)_9 \times (573)_9 = (x)_9$$

b Convert the following expressions into sum-of-products and product-of sums forms:

$$\overline{AA} = 1$$

$$(i) (AB + C)(B + C'D)$$

$$(ii) X' + X(X + Y')(Y + Z')$$

c Simplify the following expressions F together with the don't care conditions d in (I) sum-of-products form and (II) products-or-sums forms:

$$F(w,x,y,z) = \sum(3, 5, 6, 7)$$

$$d(w,x,y,z) = \sum(10, 11, 12, 13, 14, 15)$$

d Implement the following function with (i) 16:1 (ii) 8:1 and (iii) 4:1 multiplexer:

$$F(A,B,C,D) = \sum(2,4,5,7,10,14)$$

e Design an Quad-to-binary priority encoder. Provide an output V to indicate that at least one of the inputs is a 1. The input with the lowest subscript number has the highest priority. What will be the value of four outputs if inputs D5 and D3 are 1 and the other inputs are all 0's?

f Design a synchronous counter which steers through the following states: S7-S6-S5-S3-S2-S0 using J-K Flip flop.

g Design a combinational circuit that generated the 9's complement of a BCD digit.

Q.2 Attempt any two parts of the following: (2 * 5 = 10)

a What is the disadvantage of binary parallel adder? Explain how a look ahead adder speeds up the addition process. Clearly show the derivations of equations.

b What do you understand by hardwired control unit? Give various methods to design hardwired control unit. Describe one of the design methods for hardwired control unit with suitable diagram.

c i Design 4-bit Arithmetic Circuit that performs Addition, Subtraction, Increment and Decrement operations.

ii The outputs of four register R0, R1, R2, R3 are connected through 4-1 multiplexers to the inputs of the fifth register, R5. Each register is 8 bits long. The required transfer are dictated by four timing variables T0 through T3 as follows:

$$T_0 : R_5 \leftarrow R_0$$

$$T_1 : R_5 \leftarrow R_1$$

$$T_2 : R_5 \leftarrow R_2$$

$$T_3 : R_5 \leftarrow R_3$$

Draw a block diagram showing the hardware implementation of register transfers.

Q.3 Attempt any two parts of the following: (2 * 5 = 10)

a Write a program to evaluate the arithmetic statement:-

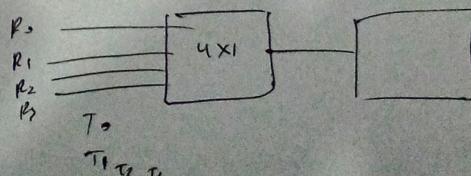
$$X = (A - B * C) / (D * E + F / G - H * I + J)$$

Using Three, Two, One and Zero address Machines.

push
pop
tos

\$
Acc
store
load

²
Mov



marks: 4

- b Show the basic organization of a CPU in terms of registers and other units for a Single-bus – organization. In such a CPU, show the complete action of the CPU in fetching and executing the instruction.

- c₁ Design a variable length opcode to allow all of the following to be encoded in a 36-bit instruction:

- I. Instruction with two 15-bit addresses and one 3-bit register number.
- II. Instruction with one 15-bit addresses and one 3-bit register number.
- III. Instruction with no address or register.

- c₂ Draw a diagram of bus system for four registers of 2-bits each. The bus is to be constructed with multiplexers.

- Q.4 Attempt any two parts of the following: (2 * 5 = 10)

- a 4K x 16 RAM chips are used to construct 128K x 64 Memory. How many chips will be required? Draw a connection diagram.

- b Obtain the truth table of an 8x3 priority encoder. Assume that the three outputs xyz from the priority encoder are used to provide a vector address of the form 101xyz00. List the eight vector addresses starting from the one with the highest priority.

- c Discuss the concept and implementation of virtual memory. Also describe a suitable scheme for translation from logical address to physical address.

- Q.5 Attempt any two parts of the following: (2 * 5 = 10)

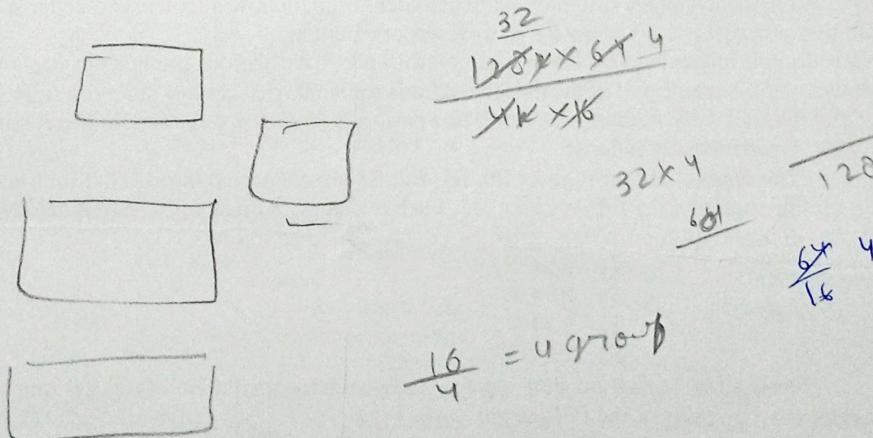
- a₁ A block set associative cache consists of a total of 256 blocks divided into eight block sets. The main memory containing 8192 blocks each consisting of 64 words.

- (i) How many bits are there in the main memory address?
- (ii) How many bits are there in each of TAG, SET and WORD field?

- b₁ What is cache memory? Consider a system having 512K main memory organized as 16K blocks of 32 words each and a cache memory of 16K arranged as 512 blocks of 32 words each. Show how the mapping is done using direct mapping.

- b₂ Describe DMA with suitable block diagram. Why does DMA have priority over the CPU when both request a memory transfer? Explain.

- c What are the basic advantages of priority interrupt over a non-priority system? Is it possible to have a priority interrupt without a mask register? Discuss.



①
2² x 2²
2¹²

M.C.A.
(SEM I) ODD SEMESTER
MAJOR EXAMINATION 2014 - 2015

COMPUTER ORGANIZATION & ARCHITECTURE

Max. Marks: 4

Time: 3 Hrs.

Note: Attempt ALL questions. Each question carries equal Marks.

Q.1 Attempt any three of the following. Q.1 (a) is compulsory. (4)

a Find the value of x in the following:

(i) $(835)_{10} = (x)_{100}$

(ii) $(E7B.4B)_{16} = (x)_4$

(iii) $(346)_7 \times (563)_7 = (x)_7$

(iv) $(12.354)_{10} = (x)_2$

(3)

b

(i) Reduce the Boolean expression $A'B(D' + C'D) + B(A + A'C'D)$ to one literal.

(ii) Implement the Boolean function $F = xy'z + x'yz' + x'z'$ with NAND gate only.

c Simplify the following expressions to (I) sum-of-products and (II) products-of-sums: (3)

(i) $(A + C + D')(A' + B + D')(A' + B + C')$

(ii) $C'D + ABC' + ABD' + A'B'D$

d With the use of maps, find the simplest sum-of-products form of the function $F = f(g)$, where $f = abc' + c'd + a'cd' + b'cd'$ and

$g = (a + b + c' + d')(b' + c' + d)(a' + c + d')$

(3)

Q.2 Attempt any three of the following. Q.2 (a) is compulsory. (4)

a Design 4 bit carry look ahead generator.

b Design a BCD to decimal decoder using the unused combinations of the BCD code as don't care conditions.

(3)

c Construct a 32x1 multiplexer with only 2x1 multiplexers. Use block diagrams.

(3)

d Draw the logic diagram of a 2 to 4 line decoder with only NOR gates. Include an enable input. (3)

Q.3 Attempt any three of the following. Q.3 (a) is compulsory.

a Write a program to evaluate the arithmetic statement:-

$$X \leftarrow A + B * [C * D + E * (F + G) * H]$$

(4)

b Using Three, Two, One and Zero address Machines.

The outputs of four register R0, R1, R2, R3 are connected through 4-1 multiplexers to the inputs of the 1 register, R5. Each register is 8 bits long. The required transfer are dictated by four timing variables T0 through T3 as follows:

$$T0 : R5 \leftarrow R0$$

$$T1 : R5 \leftarrow R1$$

$$T2 : R5 \leftarrow R2$$

$$T3 : R5 \leftarrow R3$$

c Draw a block diagram showing the hardware implementation of register transfers. (3)

d Design 4-bit Arithmetic Circuit that performs Addition, Subtraction, and Increment and Decrement operations. (3)

e Design an efficient logic circuit shared by different branch conditions derived from the combination of the Flag register bits S (sign), V (overflow), C (End carry), Z (all 0's). Specify the standalone status of the Flag register bits S (sign), V (overflow), C (End carry), Z (all 0's). Specify conditional branch instructions which can be supported by the circuit you have designed. (3)

Q.4 Attempt any three of the following. Q.4 (c) is compulsory.

a 8K x 1 RAM chips are used to construct 32K x 16 Memory. How many chips will be required? Draw connection diagram. (3)

b A block set associative cache consists of a total of 64 blocks divided into four block sets. The main memory contains 4096 blocks each consisting of 128 words.

i How many bits are there in the main memory address?

ii How many bits are there in each of TAG, SET and WORD field? (3)

c Describe DMA with suitable block diagram. Why does DMA have priority over the CPU when both request memory transfer? Explain. (4)

d Discuss the concept and implementation of virtual memory. Also describe a suitable scheme for translation of logical address to physical address. (4)

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M.C.A.
(SEM I) ODD SEMESTER
MAJOR EXAMINATION 2015 - 2016

COMPUTER PROGRAMMING WITH C

Time: 3 Hrs.

Max. Marks:

Note: Answer all questions.

- Q.1 Attempt any Three parts of the following. Q. 1(a) is compulsory.
- Discuss the different phases of Software Development Life Cycle.
 - Explain the memory hierarchy by drawing a suitable diagram.
 - What do you understand by software? Explain the various types of Operating System.
 - Define algorithm. Write an algorithm to find out the longest word from a given line written in English language.

Q.2 Attempt any Three parts of the following. Q.2(a) is compulsory.

- Explain the different types of operators in detail. What do you mean by associativity and precedence of an operator?
- Write a program in C to sum the following series

$$1/2! + 2/3! + 3/4! + \dots \dots \dots n \text{ terms where } n! \text{ denotes factorial of } n.$$
- Write a program in C to read a number from keyboard and print it in figure form. As for example input: 152 output: ONE FIVE TWO
- Write a program to print the following pattern

A
A B A
A B C B A

A B C ... Y Z Y ... C B A

Q.3 Attempt any Three parts of the following. Q. 3(a) is compulsory.

- What is structure? Declare a structure "emp" which has empid, name, salary and gender as fields. Now write a program in C which takes n records as input and print the average salary of male and female employee separately. Make suitable assumptions..

(b) Implement Binary Search in C. What is the limitation of Binary Search?

- Write a program in C to input name consisting of First Name, Middle Name and Last Name and print the name in following form.

Input: Madan Mohan Malaviya Output: M.M. Malaviya

- What is the significance of using recursion? Write a recursive function to multiply two numbers