28Pins

Variant: [No Variations]

03-12-2022
V1I1

DESIGN CONSIDERATIONS

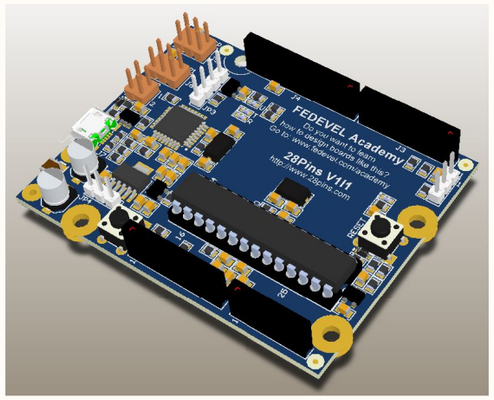
DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for debug notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.



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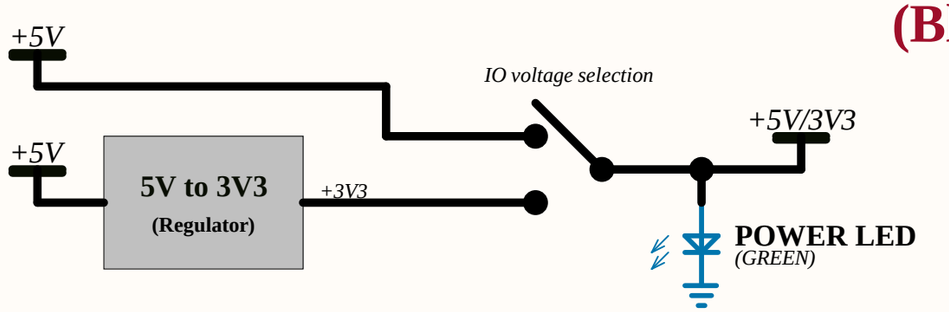
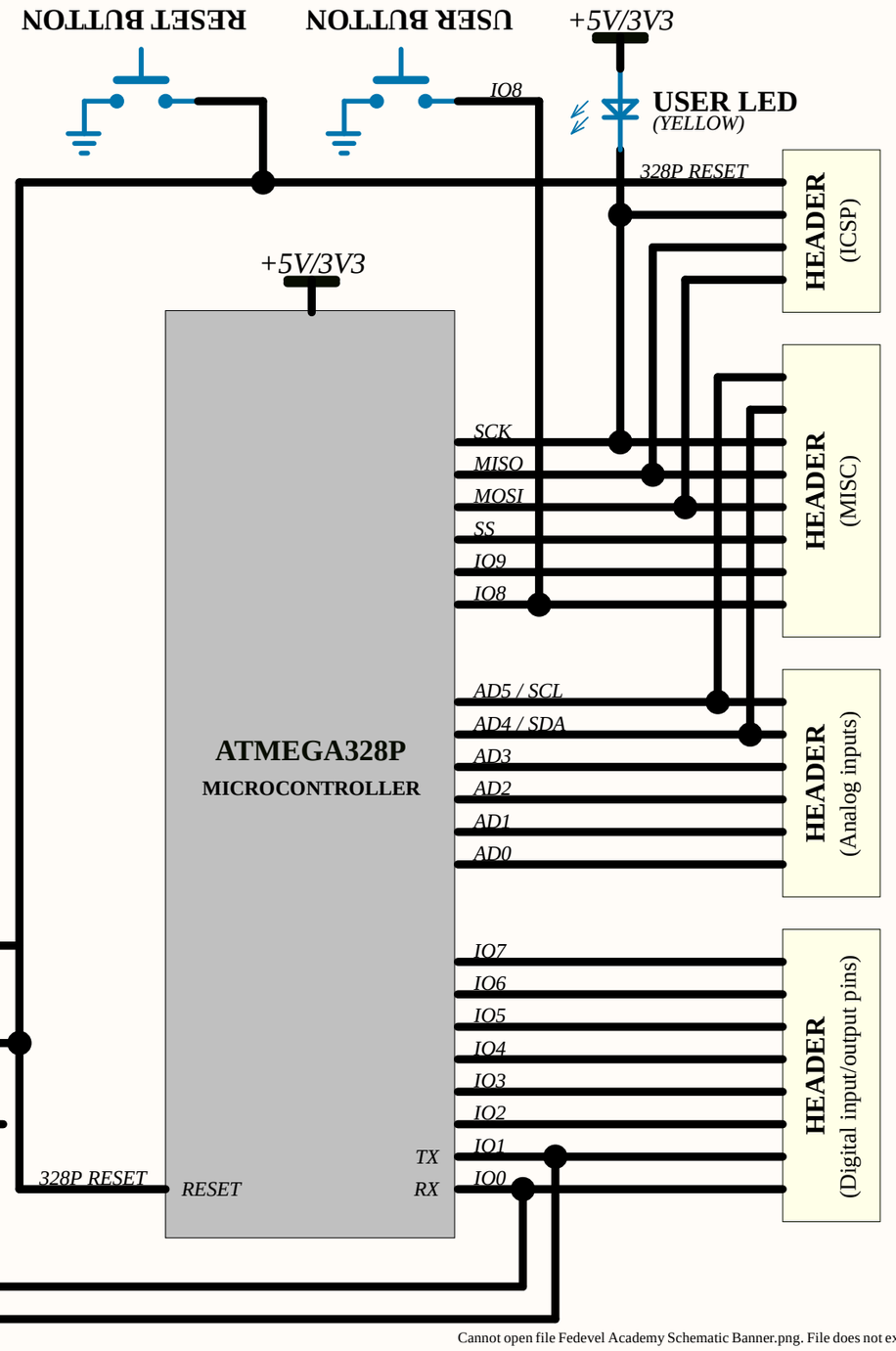
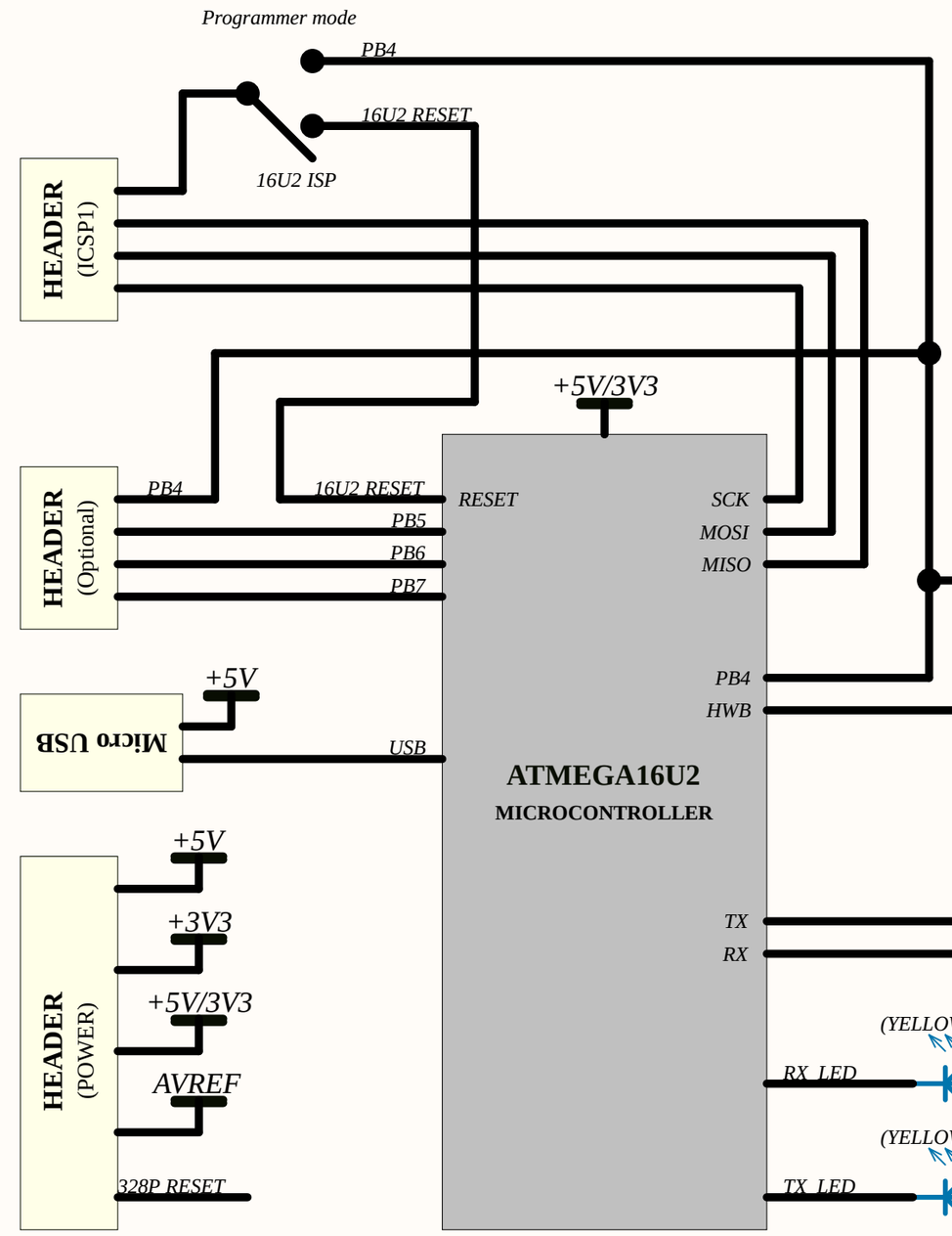
28Pins
(Block Diagram)







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28PINS - SCHEMATIC

LAYOUT NOTE:
1) Route all the POWER tracks with minimum track width 0.4mm.

2) Route all the other tracks by 0.4mm and change them by the end of the design to 0.2mm. To change all of them at once, use this filter "(not InNet('+*') and not InNet('GND')) and IsTrack and (OnLayer('L1') or OnLayer ('L2'))" and then set 0.2mm width in PCB Inspector panel.

DESIGN NOTE:
This board supports 5V or 3V3 voltage level on the IO pins:

1) 5V IO - Fit everything as defined in this schematic. NF means, do not fit this component.

2) 3.3V IO - Remove R14, Fit R15, *Replace Y1 (change from 16MHz to 10MHz), *Replace Y2 (change from 16MHz to 8MHz).

3) Both 5V and 3V3, selected through JP4 - Remove R14, Remove R15, Fit JP4, *Replace Y1 (change from 16MHz to 10MHz), *Replace Y2 (change from 16MHz to 8MHz).

*Note: The 16MHz crystals are not recommended for 3.3V operation. We need to adjust their values, thats why the change.

IMPORTANT: Once you change the crystal value, you may need to re-compile your source code.

DESIGN NOTE:

About JP3:
1) DebugWire support - Short 1&2. This was added to support possible debugWire debugging (programming?) of 328P through 16U2. In this case, the 16U2 needs to have a correct firmware and has to behave as a debugWire tool.

2) ISP programmer mode - Short 2&3. In this case, take a cable and connect J5 & J6 together. Upload AVRISP MKII firmware into 16U2 and you can program 328P. Example of AVRISP MKII firmware can be found at LUFA projects: http://www.fourwalledcubicle.com/LUFA.php (Tip: remap LEDs of the default AVRISP MKII LUFA project to the RX and TX LEDs on the 28Pin board)

3) ISP header - Short 3 & 4. In this mode, the ICSP1 header is used as a standard ISP header

DESIGN NOTE:

About JP1:
1) Autoreset Enabled - Short 1&2. In this case, 16U2 is used to reset 328P when firmware inside 328P is updated from Arduino IDE.

2) 16U2 DFU mode Enabled - Short 2&3. 16U2 HWB pin is sampled by 16U2 during RESET. If pulled low, then after Reset the 16U2 will go into DFU mode (it's the mode when you can flash 16U2 firmware through USB and Atmel Flip software: http://www.atmel.com/tools/flip.aspx).

Micro USB

J7 10118193-0001LF
L1 2u2/2A
C5 100u/10V
C6 100u/10V
R9 0R
Z1 CG0603MLC-05E
Z2 CG0603MLC-05E
Differential pair
CON_USB_N
CON_USB_P

16U2

U1 ATMEGA16U2-AU
FB1 MPZ2012S601AT000
C1 10uF/16v
C2 100n
C3 100n
R4 NF
C4 100n
R5 10K
C7 1uF / 25V
R1 560R
R2 560R
R3 100K
D1 Orange
D2 Orange
R7 22R
R8 22R
C9 18p
C10 18p
Y1 16U2_16MHZ_XTAL1
R10 1M
ABM7-16.000MHZ-D2Y-T

JP2

JP2 HDR 2x2 NF

ICSP1

J6 HDR 2x3
R6 22R
C8 100n

JP3

JP3 HDR 1x4
LINK1 LINK
LINK2 LINK

JP1

JP1 HDR 1x3
C11 100n
R13 1K

POWER PADS

J8 4MMx1.5MM
J9 4MMx1.5MM

POWER

C12 100n
C13 100n
C14 100n
C15 10uF/16v
J1 HDR FEMALE 1x8 2.54mm

Power Selection

R14 0R
R15 NF
JP4 HDR 1x3
LINK3 NF
LINK

DESIGN NOTE:
This board can be powered from micro USB connector (J7) or a single +3.3V power rail (through J1 pin 4). If +3.3V is used, fit R4 and R15. In this case, JP4 & R14 must NOT be fitted, otherwise the board may be damaged.

3V3 LDO

U2 TL1963A-33DCQR
C16 10uF/16v
C17 10uF/16v

ICSP

J5 HDR 2x3
C18 100n

328P

U3 ATMEGA328P-PU
FB2 MPZ2012S601AT000
FB3 MPZ2012S601AT000
C20 10uF/16v
C21 100n
C22 10uF/16v
C23 100n
C24 100n
R19 10K
C26 18p
C27 18p
Y2 328P_16MHZ_XTAL1
R20 1M
ABM7-16.000MHZ-D2Y-T
R22 22R
R16 SCK
C19 10uF/16v

IOH

J4 HDR FEMALE 1x10 2.54mm

AD

J2 HDR FEMALE 1x6 2.54mm

IOL

J3 HDR FEMALE 1x8 2.54mm

DIP SOCKET

SCKT FOR U1
28-DIP SOCKET
28-DIP Socket

MOUNTING HOLES

MH1 Text
MH2
MH3
MH4

FIDUCIALS

FID1
FID2
FID3
FID4

POWER LED

R18 560R
D4 Green

USER LED

R17 560R
D3 Orange
C25 100n
U4 SN74AHC1G09DBVR

RESET (16U2)

D5 SDM20U30Q-7
R21 10K
R22 22R
C29 100n
C28 100n
U5 SN74AHC1G09DBVR

RESET (328P)

D6 SDM20U30Q-7
R23 10K
R28 22R
C32 100n
R25 10K
C30 100n
U6 SN74AHC1G09DBVR
SW1 1825910-6

USER BUTTON

R24 10K
R27 22R
C33 100n
R26 560R
C31 100n
U7 SN74AHC1G09DBVR
SW2 1825910-6

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Title		
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REVISION HISTORY

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Designator
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Designator
[02] - BLOCK DIAGRAM.SchDoc

Designator
[03] - 28PINS SCHEMATIC.SchDoc

Designator
[04] - REVISION HISTORY.SchDoc

NOTES

Mark Not Fitted Components as
NF

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

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