Date:__________________

Quiz for Chapter 1 Computer Abstractions and Technology

Not all questions are of equal difficulty. Please review the entire quiz first and then budget your time carefully.

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Solutions in Red

1. [15 points] Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 – Cycles/Instruction Class	Machine M2 – Cycles/Instruction Class	Frequency
A	1	2	60%
B	2	3	30%
C	4	4	10%

(a) Calculate the average CPI for each machine, M1, and M2.

For Machine M1:

Clocks per Instruction = (60/100)* 1 + (30/100)*2 + (10/100)*4

= 1.6

For Machine M2:

Clocks per Instruction = (60/100)*2 + (30/100)*3 + (10/100)*4

= 2.5

(b) Calculate the average MIPS ratings for each machine, M1 and M2.

For Machine M1:

Average MIPS rating = Clock Rate/(CPI * 10^6)

= (80 * 10^6) / (1.6*10^6)

= 50.0

For Machine M2:

Average MIPS rating = Clock Rate/(CPI * 10^6)

= (100 * 10^6) / (2.5*10^6)

= 40.0

(c) Which machine has a smaller MIPS rating ? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Machine M2 has a smaller MIPS rating. If we change the CPI of instruction class A for Machine M2 to 1, we can have a better MIPS rating than M1 as follows:

Clocks per Instruction = (60/100)*1 + (30/100)*3 + (10/100)*4
= 1.9
Average MIPS rating = Clock Rate/(CPI * 10^6)
= (100 * 10^6) / (1.9*10^6)
= 52.6

3. [5 points] Suppose that we can improve the floating point instruction performance of machine by a factor of 15 (the same floating point instructions run 15 times faster on this new machine). What percent of the instructions must be floating point to achieve a *Speedup* of at least 4?

We will use Amdahl's Law again for this question.
Let x be percentage of floating point instructions. Since the speedup is 4, if the original program executed in 100 cycles, the new program runs in 100/4 = 25 cycles.

$$(100)/4 = (x)/15 + (100 - x)$$

Solving for x, we get:

$$x = 80.36$$

The percent of floating point instructions need to be 80.36.

4. [6 points] Just like we defined MIPS rating, we can also define something called the MFLOPS rating which stands for Millions of Floating Point operations per Second. If Machine A has a higher MIPS rating than that of Machine B, then does Machine A necessarily have a higher MFLOPS rating in comparison to Machine B?

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A higher MIPS rating for machine A compared to machine B need not imply a higher MFLOPS rating for that machine A. One reason for this can be the following: It is possible that the floating point instructions form a fairly low proportion of the all the instructions in a given program. So if the floating point operations of machine B are far more efficient than the floating point operations of machine A while the other (integer, memory etc) instructions are more efficient on B, then machine B gets a higher MFLOPS rating than A while A has a higher MIPS rating.

7. [25 points] A two-part question:

in the program before MMX optimization

(Part A)

Assume that a design team is considering enhancing a r a extension instruction) hardware to a processor. When a on the MMX hardware, it is 10 times faster than the normal m of time that could be spent using the MMX mode the *percentag*

(a) What percentage of *media enhancement* is needed t

We will use Amdahl's Law for this question.

Execution time with Media Enhancement =

(Execution time improved by Media enhancement)/(Amount of Improv

in the program after MMX optimization

Execution time unaffected

Let x be the percent of media enhancement needed for achieving an overall speed

(100)/2 = (x)/10 + (100-x)

Solving for x, we have x = 55.55

(b) What percentage of the run-time is spent in MMX mode if a speedup of 2 is achieved? (Hint: You will need to calculate the new overall time.)

The new overall time is 100/2 = 50. Now 55.55 of the original program used media enhancement. Let x be the percentage of the new run-time that is spent in MMX mode (for a speedup of 2).

x = (55.55 *50)/100 = 27.78

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(c) What percentage of the media enhancement is needed to achieve one-half the maximum speedup attainable from using the MMX mode?

The maximum speedup using MMX mode occurs when the whole program can run in media enhancement mode. The maximum speedup in this case is 10. One-half of this is 15. Plugging in 15 instead of 2 in (a):

should be 55.6

should be 5

$$(100)/15 = (x)/10 + (100-x)$$

Solving for x, we get x = 103.7

(Part B)

If processor A has a higher clock rate than processor B, and processor A also has a higher MIPS rating than processor B, explain whether processor A will always execute faster than processor B. Suppose that there are two implementations of the same instruction set architecture. Machine A has a clock cycle time of 20ns and an effective CPI of 1.5 for some program, and machine B has a clock cycle time of 15ns and an effective CPI of 1.0 for the same program. Which machine is faster for this program, and by how much?

The CPU Time is given by the equation:

$$\text{CPU Time} = \text{Instruction count} * \text{CPI} * \text{Clock cycle Time}$$

MIPS rating is defined by:

$$\text{MIPS} = (\text{Clock Rate})/(\text{CPI} * 10^6)$$

For machines A and B:

$$(\text{CPUTime})_A = (\text{Instruction count})_A * (\text{CPI})_A * (\text{Clock cycle Time})_A$$
$$(\text{CPUTime})_B = (\text{Instruction count})_B * (\text{CPI})_B * (\text{Clock cycle Time})_B$$
$$(\text{MIPS})_A = (\text{Clock Rate})_A/((\text{CPI})_A * 10^6)$$
$$(\text{MIPS})_B = (\text{Clock Rate})_B/((\text{CPI})_B * 10^6)$$

If clock rate of A is higher than that of B, and MIPS rating of A is higher than that of B,

$$(\text{MIPS})_A > (\text{MIPS})_B \quad \text{and} \quad (\text{Clock Rate})_A > (\text{Clock Rate})_B$$

From the above equations it follows that:

$$(\text{Clock Rate})_A / (\text{Clock Rate})_B > (\text{CPI})_A / (\text{CPI})_B$$
$$(\text{Clock Cycle Time})_B / (\text{Clock Cycle Time})_A > (\text{CPI})_A / (\text{CPI})_B$$

From this it emerges that if the instruction counts are the same, processor A will always execute faster than processor B.

Assuming instruction counts are the same,

$$(\text{CPUTime})_A = (I) * 1.5 * 20\text{ns} = (I)*30\text{ns}$$
$$(\text{CPUTime})_B = (I) * 1.0 * 15\text{ns} = (I)*15\text{ns}$$

Machine B is faster by twice as much as Machine A.

9. [5 points] Computer A has an overall CPI of 1.3 and can be run at a clock rate of 600MHz. Computer B has a CPI of 2.5 and can be run at a clock rate of 750 Mhz. We have a particular program we wish to run. When compiled for computer A, this program has exactly 100,000 instructions. How many instructions would the program need to have when compiled for Computer B, in order for the two computers to have exactly the same execution time for this program?

$(\text{CPUTime})_A = (\text{Instruction count})_A * (\text{CPI})_A * (\text{Clock cycle Time})_A$
$= (100{,}000)*(1.3)/(600*10^6)$ ns
$(\text{CPUTime})_B = (\text{Instruction count})_B * (\text{CPI})_B * (\text{Clock cycle Time})_B$
$= (I)_B*(2.5)/(750*10^6)$ ns
Since $(\text{CPUTime})_A = (\text{CPUTime})_{B,}$

we have to solve for $(I)_B$ and get 65000