Chapter 2 – Additional Notes

Immediate Operands

 Constant data specified in an instruction addi x22, x22, 4

Make the common case fast

- Small constants are common
- Immediate operand avoids a load instruction

RISC-V R-format Instructions

funct7	rs2	rs1	funct3	rd	opcode
7 bits	5 bits	5 bits	3 bits	5 bits	7 bits

Instruction fields

- opcode: operation code
- rd: destination register number
- funct3: 3-bit function code (additional opcode)
- rs1: the first source register number
- rs2: the second source register number
- funct7: 7-bit function code (additional opcode)

RV32I Architectural State

XLEN-1 0 XLEN-1

x0 / zero
x1
x2
х3
x4
х5
х6
х7
x8
х9
x10
x11
x12
x13
x14
x15

ALEN-1		U .
	x16	
	x17	
	x18	
	x19	
	x20	
	x21	
	x22	
	x23	
	x24	
	x25	
	x26	
	x27	
	x28	
	x29	
	x30	
	x31	
	рс	

RISC-V Register Usage Convention

Register	ABI Name	Description	Saver
х0	zero	Hard-wired zero	_
x1	ra	Return address	Caller
x2	sp	Stack pointer	Callee
хЗ	gp	Global pointer	_
x4	tp	Thread pointer	_
x5-7	t0-2	Temporaries	Caller
x8	s0/fp	Saved register/frame pointer	Callee
х9	s1	Saved register	Callee
x10-11	a0-1	Function arguments/return values	Caller
x12-17	a2-7	Function arguments	Caller
x18-27	s2-11	Saved registers	Callee
x28-31	t3-6	Temporaries	Caller

[from page 100, The RISC-V Instruction Set Manual]

RV32I Arithmetic and Logical Operations

	. [4.4	01	1	000	1	0010011	ADDI
	imm[11:	,	rs1	000	rd	0010011	ADDI
	$\operatorname{imm}[11:$	0]	rs1	010	rd	0010011	SLTI
	$\operatorname{imm}[11:$	0]	rs1	011	rd	0010011	SLTIU
	imm[11:	0]	rs1	100	rd	0010011	XORI
	imm[11:	0]	rs1	110	rd	0010011	ORI
	imm[11:	0]	rs1	111	rd	0010011	ANDI
	0000000	shamt	rs1	001	rd	0010011	SLLI
	0000000	shamt	rs1	101	rd	0010011	SRLI
	0100000	shamt	rs1	101	rd	0010011	SRAI
	0000000	rs2	rs1	000	rd	0110011	ADD
	0100000	rs2	rs1	000	rd	0110011	SUB
	0000000	rs2	rs1	001	rd	0110011	SLL
	0000000	rs2	rs1	010	rd	0110011	SLT
	0000000	rs2	rs1	011	rd	0110011	SLTU
	0000000	rs2	rs1	100	rd	0110011	XOR
	0000000	rs2	rs1	101	rd	0110011	SRL
	0100000	rs2	rs1	101	rd	0110011	SRA
	0000000	rs2	rs1	110	rd	0110011	OR
	0000000	rs2	rs1	111	rd	0110011	AND
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Load/Store Operations

Both need two registers and a 12-bit immediate

imm[11:0]		rs1	011	rd	0000011	LD
imm[11:5]	rs2	rs1	011	imm[4:0]	0100011	SD

Memory Operand Example

imm[11:0]		rs1	011	rd	0000011	LD
imm[11:5]	rs2	rs1	011	imm[4:0]	0100011	SD

• C code:

$$A[12] = h + A[8];$$

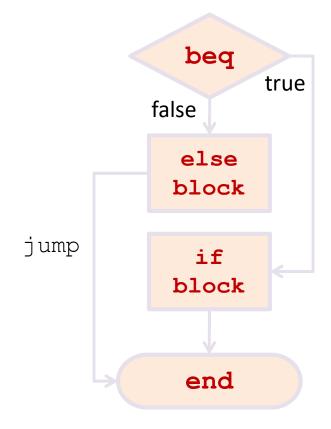
- h in x21, base address of A in x22
- Compiled RISC-V code:
 - Index 8 requires offset of 64
 - 8 bytes per doubleword

Control flow in assembly

- Not all programs follow a linear set of instructions.
 - Some operations require the code to branch to one section of code or another (if/else).
 - Some require the code to jump back and repeat a section of code again (for/while).
- For this, we have labels on the left-hand side that indicate the points that the program flow might need to jump to.
 - References to these points in the assembly code are resolved at compile time to offset values for the program counter.

A trick with if statements

 Use flow charts to help you sort out the control flow of the code:



Lab D – C code

```
main.c
   1 /* C program to swap bytes/words of integer number. */
   2 #include <stdio.h>
      int main()
   6
          unsigned int data=0xAABB1234;
          printf("\ndata before swapping : %04X",data);
   8
          data= ((data<<8)&0xff00) | ((data>>8)&0x00ff);
  10
  11
          printf("\ndata after swapping : %04X",data);
  12
 13
          return 0;
  14
  15
```

But what if I have nested function calls?

```
(1) jal FUNCTION X
   sum = 3;
                           ra set to PC of the next instruction.
   function X(sum)
   sum += 5;
                                      (2) Execution continues
                                      from here
void function X (int sum) {
                                                      (4) Execution continues
                                                      from here
                           (3)
   //do something
                           jal FUNCTION_Y
   function Y();
                                              void function Y ()
                           ra set to PC of next
                           instr
   return;
                                                  //do something
                                                  recurn;
                                                               (5) jr ra
                               Which $ra?
                 (6) Execut
                              No way back! ⊗
```

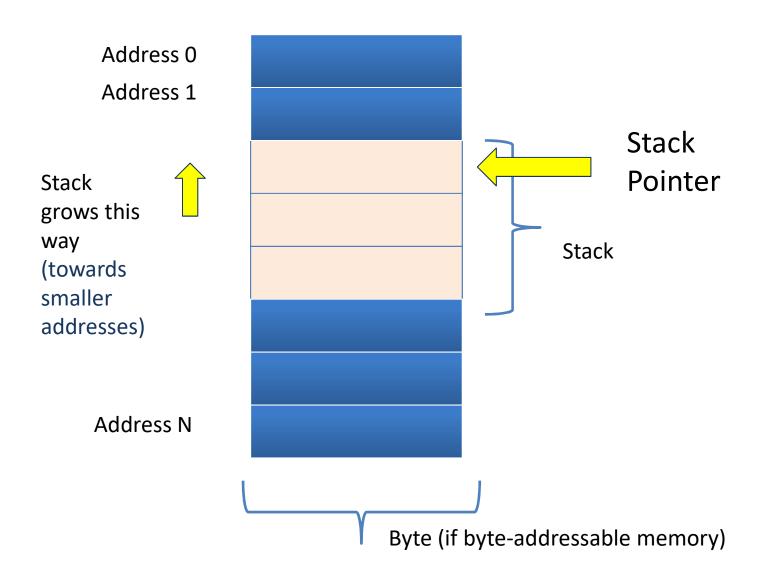
The stack to the rescue!

- Store ra in the stack.
 - Different versions of ra will exist in the stack
- We can also use the stack to store*:
 - Function arguments
 - Function return values
 - And also to maintain register values (more on this later).

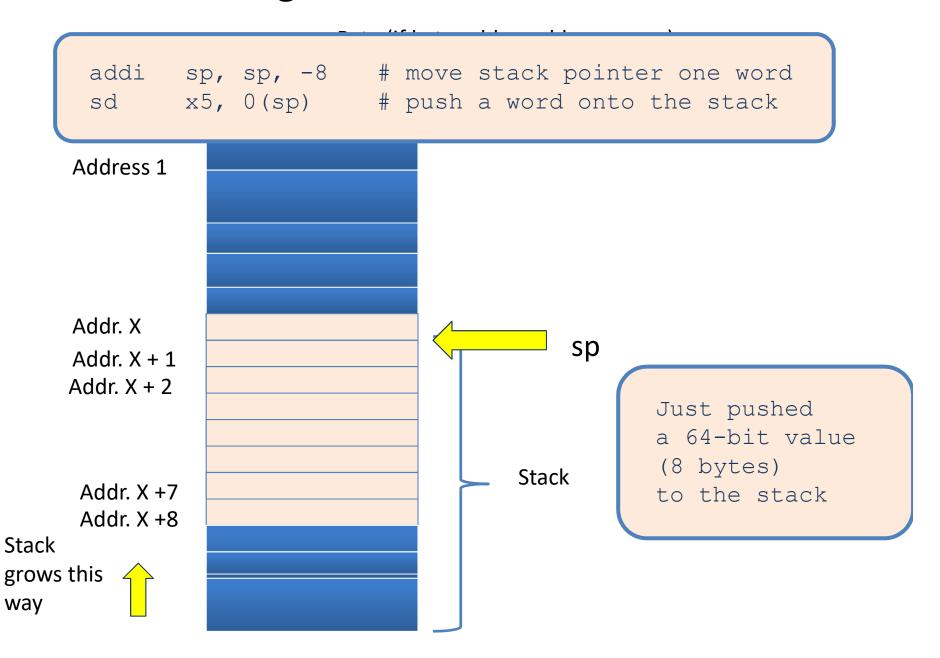
• E.g., if there are more than 4 arguments.

^{*} As mentioned before there are some predefined registers used for the function arguments and return values; the stack is used if this number is exceeded.

The Stack



Pushing Values to the stack - After



Stack Usage

- Pushing something onto the stack
 - Allocate space by <u>decrementing</u> the stack pointer by the appropriate number of bytes.
 - Do a store (or multiple stores as needed).
- Popping something from the stack:
 - Do a load (or multiple loads as needed)
 - De-allocate space by incrementing the stack pointer by the appropriate number of bytes.

More advice on using the stack

- Any space you allocate on the stack, you should later deallocate.
- You should pop the items in the same order as you push them.
 - It might help to draw out an image of how your stack will look like.
- When pushing more than one item onto the stack, you can
 :
 - Either allocate all the space in the beginning
 - Or allocate space as you go.
 - Same for popping.

Let's do an example.

Figure shows stack *after* the push.

• Push contents of registers x2 and x3onto the stack.

addi sp, sp, -16 sd x2, 0(sp) sd x3, 8(sp)

Address X+1

Address X

sp

 Restore stack values pushed to registers x2 and x3.

```
1d \times 2, 0(sp)
ld x3, 8(sp)
addi sp, sp, 16
```

Contents ofregister x2

Contents

register