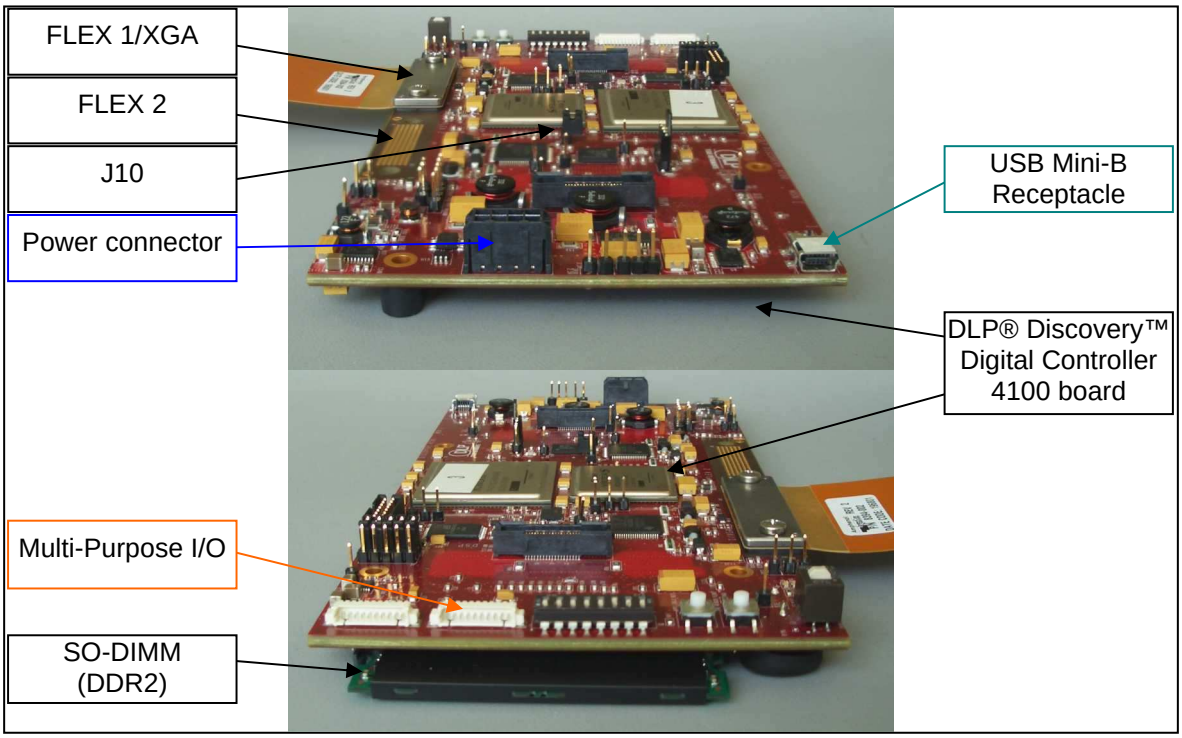


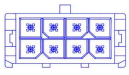
External Connections and Ports

The ALP-4.1 *high-speed* hardware consists of the DLP® Discovery™ Digital Controller 4100 board (DCB4100) extended by a memory module and a battery supported FPGA key. This document provides details about the electrical interfaces.



Connectors

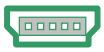
On the DLP® Discovery™ Board, an 8-pin Molex DC power jack is provided to bring power in from a power supply unit.



Power connector

This is a Molex micro fit 3.0 dual row header, part number 43045-0812. It mates with micro fit 3.0 receptacle 43025-08xx.

Pin Number	Signal Name	Power Consumption
1 – 4 (lower on drawing)	GND	-
5 – 8	5 V	6 A



USB Mini-B connector

This is the connector for USB connection to the PC. Use the supplied USB cable to connect the board.

Pin Number	Signal Name
1 (left on photo)	USB VCC
2	USB D–
3	USB D+
4	not connected
5	GND

Multi-Purpose I/O (Synchronization) connector

The trigger connector of ALP-4.1 *high-speed* is connector J6 on the DCB4100. It is a Molex header, part number 53261-1071. It mates with Molex part number 51021-**10**00. Use crimp contacts 50079-8000.

Two pins are connected to the 2.5 V power regulator and ground. The other eight pins are logic input and output signals with 2.5 V LVCMOS IO standard. Input and In/Out pins have weak pull-ups. For details please consult the documentation of the Xilinx Virtex-5 FPGA: www.xilinx.com/support/documentation/data_sheets/ds202.pdf (Table 7: SelectIO DC Input and Output Levels and Table 3: DC Characteristics Over Recommended Operating Conditions). Drive strength is 2 mA.

Pin Number	Signal Name	Direction	Purpose
1 (left on photo)	2.5 V	—	Power
2	SPARE1	IN/OUT	
3	SPARE2	IN/OUT	
4	SPARE3	IN/OUT	
5	SPARE4	IN/OUT	
6	SPARE5	IN/OUT	
7	VD_IN	IN	Trigger Input
8	TRIGGER	OUT	Trigger Output
9	SPARE6	IN/OUT	
10	GND	—	Power

WARNING: This connector is directly connected to the FPGA. There is no over-voltage protection, debounce, nor similar circuitry in between.

NOTE: Higher input voltage is allowed only in conjunction with a series resistance. For 5 V we recommend a resistor of 2.2 kΩ. If deeper understanding is required, please consult the Virtex-5 Data Sheet (see above) and the Virtex-5 User Guide:
www.xilinx.com/support/documentation/user_guides/ug190.pdf
(Section 3.3V I/O Design Guidelines).

SO-DIMM Socket

A standard DDR2 SO-DIMM (small outline dual-inline memory module) is supplied with ALP-4.1 *high-speed*. Please always use the module specified and supplied by ViALUX. Always switch off the device before removal or insertion of the memory module.

FLEX 1/XGA, FLEX 2, and J10

When using an XGA DMD please connect FLEX 1 and open jumper J10. The 1080p DMD requires J10 being installed and both flex cables connected.

Always switch the device off before exchanging the DMD.

Mounting Instructions and Measures

To get measures of outline and holes of the DCB 4100, refer to drawings supplied in the DLP® Discovery™ Knowledge Base.

Never drill into a multi-layer board!

Please be aware that there is an on-board battery that supplies memory for FPGA encryption. Avoid short-circuits when mounting the board in order to not lose the encryption key.

The ALP system is designed to work in any mounting position. Good air circulation is recommended.