LAB 3

Overview

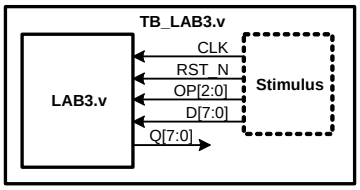
The goal of this project is to design a sequential logic circuit. In LAB3, you will be asked to construct both a simple sequential logic block (*LAB3.v*) and its corresponding testbench (*TB_LAB3.v*). Submit a ***report*** along with the modified ***LAB3.v*** and ***TB_LAB3.v*** files. Please follow the instructions below for more details.

Files

You have been provided with two files that need to be modified.

1. LAB3.v: The main module which operates sequentially.

2. TB_LAB3.v: A testbench file to validate your design



Design

1. 8-bit operator (LAB3.v)

When RST_N is low, the output (Q[7:0]) is always zero, regardless of the input (D[7:0]) or the control signal (OP[2:0]).

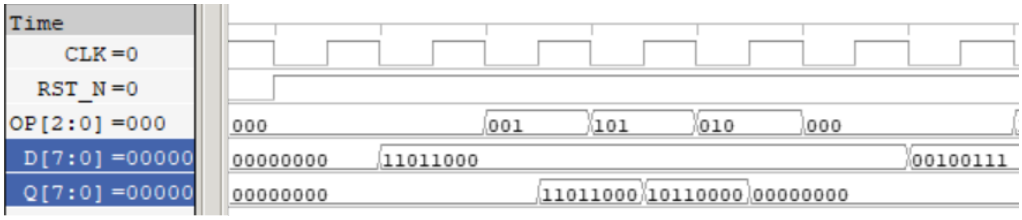
When RST_N is high, the output (Q[7:0]) is changed on the rising edge of the clock based on the control signal (OP[2:0]), as follows:

OP[2:0]	Operation	OP[2:0]	Operation
000	Hold (Q → Q)	100	Add (Q + D → Q)
001	Load (D → Q)	101	Left shift (Q ≪ 1 → Q)
010	Synchronous reset (0 → Q)	110	Count the number of 1 (# of D → Q)
011	1's complement (-Q → Q)	111	*"Your custom operation"*

2. Testbench (TB_LAB3.v)

- The testbench should verify the functionality of RST_N (asynchronous reset).
- It should include all eight operations (OP[2:0]).
- You can manually check the validity of the output using waveform analysis, but you should compare the results with your hand calculation on your report.

This is the example waveform.



Simulation Output & Grading

The total score is 25 pts. 20 pts are allocated for your design, while an additional 5 pts are for your extra writing.

- Please attach your main code along with the waveforms and explain them in your report.
- Each operation and the asynchronous reset are worth 2 points respectively, while your custom operation (OP = 111) is worth 4 points. (Note that operations that are not verified will not receive any points, even if your LAB3.v design is perfect.)
- It is recommended to emphasize any significant points or observations in your report, such as design issues or noteworthy aspects of your implementation. This will help in demonstrating your understanding and analysis of the project. (it is worth additional 5 pts.)

If you have any question, please contact to TA Hansol Jeong (1sol_jeong@kaist.ac.kr).