[EE303B] Digital System Design Due Date : 12/06 23:59

Overview

This project's purpose is to understand the combinational logic. In Lab2, you should implement an decoder logic by using Verilog language. You should submit your decoder.v code through KLMS until the due date. This project is to design 7 segment decoder as below figure.

Files

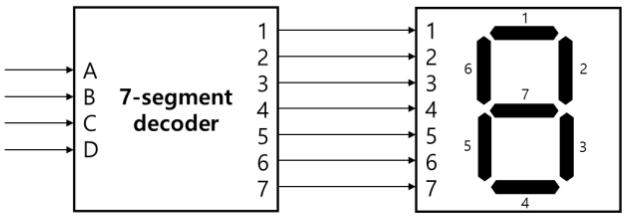
You are given two files and you only need to change decoder.v. You do not need to change TB.v.

1. decoder.v : This is where you implement the decoder module

2. TB.v : A testbench file which you can test and grade your decoder module.

Decoder Design

This project is to design 7 segment decoder as below figure.



Input (0~9)				Output to 7-segment (0: led off, 1: led on)							Decimal number
A	B	C	D	1	2	3	4	5	6	7	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9

Simulation Output & Grading

Testbench code tests 10 cases (number 0~9). Each case is 1 point and full score is 10 points. If you pass the all the test is TB, you can have the same massage below. If you have any question, please contact to TA Seunghee Han (shhan1755@kaist.ac.kr).

```
Case 1 is passed
Case 2 is passed
Case 3 is passed
Case 4 is passed
Case 5 is passed
Case 6 is passed
Case 7 is passed
Case 8 is passed
Case 9 is passed
Total score: 10
```