



CGT Board Level Tester Daughter Card Software Design Specification

Revision History

Revision	Date	Author	Description
00.01	12/12/95	Mike Hammersley x2594	Initial Draft

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1.0 CT25CWi Daughter Card Software Design Specification

1.1 Purpose

This purpose of this document is to outline and describe the software implementation for the CR25CWi board level test utilizing a CGT as the host and a daughter card as the DUT interface.

1.2 Scope

This document is applicable only to the CT25CWi product line.

1.3 Test Plan

1. Check for correct STEALTH boot-up.
2. Check all power levels and battery power control signals (-EPS, -FSK.EN, LOWBATT).
3. Check off-hook DC resistance.
4. Check receive gain of the speech network.
5. Check transmit gain of the speech network.
6. Check the key matrix and DTMF gain of the speech network & adjust DTMF trim pot.
7. Check the ring detect circuit.
8. Check the Line-in-use circuit.
9. Check the dial tone detection circuit.
10. Check the FSK gain circuit and adjust the FSK potentiometer.
11. Calibrate and sweep the 2130 and 2750 filter stages.
12. Check the CAS tone detection circuit.

1.4 Test Descriptions

The following is a list of the individual tests that will be performed by the CGT and a description of each test.

1.4.1 Test #1: STEALTH Boot-up test.

The tester turns on power to the DUT and waits for a Reset pulse from the STEALTH processor. If the Reset pulse does not occur within approximately 400mSec, the tester times out and reports a STEALTH boot-up error on the tester front panel display.

1.4.2 Test #2: Power check.

The tester measures the power supply voltages when AC adapter is applied and again when battery voltage applied. The test also checks the low battery circuit, the -EPS circuit and the -FSK.EN circuit.

1. Apply +9.0 Vdc to the AC adapter (+AC) input.
2. Check for -EPS to be active low.
3. Check if VADPT, VDD, VCD,VCC, VDDX, +VCCA, +VCCAX, VMID, VMID2 power levels are within spec.
4. Turn off AC adapter power and apply +9.0 Vdc battery power.
5. Check for -EPS to be inactive high.
6. Set -FSK.EN to the active low state.
7. Check if VCC, VCD, +VCCAX power are within spec.
8. Turn off all power to DUT, set -FSK.EN to inactive high state and go off-hook.
9. Check if VCD is within spec during POTs mode.
10. Turn on AC adapter power and apply +4.0 Vdc battery power.
11. Check if the LOWBATT signal is active high.
12. If an error occurs, the tester logs the error, clears all active signals and exits the test.

1.4.3 Test #3: Off-hook DC Resistance test.

This test measures the DC resistance across Tip & Ring in the off-hook position.

1. Go to the Off-hook state.
2. Determine the line current and save.
3. Check if the voltage measured across Tip & Ring is within the required limit.
4. Reverse the Tip & Ring input and repeat step #2.
5. Go to the on-hook state.
6. Check if the voltage measured across Tip & Ring is within the required limit.
7. If an error occurs, the tester logs the error, clears all active signals and exits the test.

1.4.4 Test #4: Handset Receive Gain test

This test checks the RxD gain of the speech network in the off-hook handset mode with the line current limited to 20 mA. The receive gain is checked by applying three different frequencies with a 1Vp-p signal level across Tip & Ring. The test is repeated with the line current set to 90mA.

1. Go to the off-hook state.
2. Apply a 500 Hz, 1.0 Vp-p signal across Tip & Ring.
3. Measure the receive gain of the speech network across a 300 ohm load and see if within spec.
4. Repeat steps 2 and 3 for signals at 1200 Hz and 2000 Hz.
5. If an error occurs, the tester logs the error, clears all active signals and exits the test.

1.4.5 Test #5: Handset Transmit Gain test.

This test checks the TxD gain of the speech network in the off-hook handset mode with the line current limited to 20 mA. The transmit gain is checked by applying 3 different frequencies with a 10 mVrms signal level across the MIC+ and MIC- inputs. The test is repeated with the line current set to 90 mA.

1. Go to the off-hook state.
2. Apply a 500 Hz, 10.0 mVrms signal across the microphone input of the Speech Network.
3. Measure the transmit gain across Tip and Ring.
4. Repeat steps 2 and 3 for signals at 1200 Hz and 2000 Hz.
5. If an error occurs, the tester logs the error, clears all active signals and exits the test.

1.4.6 Test #6: DTMF Gain test and key matrix test

This test checks the key matrix and the DTMF gain of the speech network with the line current limited to 20 mA in the off-hook mode. The test is repeated with the line current set to 90mA.

1. Go to the on-hook mode.
2. Close the first DTMF key.
3. The tester waits for the STEALTH to recognize the key by monitoring the serial output line from the STEALTH.
4. Send a dial key command to the STEALTH.
5. Measure the DTMF gain of the speech network.
6. Repeat steps 2 thru 5 for all 12 DTMF keys.
7. Set the CASDET signal active high.
8. Send a DTMF 'D' row tone command to the STEALTH.
9. Adjust the DTMF trim pot to the mid range.
10. Send a DTMF 'D' column tone command to the STEALTH.
11. Measure the gain difference, should be within +/- 2db.
12. Repeats steps 8 thru 11 as needed.

13. If an error occurs, the tester logs the error, clears all active signals and exits the test.

1.4.7 Test #7: Ring test.

This test checks the ring detect circuitry.

1. Go to the on-hook state.
2. Check the -RING signal, should be in the inactive high state. Exit the test if stuck low.
3. Apply a 20 Hz, 40Vrms signal across Tip and Ring.
4. Check the -RING signal, it should be in the active low state.
5. Check if the piezo driver output is within the specified limits.
6. If an error occurs, the tester logs the error, clears all active signals and exits the test.

1.4.8 Test #8: LIU Threshold test

This test checks the Line-in-use thresholds of the LIU detection circuit.

1. Set nominal line voltage = 48 Vdc.
2. Check the -LIU signal, should be in the inactive high state, go to step 5.
3. While monitoring -LIU, check the threshold going from low voltage to high voltage.
4. While monitoring -LIU, check the threshold going from high voltage to low voltage.
5. If an error occurs, the tester logs the error, clears all active signals and exits the test.

1.4.9 Test #9: Dial Tone Detection Test

This test checks the dial tone detection circuit by applying a 330/440 Hz dual tone signal across Tip & Ring with a 100 milli-second on and a 100 milli-second off cycle time.

1. Check the DIAL.TONE signal, should be in the inactive low state. If not, go to step 4.
2. Apply a 330/440 Hz, 1.0 Vp-p signal across Tip & Ring.
3. The tester monitors the DIAL.TONE signal which should be active high in the presence of a dial tone signal and inactive low with no signal present.
4. If an error occurs, the tester logs the error, clears all active signals and exits the test.

1.4.10 Test #9: FSK Gain and Calibration.

This test checks the gain of the FSK circuit and checks the operation of the XR2211 I.C. After the circuit is tested, the operator is then prompted to adjust the FSK Pot for a 50% duty cycle as indicated by the fixture front panel adjustment LEDs. The test sequence is as follows:

1. Checks the -CD signal, should be in the inactive high state in the absence of FSK data.
2. Input a 1200/2200 Hz, 30mVrms signal across Tip & Ring.
3. Check the -CD signal, should be in the active low state in the presence of FSK data.
4. Check if the gain of the FSK signal is within the spec limit.
5. Check if the gain of the TONE.OUT signal is within the spec limit.
6. If an error occurs, the tester logs the error, clears all active signals and exits the test.
7. The operator adjusts the pot (R75) on the DUT until the green OK LED on the test fixture front panel turns on. If the adjustment fails, the operator must note down this failure.

1.4.11 Test #10: Tuning of 2130 first filter stage

This is a calibration test whereby the tester will measure the output of the first stage of the 2130 filter and provide feedback to the operator to enable the operator to adjust the trim pot and calibrate the first filter stage. A set of three LEDs on the front panel of the mechanical fixture will provide the visual feedback whereby the operator will adjust the trim pot until the meter is peaked. If the operator cannot peak the meter, the operator must then note down the failure.

1.4.12 Test #11: Tuning of 2130 second filter stage

This is a calibration test whereby the tester will measure the output of the second stage of the 2130 filter and provide feedback to the operator to enable the operator to adjust the trim pot and calibrate the second filter stage. A set of three LEDs on the front panel of the mechanical fixture will provide the visual feedback whereby the operator will adjust the trim pot until the meter is peaked. If the operator cannot peak the meter, the operator must then note down the failure.

1.4.13 Test #12: Tuning of 2750 filter stage

This is a calibration test whereby the tester will measure the output of the stage of the 2750 filter and provide feedback to the operator to enable the operator to adjust the trim pot and calibrate the 2750 filter stage. A set of three LEDs analog meter on the front panel of the mechanical fixture will provide the visual feedback whereby the operator will adjust the trim pot until the meter is peaked. If the operator cannot peak the meter, the operator must then note down the failure.

1.4.14 Test #13: Frequency Sweep 2130 Filter Test

This test will frequency sweep the 2130 filter for proper frequency response at varying amplitudes and frequencies. Seven different frequency and amplitude combinations are used. The output of the filter is a digitized square wave of the input frequency when the frequency is in the pass band of the filter. Otherwise, little or no output should be emitted by the filter outside the pass band.

The filter output of the 2130 filter stages is received by the tester input capture register. The incoming frequency is averaged and verified against what the appropriate frequency should be for the provided stimulus.

1.4.15 Test #14: Frequency Sweep 2750 Filter Test

This test will frequency sweep the 2750 filter for proper frequency response at varying amplitudes and frequencies. Seven different frequency and amplitude combinations are used. The output of the filter is a digitized square wave of the input frequency when the frequency is in the pass band of the filter. Otherwise, little or no output should be emitted by the filter outside the pass band.

The filter output of the 2750 filter stage is received by the tester input capture register. The incoming frequency is averaged and verified against what the appropriate frequency should be for the provided stimulus.

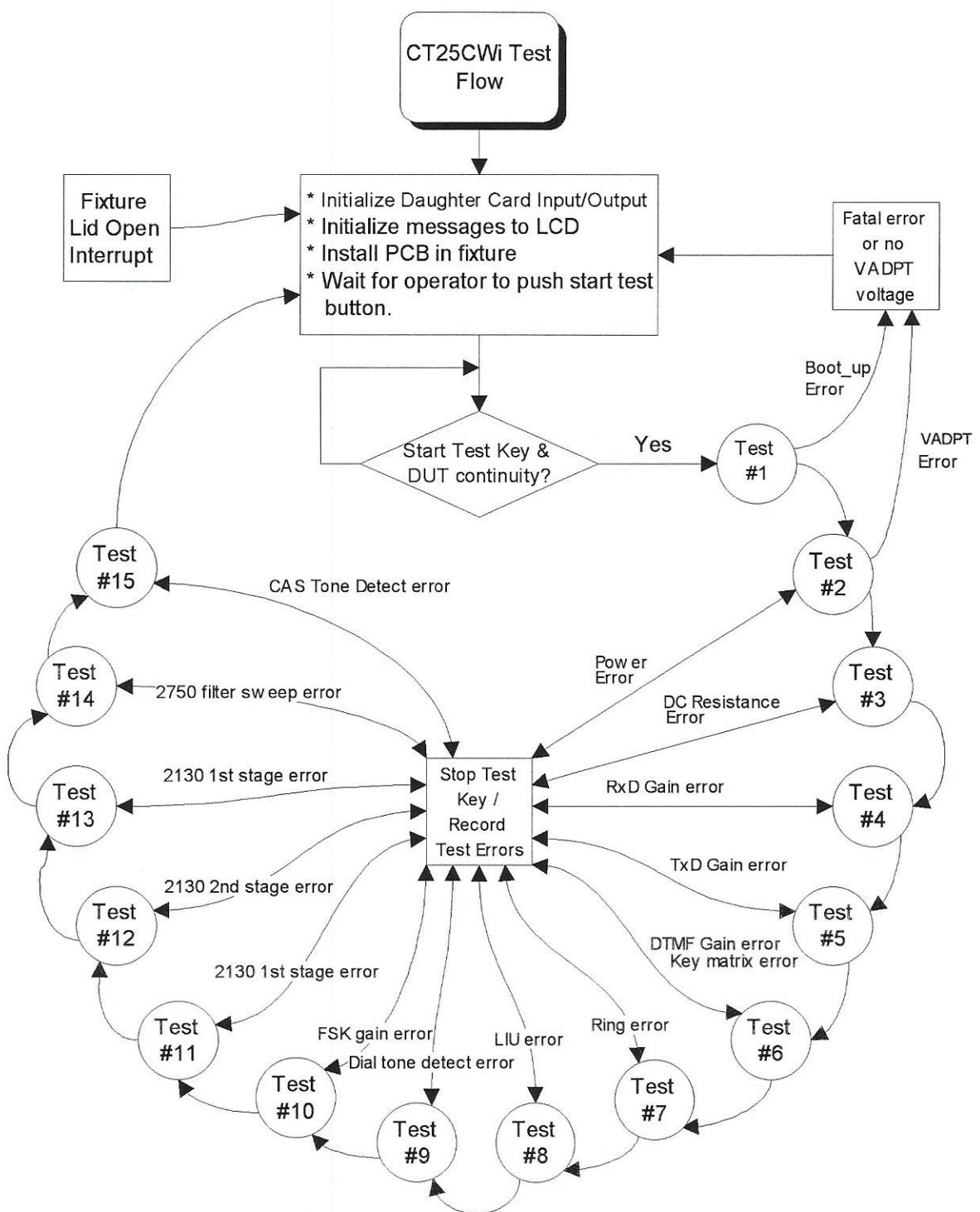
1.4.16 Test #15: CAS Tone Detection Test

This test generates 80 milli-seconds of CAS tone and waits for the tone processor to assert the -CASDET signal. The tester monitors the -CASDET signal which should go to the active low state. If the -CASDET does not get asserted, the tester then flags an error and exits the test.

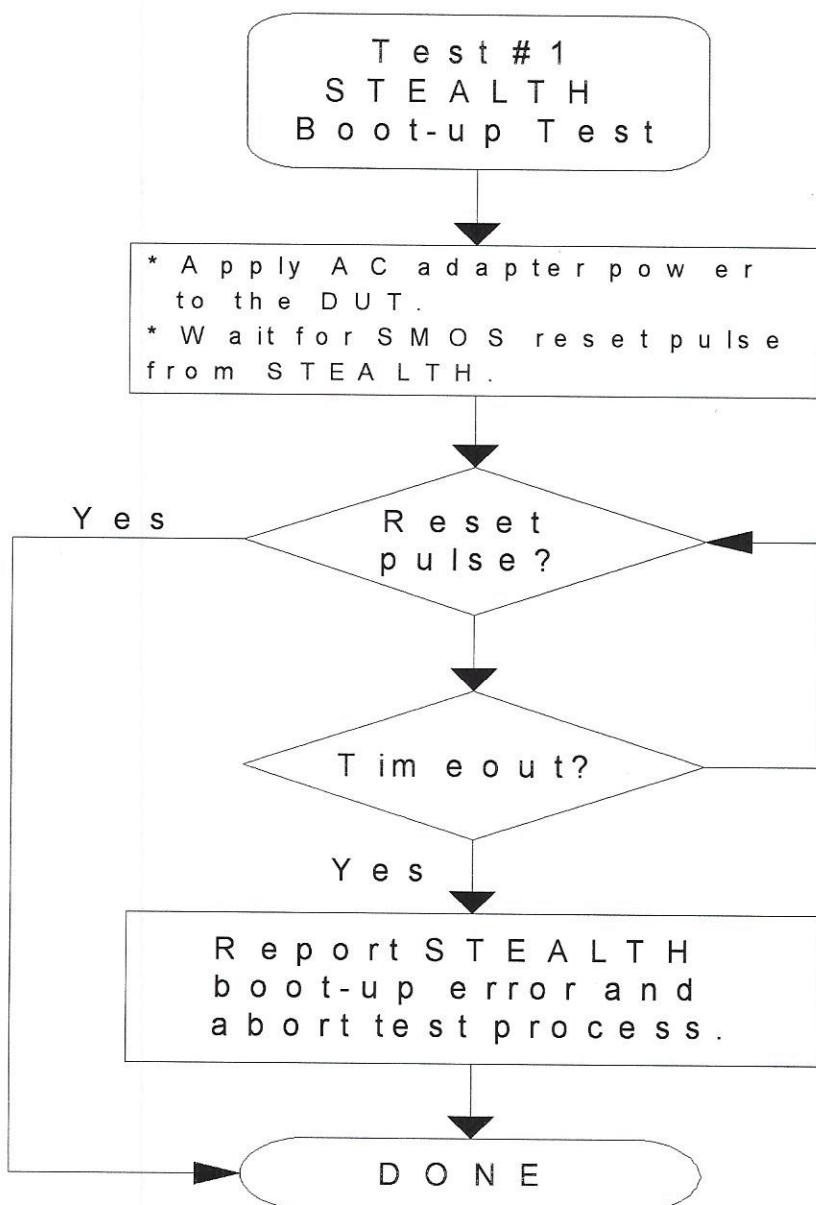
1.5 Software Flow Diagrams

The following diagrams diagram the flow of the CT25CWi test software including the Daughter card initialization software and the individual test software. The flow diagrams will not include any of the main CGT software, the only CGT software that will be diagrammed will be what is needed by the application software.

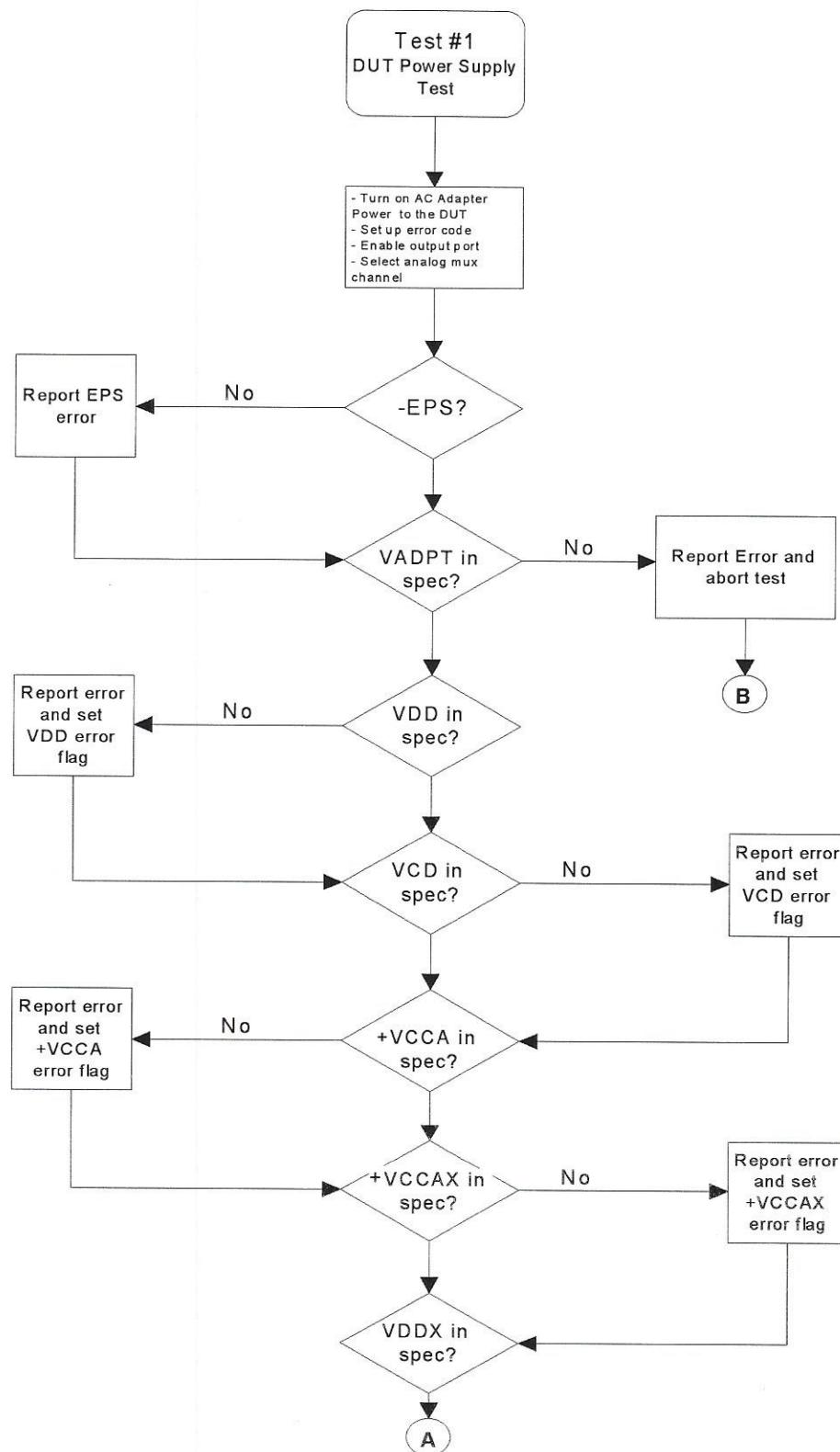
1.5.1 Test Process Flow Diagram

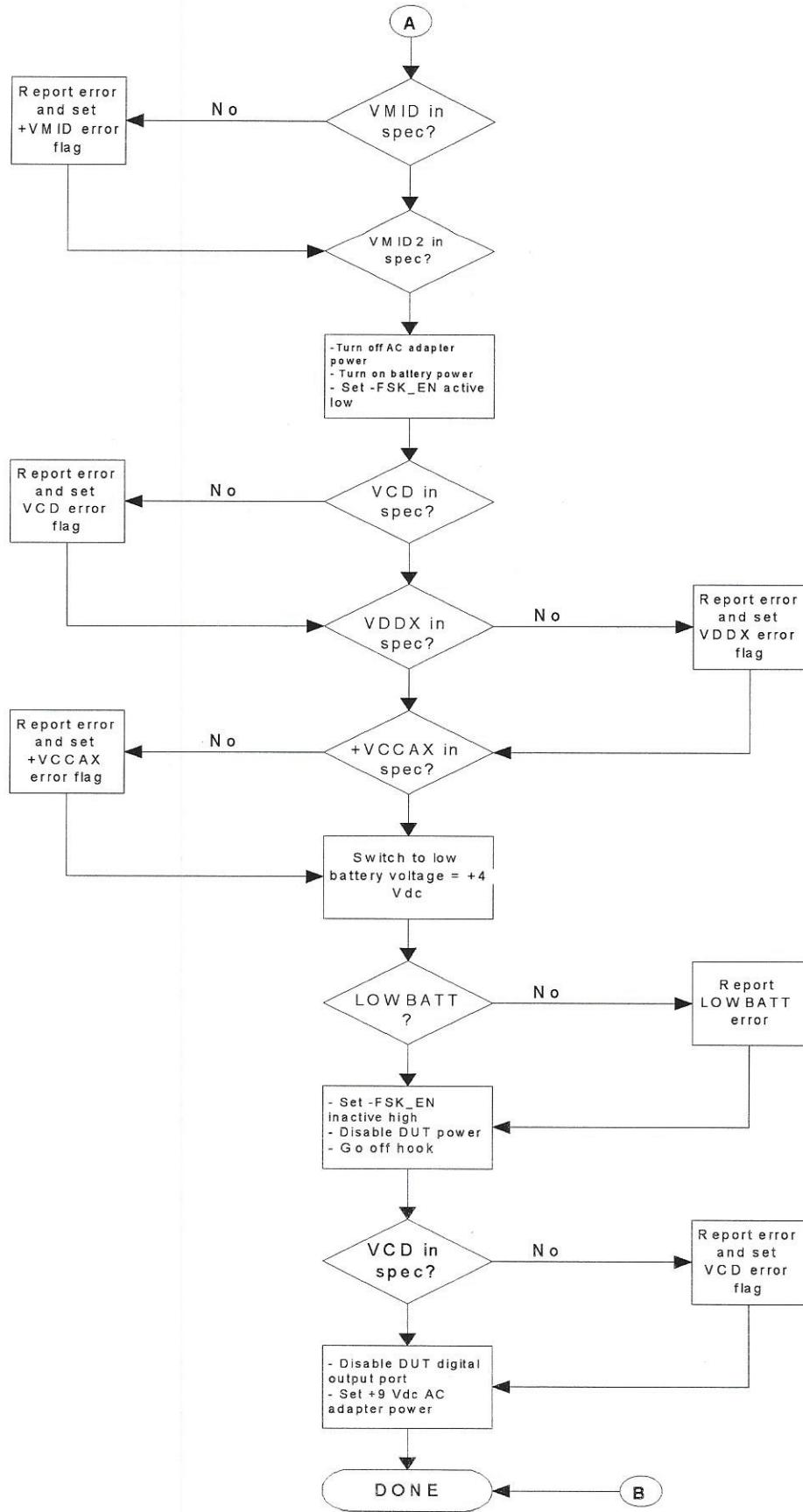


1.5.2 STEALTH Boot-up Test Flow Diagram

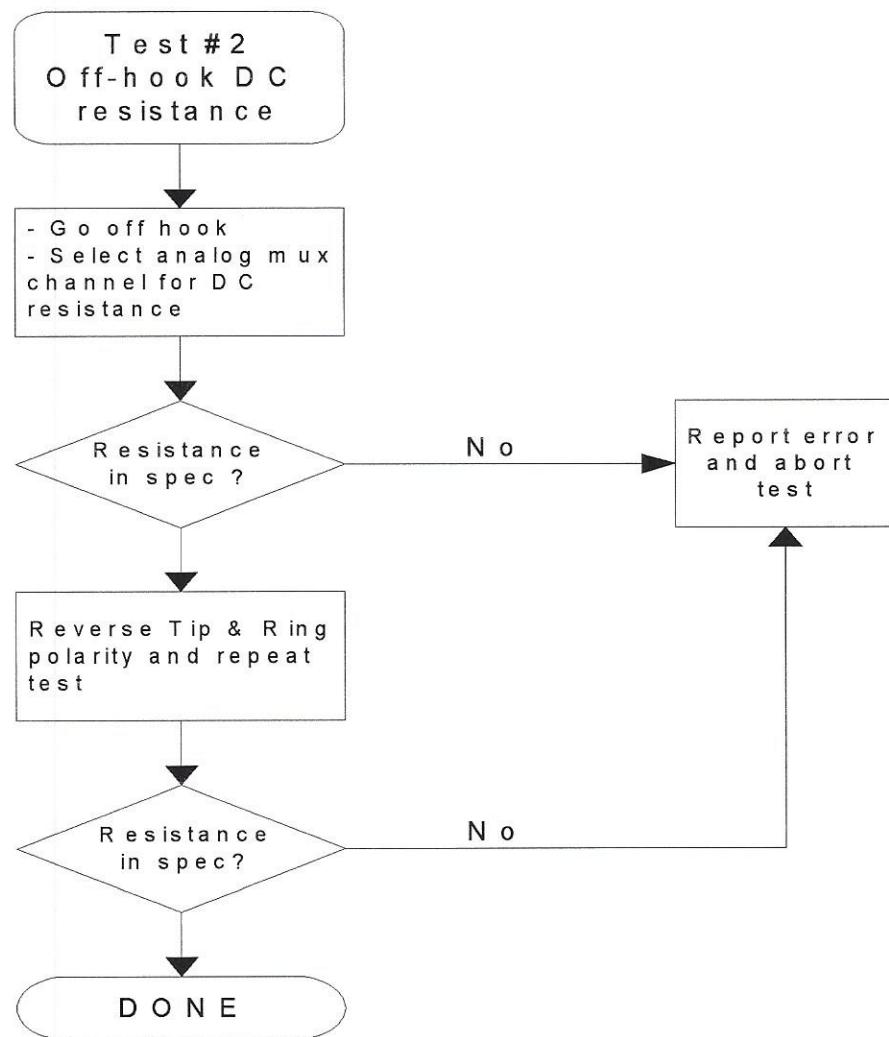


1.5.3 Power Supply Test Flow Diagram

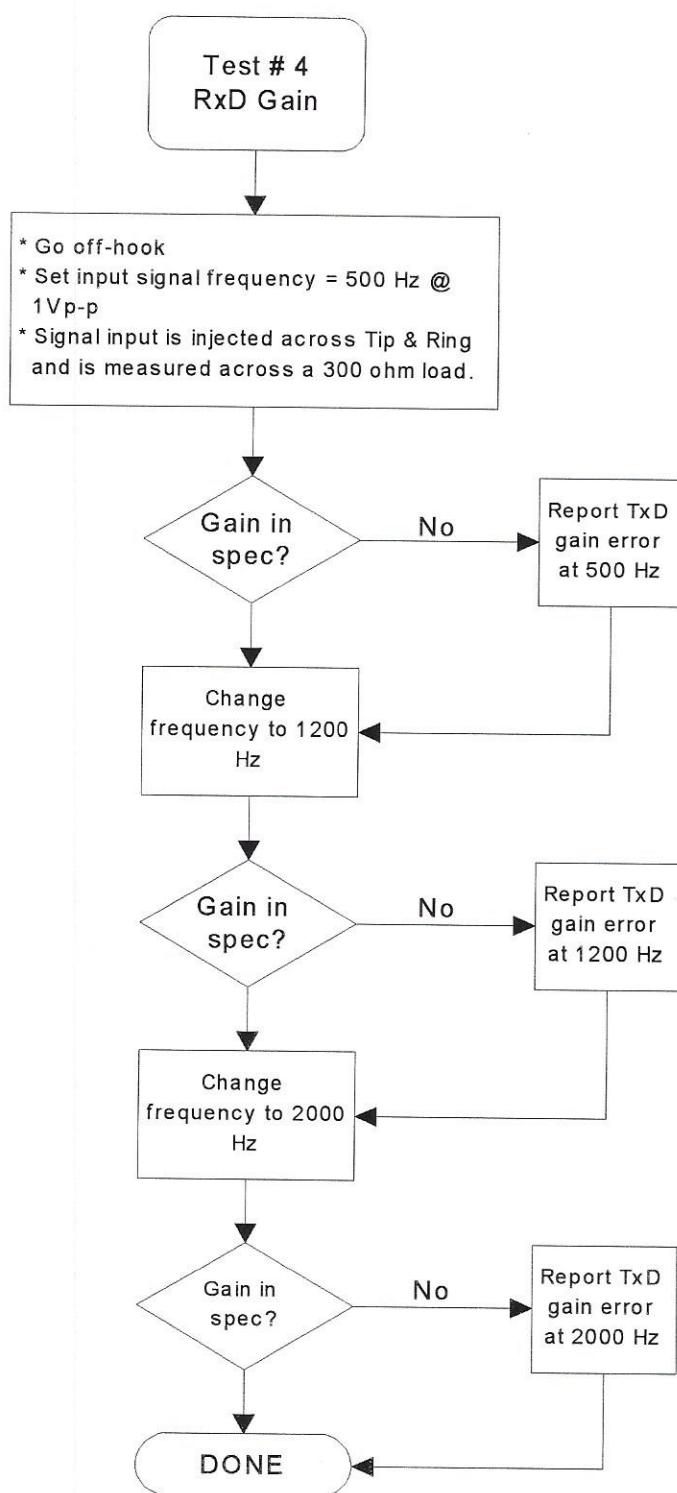




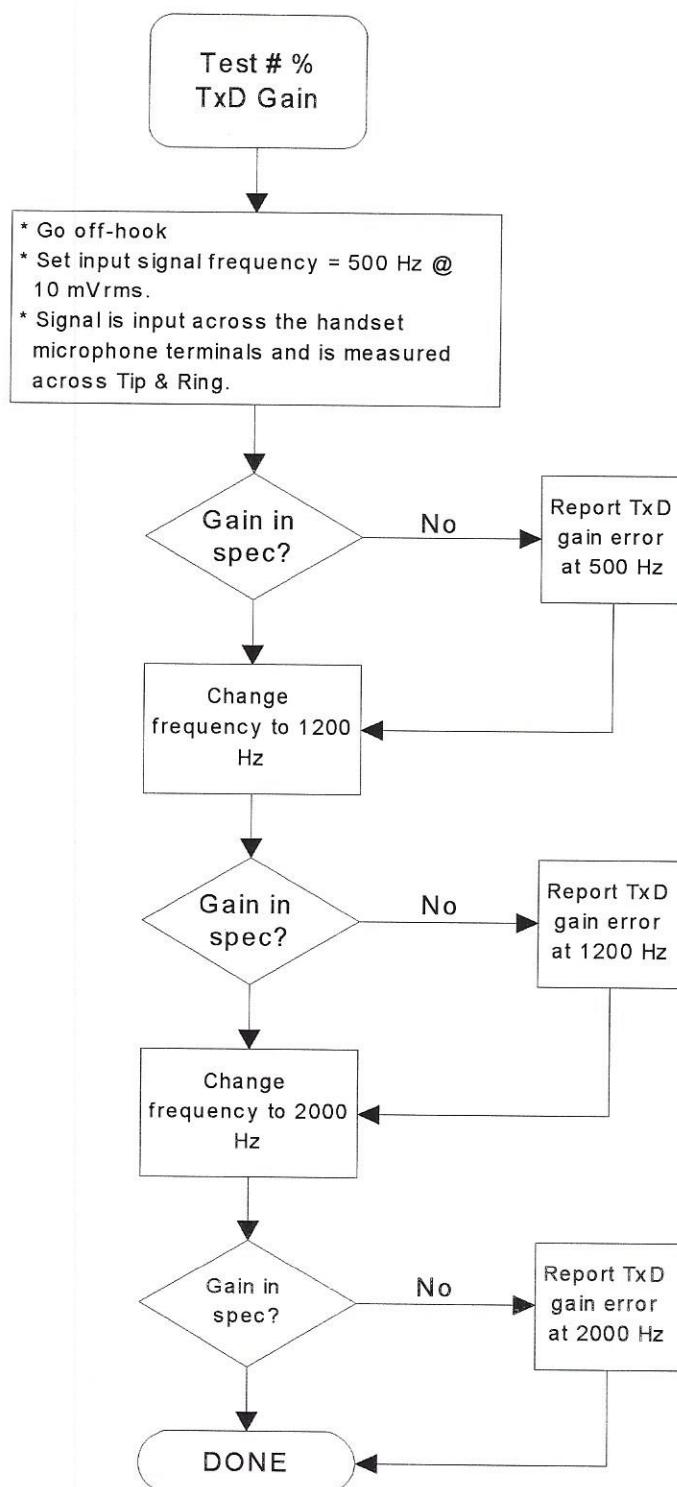
1.5.4 DC On-hook / Off-hook Test Flow Diagram



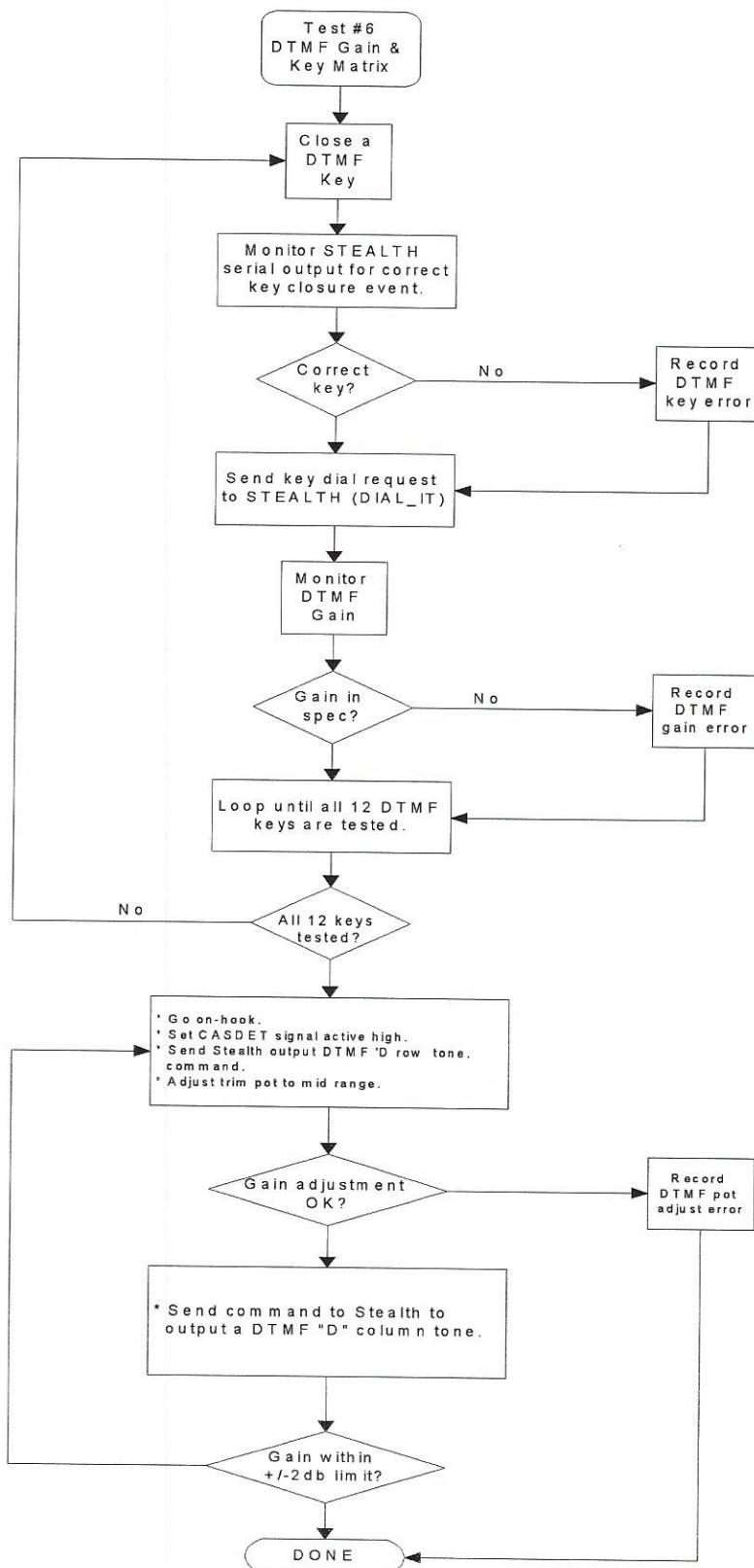
1.5.5 RxD Handset Gain Test Flow Diagram



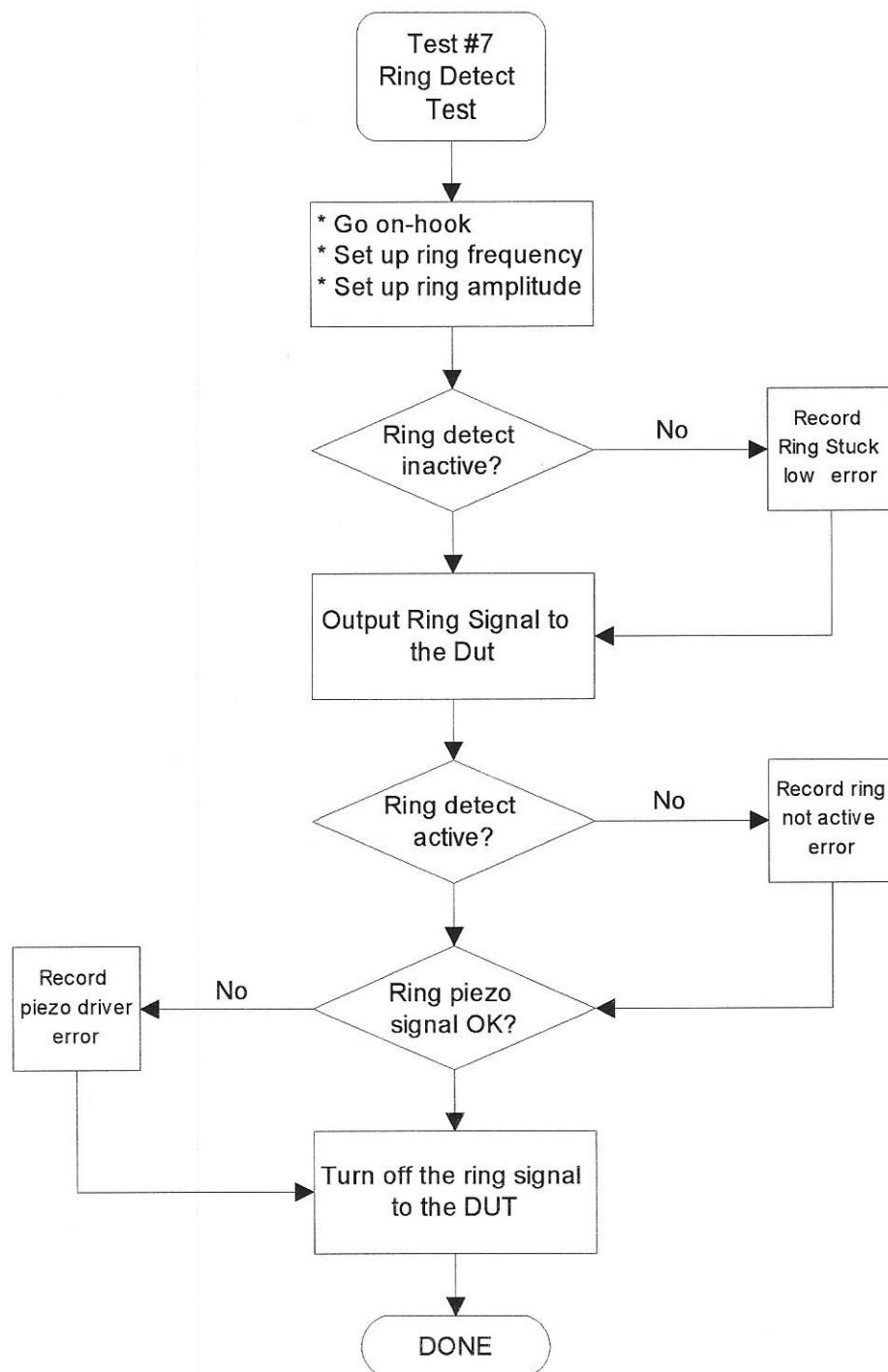
1.5.6 TxD Handset Gain Test Flow Diagram



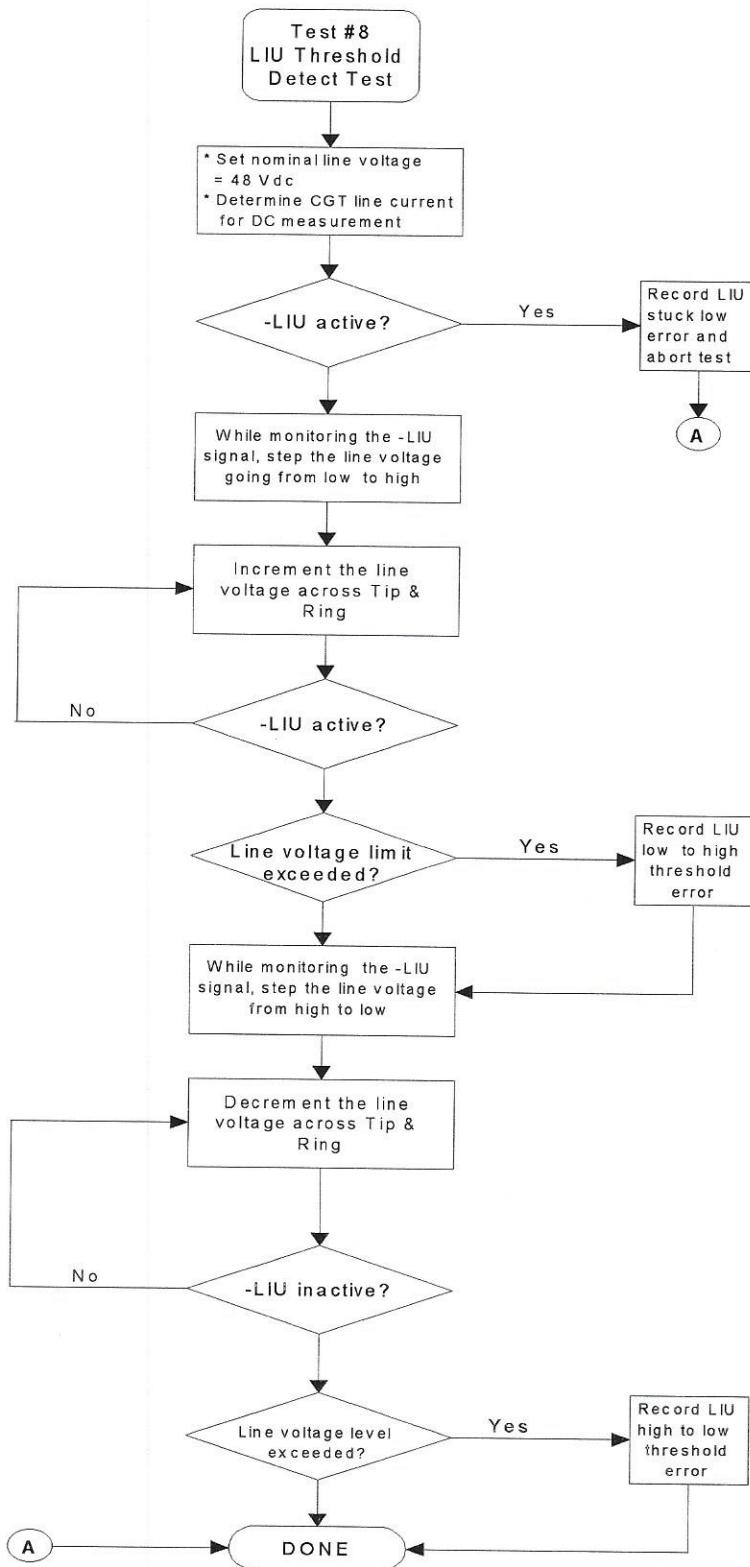
1.5.7 DTMF Gain Test Flow Diagram



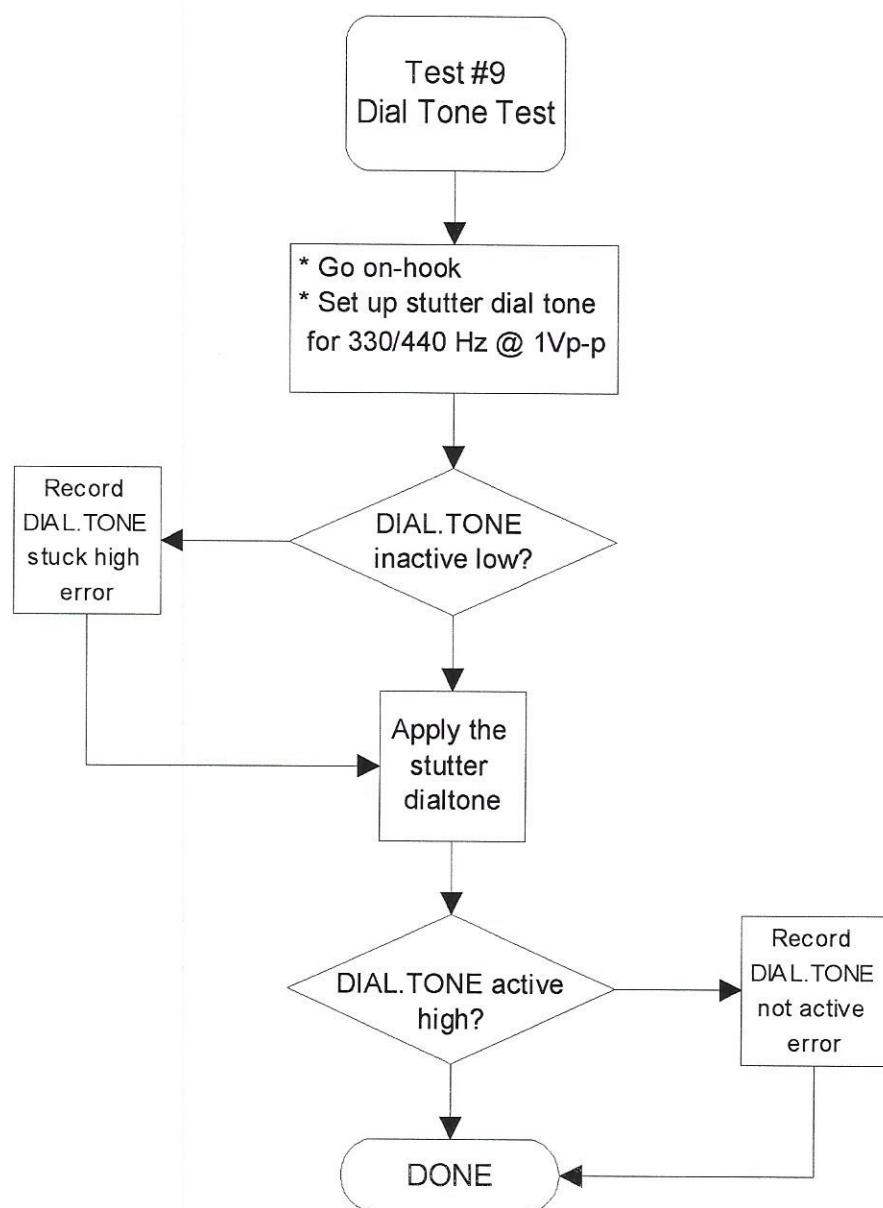
1.5.8 Ring Detect and Ring Piezo Driver Test Flow Diagram



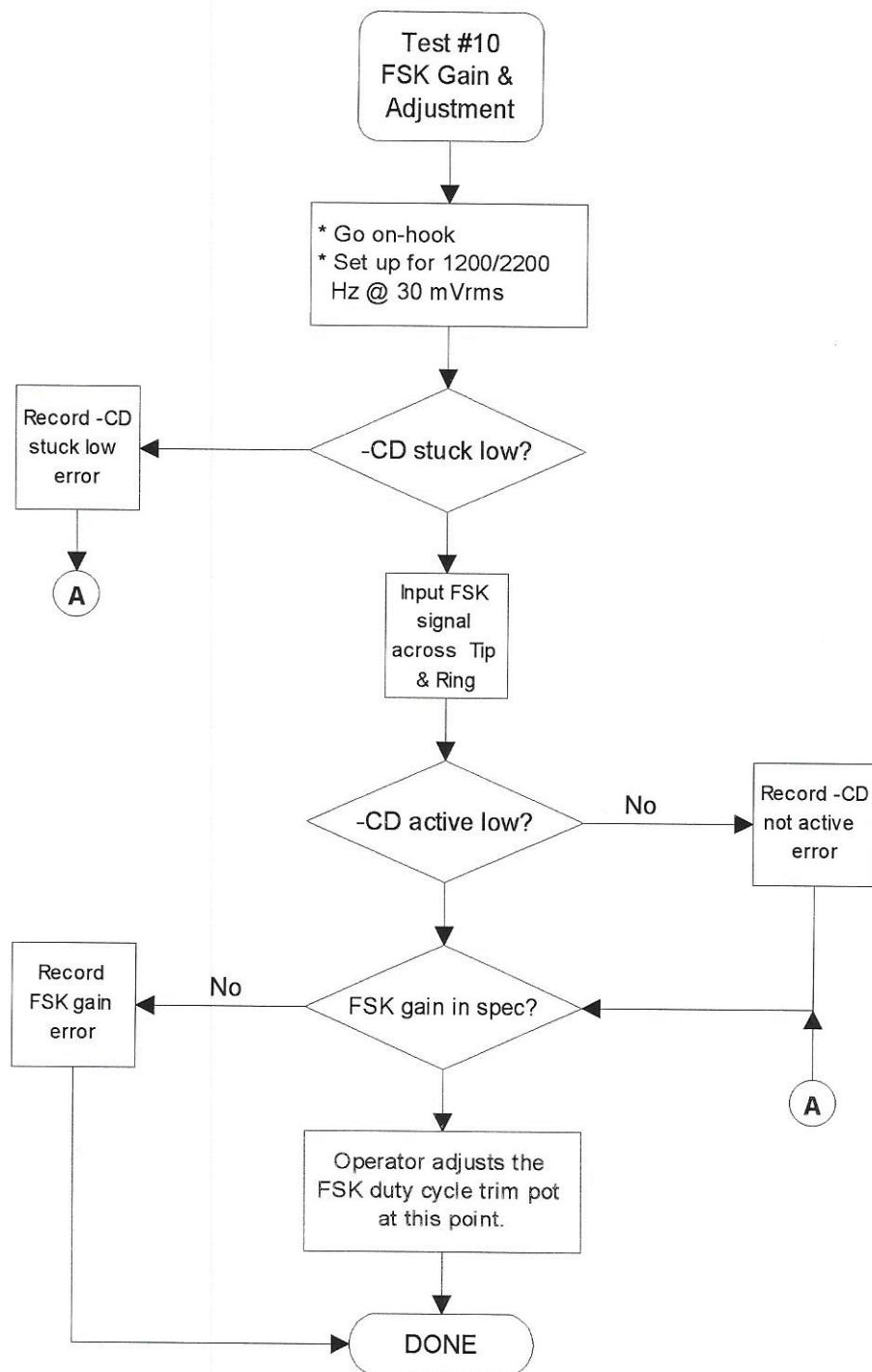
1.5.9 LIU Threshold Detect Test Flow Diagram



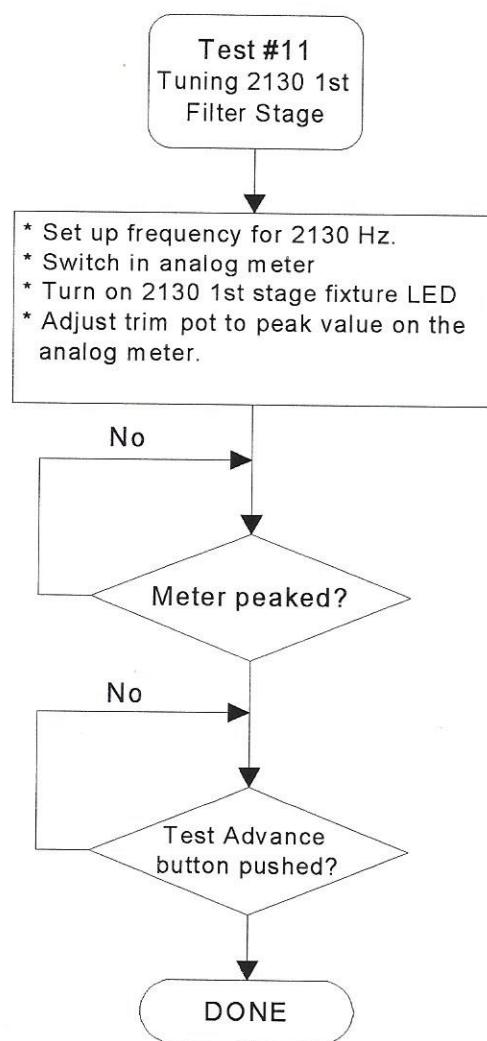
1.5.10 Dial Tone Detect Test Flow Diagram



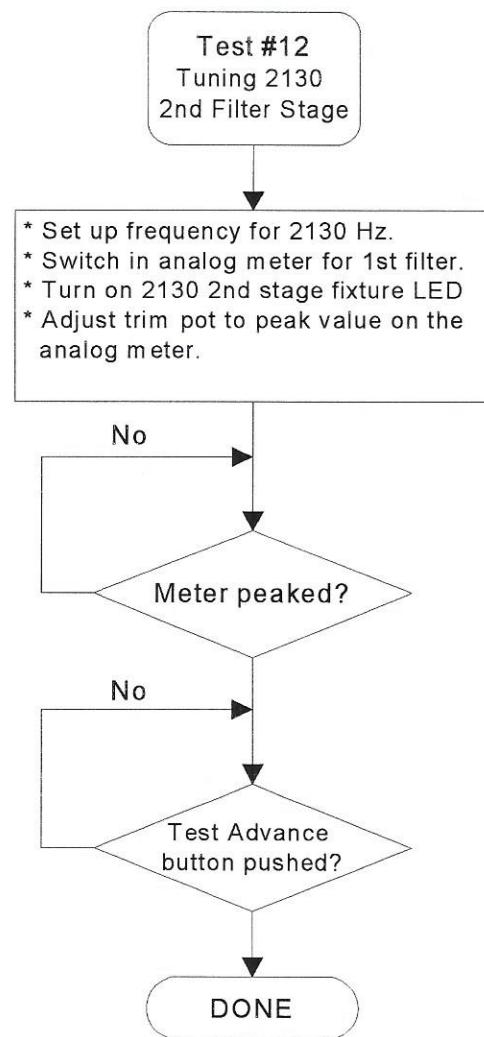
1.5.11 FSK Gain Test and FSK Duty Cycle Adjustment Flow Diagram



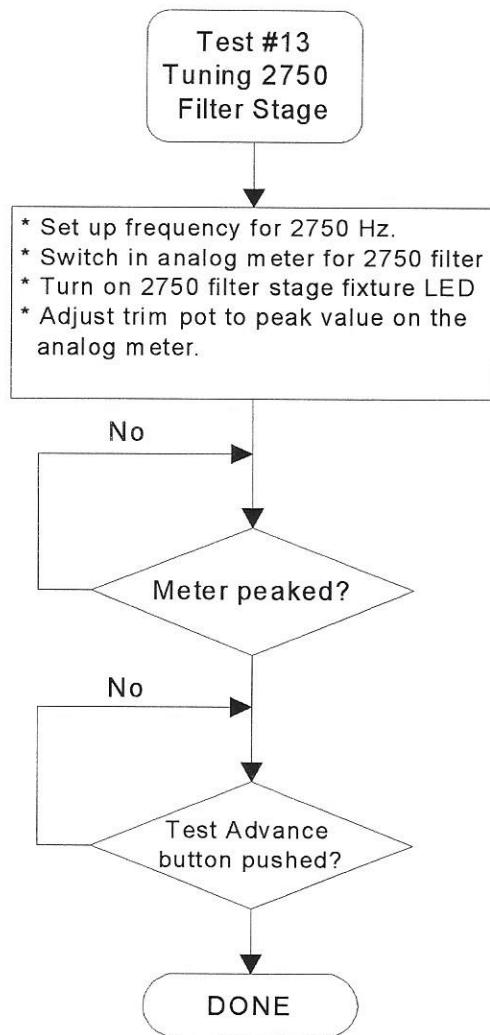
1.5.12 Tuning of 2130 First Filter Stage Flow Diagram



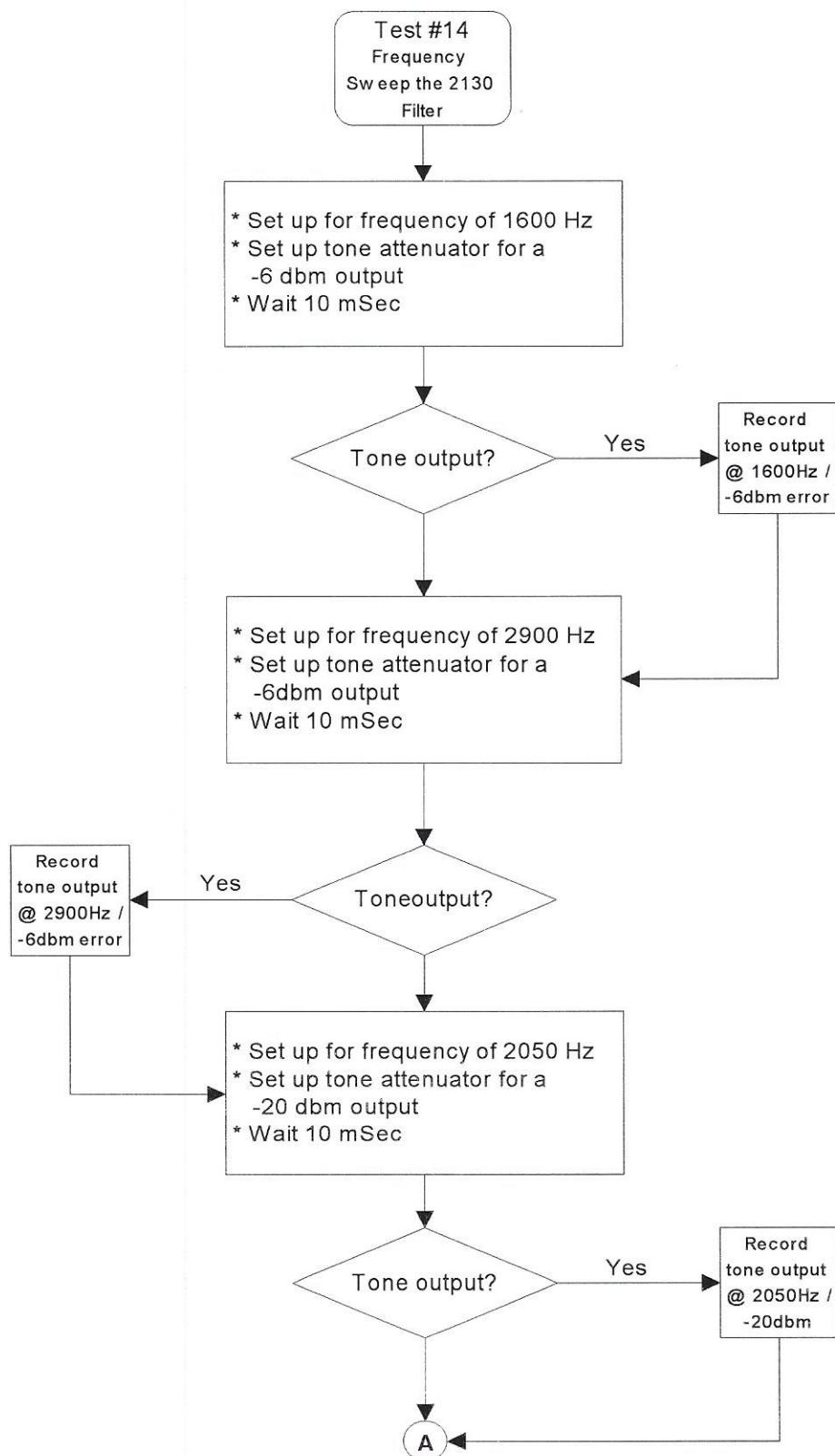
1.5.13 Tuning of 2130 Second Filter Stage Flow Diagram

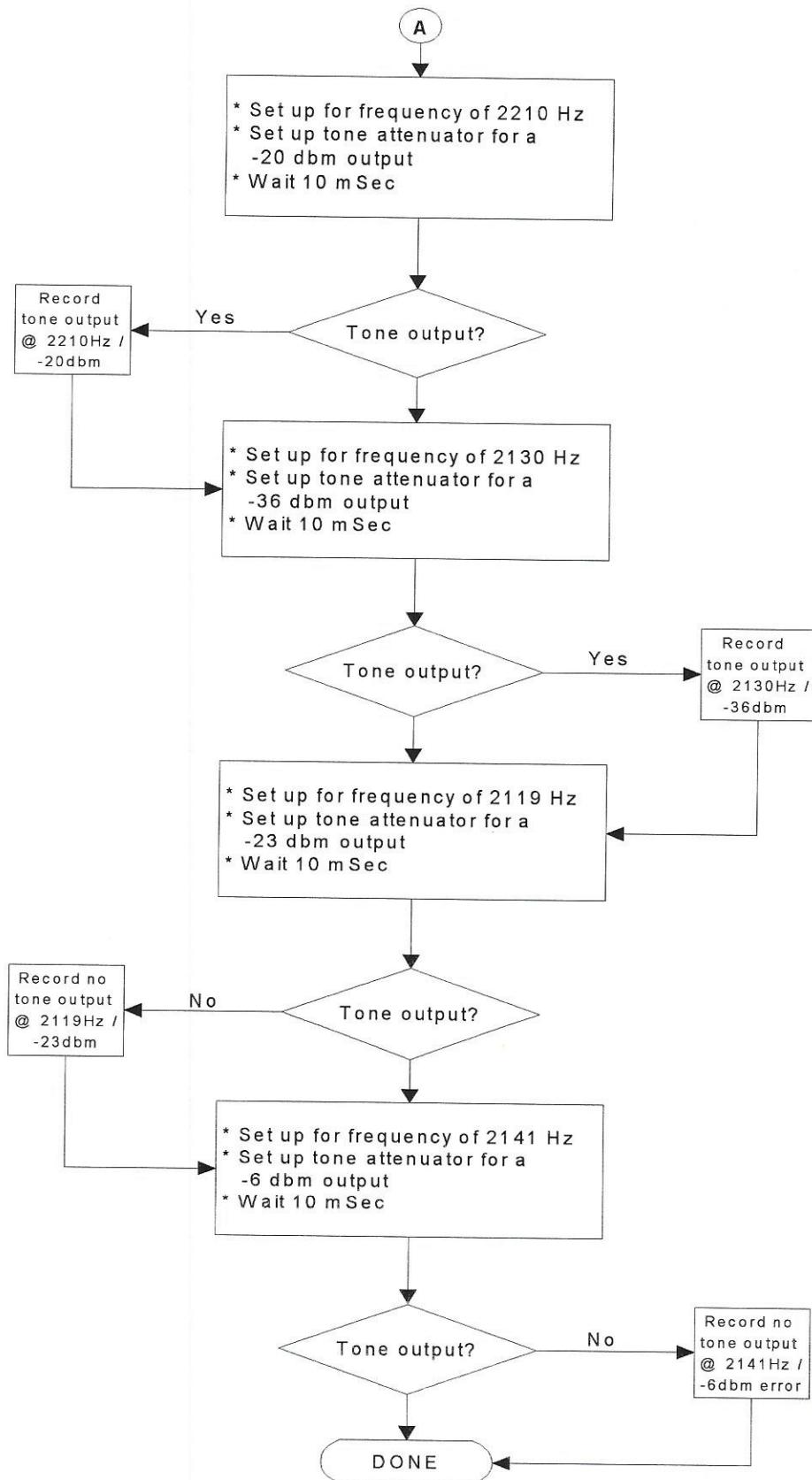


1.5.14 Tuning of 2750 Filter Stage Flow Diagram

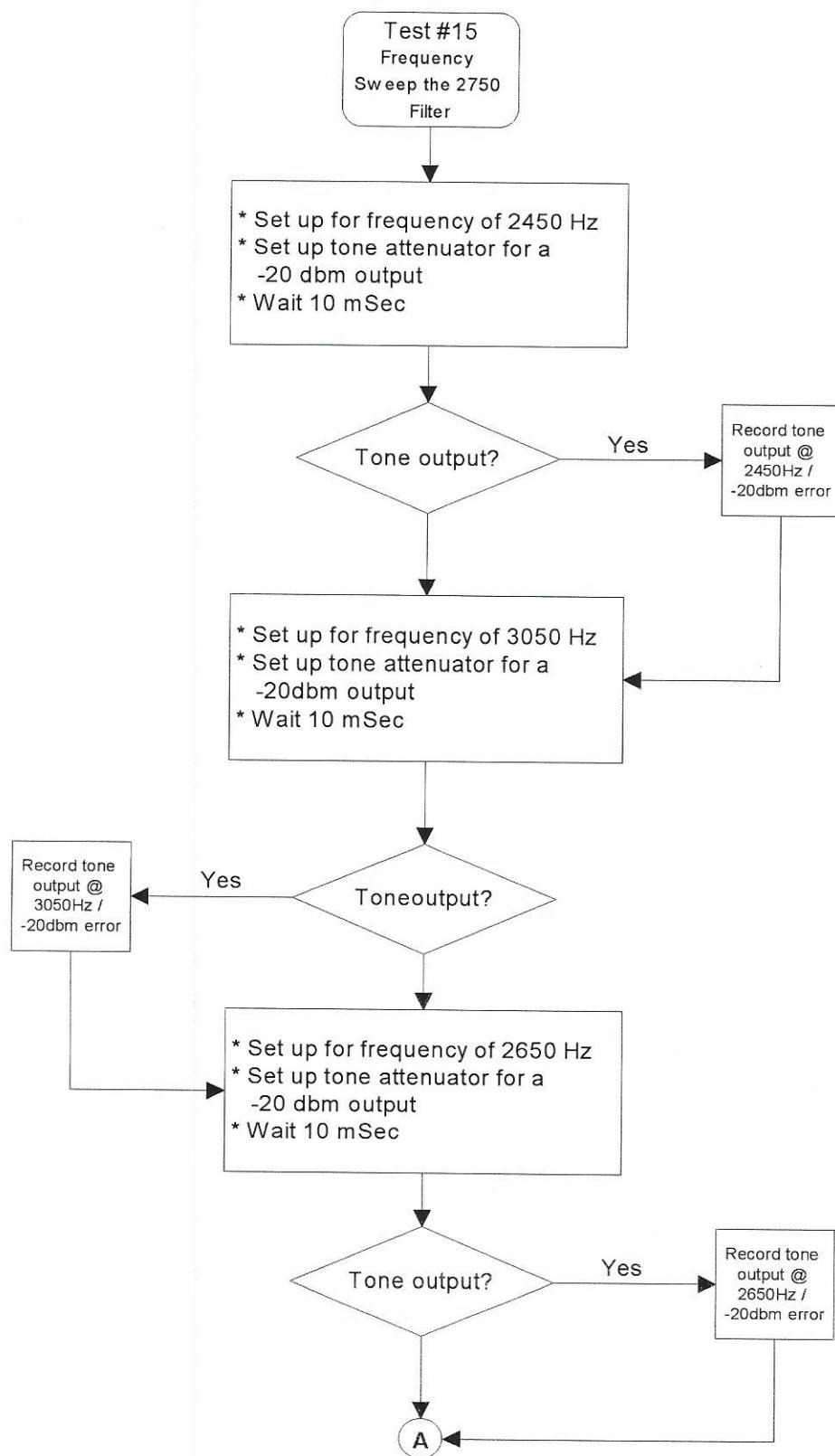


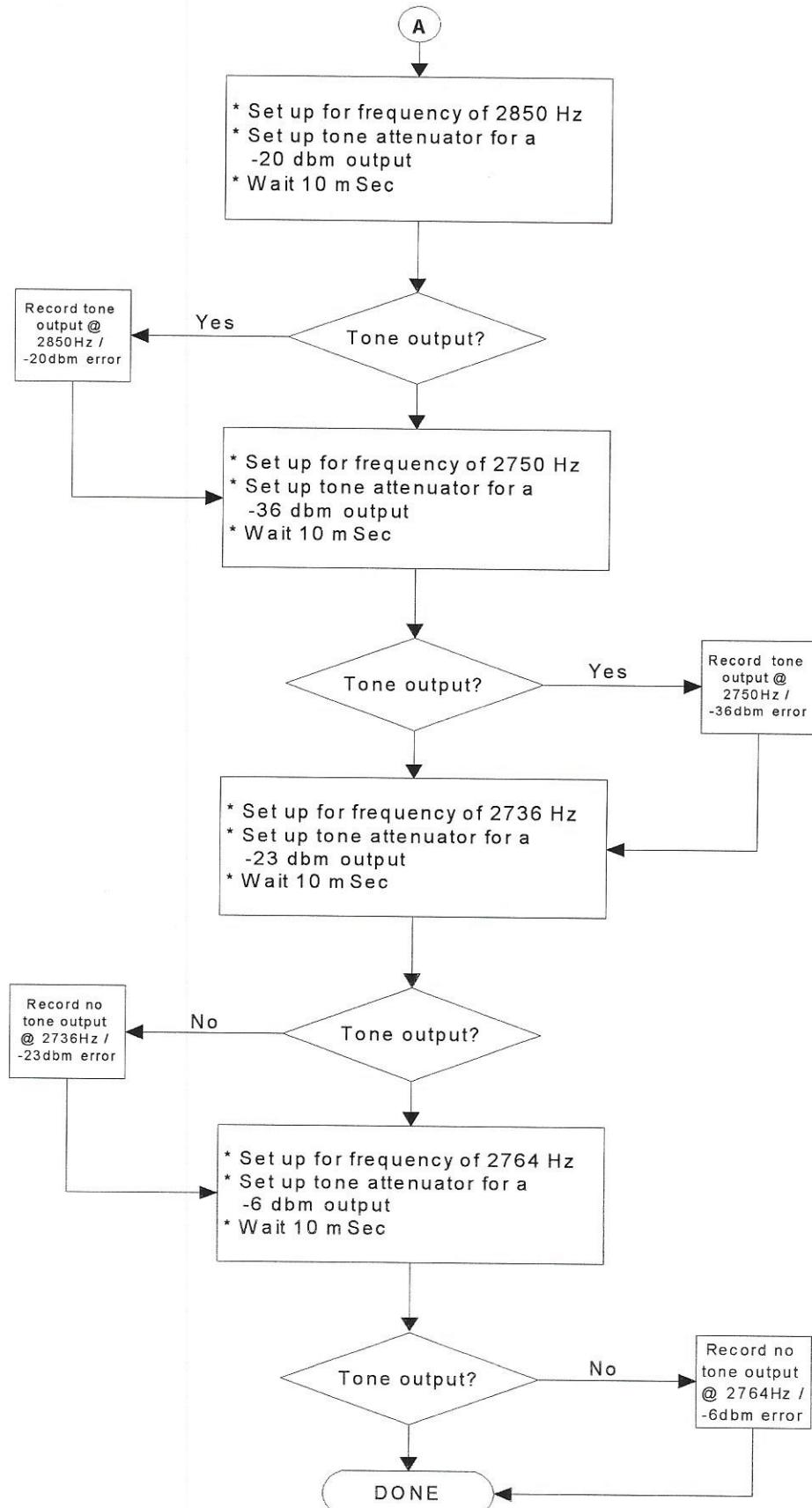
1.5.15 Frequency Sweep 2130 Filter Test Flow Diagram





1.5.16 Frequency Sweep 2750 Filter Test Flow Diagram





1.5.17CAS Tone Detection Test Flow Diagram

