



"The Caller ID Company"

**CGT TESTER DAUGHTER CARD
HARDWARE DESIGN SPECIFICATION**

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1. CGT TESTER DAUGHTER CARD

The CGT tester Daughter Card is a generic test PCB that resides inside a mechanical pogo-pin clamshell style fixture and interfaces the CGT electronics to a Device Under Test (DUT) PCB. The Daughter Card includes all the necessary electronics that will allow the CGT to perform a complete functional test of all the electronic circuitry of the DUT card.

1.1 Daughter Card Features

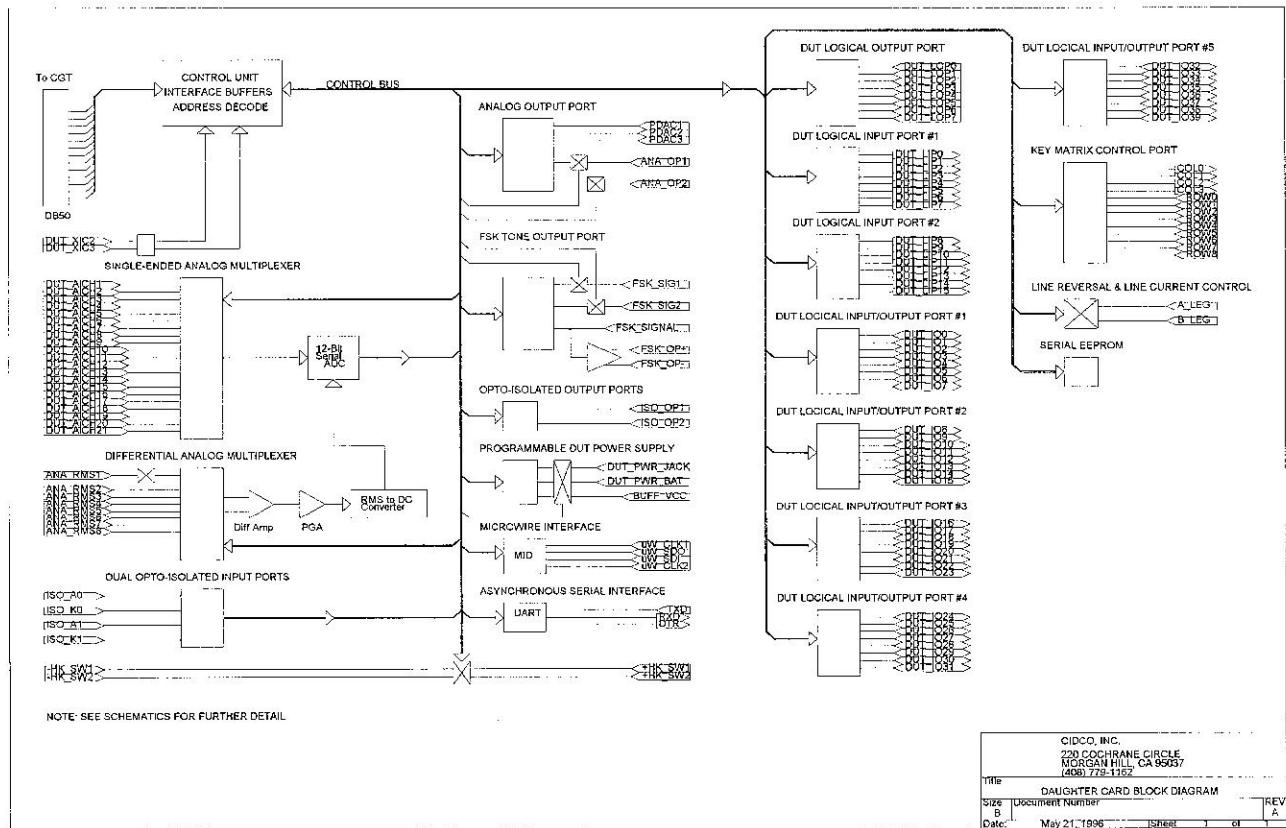
- 1.1.1 One 8-bit tri-stateable output only digital port (not bit programmable).
- 1.1.2 Two 8-bit tri-stateable input only digital ports with selectable pull-ups to isolated power (not bit programmable).
- 1.1.3 Five 8-bit tri-stateable digital ports configurable as either input or output (not bit programmable).
- 1.1.4 Serial Peripheral Interface (SPI) configurable to either operate in the master or slave mode.
- 1.1.5 Asynchronous serial interface (UART) port.
- 1.1.6 A 1K -bit serial EEPROM for parameter characterization and board identification.
- 1.1.7 Eight selectable differential 12-bit Analog-to-Digital channels with programmable gain control and RMS-to-DC conversion.
- 1.1.8 Twenty selectable single-ended 12-bit Analog-to-Digital channels.
- 1.1.9 Three channels of programmably attenuated FSK signal output with one of the channels converted from single-ended to differential.
- 1.1.10 Four programmably selectable single-ended digital-to-analog output channels.
- 1.1.11 Two input and two output digital opto-isolated ports.
- 1.1.12 Programmably selectable switch matrix which can control up to a 9 column by 4 row switch matrix.
- 1.1.13 Eight selectable LED ports for driving external LEDs.

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- 1.1.14 A DPST hook switch relay to control the DUT hook switch status.
- 1.1.15 A programmable power supply with four power levels for driving the DUT AC adapter or battery inputs.
- 1.1.16 A DUT current monitor with programmable current level setting and over-current interrupt to shut off power to the DUT.
- 1.1.17 The Daughter Card can be assigned its own identification by a switch configurable to any of 255 combinations.
- 1.1.18 Other features include a line reversal relay, a line current relay to switch between 20mA or 80mA and a power relay to remove power from the DUT.

1.2 Daughter Card Block Diagram





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1.3 Daughter Card Circuit Description

1.3.1 CGT Interface

1.3.1.1 CGT Interface Circuit Description

The CGT interface comprises circuitry which buffers all input and output signals between the CGT and the Daughter Card over a 50-pin DB50 style connector. The 8-bit octal buffers at locations U16 and U23 buffer the address and control signals between the CGT and the Daughter Card. The 8-bit bi-directional octal buffer at location U28 bufers the data bus between the CGT and the Daughter Card and the data direction is controlled by the state of the signal, -RDSTB. When the -RDSTB signal is in the low state, the data direction is from the Daughter Card to the CGT and when the -RDSTB signal is in the high state, the data direction is from the CGT to the Daughter Card.

1.3.1.2 CGT Interface Signal Description Table

The following table lists and describe each of the interface signals:

DB50 Connector	Signal Type	Signal Name	Description
1			No Connection
2	Power	Ground	Analog ground
3			No Connection
4	Power	Ground	Analog ground
5	Power	Ground	No Connection
6	Power	Ground	Analog ground
7	Input	FSK_SIG	FSK signal input
8	Power	Ground	Analog ground
9	Power	Ground	Analog ground
10			No Connection
11			No Connection
12			No Connection
13	Power	Ground	Digital ground
14	Power	+5VDC	Digital circuit power, input #1
15	Power	+5VDC	Digital circuit power, input #2
16	Power	Ground	Digital ground
17	I/O Bus	RTIO	DUT data bus 6
18	I/O Bus	RTIO	DUT data bus 7



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19	I/O Bus	RTIO	DUT data bus 4
20	I/O Bus	RTIO	DUT data bus 5
21	I/O Bus	RTIO	DUT data bus 2
22	I/O Bus	RTIO	DUT data bus 3
23	I/O Bus	RTIO	DUT data bus 0
24	I/O Bus	RTIO	DUT data bus 1
25	Power	Ground	Digital ground
27	Power	-24VDC	Negative analog circuit power
28	Power	+24VDC	Positive analog circuit power
29	Input	-RDSTB	Read strobe
30	Input	-WRSTB	Write strobe
31	Input	OC2/GPIO3	Address decode bit A2
32	Input	OC3/GPIO2	Address decode bit A3
33	Input	DUT_SYSCLK	DUT system clock
34	Input	XIC4-IO5	Address decode bit A1
35	Output	DUT_INT	DUT interrupt request
36	I/O	XIC3-IO4	Not used
37	Input	DUTDEC_CLK	
38	I/O	XIC2-IO3	Not used
39	Power	Ground	Digital ground
40	Power	Ground	Digital ground
41	Input	DUT_SCLK	Serial clock
42	Input	XIC1-IO2	Address decode bit A4
43	Output	DUT_SDO	Serial data output
44	I/O	XPW2_IO1	Not used
45	Input	DUT_SDI	Serial data input
46	Input	XPW1-IO0	Address decode bit A0
47	Output	DUT_FIXPB	Not used
48	Input	-DUT_RESET	DUT master reset
49	Power	Ground	Digital ground
50	Power	Ground	Digital ground

1.3.2 Address Decode

1.3.2.1 Address Decode Circuit Description

The address decode block comprises buffer U23 and 3-to8 line decoder U24 which together decodes all of the digital control ports on the Daughter Card.



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1.3.2.2 Address Decode Map Table

The following table is a map of all the ports and their addresses. The following equates are true:

Signal input: XIC1-IO2 = A4

Signal input: OC3/GPIO2 = A3

Signal input: OC2/GPIO3 = A2

Address Lines					Decode	Signal Description
A4	A3	A2	A1	A0	U24 Output	
0	0	0	0	0	-HK_CS0+0	PortA of Housekeeping Port #1 @ U61
0	0	0	0	1	-HK_CS0+1	PortB of Housekeeping Port #1 @ U61
0	0	0	1	0	-HK_CS0+2	PortC of Housekeeping Port #1 @ U61
0	0	0	1	1	-HK_CS0+3	Housekeeping port control register of U61
0	0	1	0	0	-HK_CS1+0	PortA of Housekeeping Port #2 @ U62
0	0	1	0	1	-HK_CS1+1	PortB of Housekeeping Port #2 @ U62
0	0	1	1	0	-HK_CS1+2	PortC of Housekeeping Port #2 @ U62
0	0	1	1	1	-HK_CS1+3	Housekeeping port control register of U62
0	1	0	0	0	-DUT_CS0+0	PortA of DUT Port #1 @ U64
0	1	0	0	1	-DUT_CS0+1	PortB of DUT Port #1 @ U64
0	1	0	1	0	-DUT_CS0+2	PortC of DUT Port #1 @ U64
0	1	0	1	1	-DUT_CS0+3	DUT port control register of U64
0	1	1	0	0	-DUT_CS1+0	PortA of DUT Port #2 @ U63
0	1	1	0	1	-DUT_CS1+1	PortB of DUT Port #2 @ U63
0	1	1	1	0	-DUT_CS1+2	PortC of DUT Port #2 @ U63
0	1	1	1	1	-DUT_CS1+3	DUT port control register of U63
1	0	0	0	0	-DUT_CS2+0	PortA of key matrix port @ U31
1	0	0	0	1	-DUT_CS2+1	PortB of key matrix Port @ U31
1	0	0	1	0	-DUT_CS2+2	PortC of key matrix Port @ U31
1	0	0	1	1	-DUT_CS2+3	Key matrix port control register of U31
1	0	1	0	0	-CS_MID	DUT serial interface control Reg of U29
1	0	1	0	1	-XIO_BUS+0	PortA of DUT Port #3 @ U65
1	0	1	1	0	-XIO_BUS+1	PortB of DUT Port #3 @ U65
1	0	1	1	1	-XIO_BUS+2	PortC of DUT Port #3 @ U65
1	1	0	0	0	-XIO_BUS+3	DUT port control register of U65
1	1	0	0	1	-UART	UART serial control register of U66

1.3.3 Housekeeping Digital Control Ports



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1.3.3.1 Housekeeping Digital Control Ports Circuit Description

The digital housekeeping control ports are two 82C55 programmable peripheral interface ICs which each have three 8-bit programmable I/O ports for a combined total of 48 digital I/O pins. The main function of the two I/O ports are to control all housekeeping functions of the Daughter Card.

1.3.3.2 Housekeeping Control Port #1 Signal Description Table

IC Pin #	Port ref	Signal name	Signal description
43	PA0	-ADC_RFS	Enable data reception from ADC at U11
42	PA1	-ADC_TFS	Enable data transmission to ADC at U11
41	PA2	-PGA_WR	Write to programmable gain select analog switch at S1
40	PA3	AMUX_EN	Analog multiplexer enable
38	PA4	-FSK_WR	Write to FSK analog select switch at S2C & S2D
37	PA5	-ADC_CNV	Start ADC conversion cycle at U11
36	PA6	-LD_ATT	Loads FSK attenuator DAC value into U12
35	PA7	-DAC8_LD	Loads value and selects channel of DAC at U14
14	PB0	-ENABIO1	Enables DUT I/O buffer at U40
15	PB1	-ENABIO2	Enables DUT I/O buffer at U41
16	PB2	DIRBIO1	Selects data direction of buffer at U40
18	PB3	DIRBIO2	Selects data direction of buffer at U41
19	PB4	GPIO0	General purpose I/O bit 0
20	PB5	GPIO1	General purpose I/O bit 1
21	PB6	GPIO2	General purpose I/O bit 2
23	PB7	GPIO3	General purpose I/O bit 3
9	PC0	AMUX0	Analog multiplexer channel select bit 0
10	PC1	AMUX1	Analog multiplexer channel select bit 1
11	PC2	AMUX2	Analog multiplexer channel select bit 2
13	PC3	AMUX3	Analog multiplexer channel select bit 3
8	PC4	-ENABIO345	Enables DUT I/O buffers at U52, U53 & U54
7	PC5	DUT_PBIN1	Enables DUT input buffers at U32 & U33
6	PC6	LC_RLY	Controls the line current select relay at K6
5	PC7	DUT_PAOUT	Enables the DUT output buffer at U39

1.3.3.4 Housekeeping Control Port #2 Signal Description Table

IC Pin #	Port ref	Signal name	Signal description
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43	PA0	ID0	Daughter Card identification bit 0
42	PA1	ID1	Daughter Card identification bit 1
41	PA2	ID2	Daughter Card identification bit 2
40	PA3	ID3	Daughter Card identification bit 3
38	PA4	ID4	Daughter Card identification bit 4
37	PA5	ID5	Daughter Card identification bit 5
36	PA6	ID6	Daughter Card identification bit 6
35	PA7	ID7	Daughter Card identification bit 7
14	PB0	EN_HKSW	Enables the DUT hook switch relay at K4
15	PB1	EEPCS	Chip select for the serial EEPROM at U17
16	PB2	EN_TRLY	Enable the Tip & Ring relay
18	PB3	EN_CAP	Enable the RMS to DC converter capacitor relay at K2
19	PB4	EN_MSTR	Configure the DUT serial interface to the master mode
20	PB5	EN_SLAVE	Configure the DUT serial interface to the master mode
21	PB6	PWR_RLY	Enable the DUT power select relay at K3
23	PB7	LR_RLY	Enable the line reversal relay at K7
9	PC0	DIRBIO3	Set data direction of buffer U53: 0=input, 1=output
10	PC1	DIRBIO4	Set data direction of buffer U52: 0=input, 1=output
11	PC2	DIRBIO5	Set data direction of buffer U54: 0=input, 1=output
13	PC3	DIS_PWR	Disconnect power from the DUT at relay K5
8	PC4	EN_4VDC	Enable +4Vdc power to the DUT
7	PC5	EN_6VDC	Enable +6Vdc power to the DUT
6	PC6	EN_9VDC	Enable +9Vdc power to the DUT
5	PC7	EN_12VDC	Enable +12Vdc power to the DUT

1.3.4 Analog and DC Signal Measurement Block

1.3.4.1 Analog to Digital Signal Measurement Block Components

The signal measurement block consists of the following components:

1. 16-channel signal-ended analog multiplexer at location U10.
2. 8-channel differential analog multiplexer at location U5.
3. Differential to single-ended analog signal converter at location U6A.
4. Programmable gain stage at locations U6 and S1.
5. RMS to DC analog signal converter at location U7.
6. An 8-channel, 12-bit analog-to-digital converter with serial interface and digital control at location U11.



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1.3.4.2 Analog to Digital Signal Measurement Block Circuit Description

The measurement process is started by deciding which signal needs to be measured. The appropriate multiplexer and analog signal paths are selected based on whether the signal is single-ended or differential analog or DC level. Next the appropriate gain setting needs to be set depending upon the signal level to be measured. There are four gain settings; 1x, 2x, 5x, 10x and are set by selecting the appropriate analog switch setting at S1. The I/O control port at U61 starts the A-to-D conversion cycle at U11 by first setting the signal -TFS active low and then toggling the -CONVST signal. After waiting for the conversion cycle to complete, the CGT reads the value from the A-to-D via the serial interface and then determines whether the value read is within a specified limit and sets the pass/fail criteria based on the prescribe limit values.

1.3.4.3 Analog to Digital Signal Measurement Block Signal Table

The following table lists and describes the analog signals between the DUT and the Daughter Card:

Conn Pin #	Port Pin #	Signal Name	Signal Description
J16-1/J16-2	U10-19	DUT_AiCH1	DC Tip & Ring measurements
J18-1	U10-20	DUT_AiCH2	General purpose single-ended analog input #2
J18-2	U10-21	DUT_AiCH3	General purpose single-ended analog input # 3
J18-3	U10-22	DUT_AiCH4	General purpose single-ended analog input # 4
J18-4	U10-23	DUT_AiCH5	General purpose single-ended analog input # 5
J18-5	U10-24	DUT_AiCH6	General purpose single-ended analog input # 6
J18-6	U10-25	DUT_AiCH7	General purpose single-ended analog input # 7
J18-7	U10-26	DUT_AiCH8	General purpose single-ended analog input # 8
J18-8	U10-11	DUT_AiCH9	General purpose single-ended analog input # 9
J18-9	U10-10	DUT_AiCH10	General purpose single-ended analog input # 10
J18-10	U10-9	DUT_AiCH11	General purpose single-ended analog input # 11
J18-11	U10-8	DUT_AiCH12	General purpose single-ended analog input # 12
J18-12	U10-7	DUT_AiCH13	General purpose single-ended analog input # 13
J18-13	U10-6	DUT_AiCH14	General purpose single-ended analog input # 14
J18-14	U10-5	DUT_AiCH15	General purpose single-ended analog input # 15
J18-15	U11-17	DUT_AiCH17	General purpose single-ended analog input # 17
J18-16	U11-18	DUT_AiCH18	General purpose single-ended analog input # 18
J18-17	U11-19	DUT_AiCH19	General purpose single-ended analog input # 19
J18-18	U11-20	DUT_AiCH20	General purpose single-ended analog input # 20
J18-19	U11-21	DUT_AiCH21	General purpose single-ended analog input # 21



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J18-20	U5-	+HS_EAR	Positive receive gain of the handset
J18-21	U5-	-HS_EAR	Negative receive gain of the handset
J18-22	U5-	+AUD_AMP	Positive audio amplifier gain
J18-23	U5-	-AUD_AMP	Negative audio amplifier gain
J18-24	U5-	+RING_VOL	Positive ring volume level
J18-25	U5-	-RING_VOL	Negative ring volume level
J18-26	U5-	+ANA_RMS5	General purpose +differential analog input #5
J18-27	U5-	-ANA_RMS5	General purpose -differential analog input #5
J18-28	U5-	+ANA_RMS6	General purpose +differential analog input #6
J18-29	U5-	-ANA_RMS6	General purpose -differential analog input #6
J18-30	U5-	+ANA_RMS7	General purpose +differential analog input #7
J18-31	U5-	-ANA_RMS7	General purpose -differential analog input #7
J18-32	U5-	+ANA_RMS8	General purpose +differential analog input #8
J18-33	U5-	-ANA_RMS8	General purpose -differential analog input #8

1.3.5 DUT Digital Input / Output Control Block

1.3.5.1 Control Block Components

The digital input/output control block consists of the following components:

1. Three 82C55 24-bit peripheral interface ports at locations U63, U64 and U65.
2. One octal tri-stateable output only buffer at location U39.
3. Two octal tri-stateable input only buffers at locations U32 and U33.
4. Five octal tri-stateable buffers configurable as either input or output at locations U40, U41, U52, U53 and U54.
5. Two opto-isolated output ports at locations U44 and U45.
6. Two opto-isolated input ports at locations U42 and U43.
7. Fixture front panel push-button and switch scan port, DUT overcurrent port and four external LED driver ports with interrupt port at locations U64, U58 and U30A.

1.3.5.2 DUT Digital Port Circuit Description

The digital input/output ports at locations U63, U64, and U65 are instructed by the CGT over the data bus and control bus to select the appropriate input port bit or output port bit. The CGT then instructs the



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housekeeping control port at location U61 to enable the appropriate input or output buffer that corresponds to the selected input bit or output bit of the DUT control port. If an input buffer is selected, the CGT will read the input status of the selected DUT input signal by interrogating the DUT control port (either U62, U63 or U64) input register. If an output bit is selected, the DUT control port will output the appropriate signal to the DUT through the selected output buffer.

1.3.5.3 Fixture Pushbutton & Switch Scan Port

The fixture pushbutton status, fixture switch status and DUT overcurrent status can be scanned by the DUT control port at location U64 and reported back to the CGT. While the test is in progress, an interrupt can be triggered by a stop pushbutton, fixture switch opening or an overcurrent condition whereby the test will either be stopped or be aborted by the CGT.

1.3.5.4 LED Driver Port

The DUT control port at location U63 can control four LED drivers by enabling or disabling the LED driver gates. The LED driver gates are located at U36A,B,C & D. The drivers can sync one standard LED per gate with each gate having a 330 ohm current limiting resistor in series with the external LED. Each of these gates are general purpose in nature and can be used for other purposes.

1.3.5.5 Opto-isolator Ports

There two opto-isolated outputs ports at locations U44, U45, U38A & U38B and two opto-isolated input ports at locations U42 and U43 which are controlled by the DUT control port at location U64. The opto-isolated ports are for general purpose usage and are used when signal isolation or signal translation is needed.

Conn Pin #	Port Pin #	Signal Name	Signal Description
J11-1	U45-8	ISO_OP1_VCC	Opto-isolator output #1 device power
J11-2	U45-5	ISO_OP1_GND	Opto-isolator output #1 device ground
J11-3	U45-6,7	ISO_OP1	Opto-isolator output port #1
J11-4	U44-6,7	ISO_OP2	Opto-isolator output port #1



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J11-5	U44-8	ISO_OP2_VCC	Opto-isolator output #1 device power
J11-6	U44-5	ISO_OP2_GND	Opto-isolator output #1 device ground
J11-7	U43-2	ISO_A0	Opto-isolator input port #1
J11-8	U43-3	ISO_K0	
J11-9	U42-2	ISO_A1	Opto-isolator input port #2
J11-10	U42-3	ISO_K1	

1.3.5.7 DUT Control Ports Table

The following table lists and describes the interface pins and signal descriptions between the DUT and the Daughter Card input/output buffers.

Conn Pin #	Port Pin #	Signal Name	Signal Description
J12-1	U39-11	DUT_OUT0	General purpose DUT digital output bit #0
J12-2	U39-12	DUT_OUT1	General purpose DUT digital output bit #1
J12-3	U39-13	DUT_OUT2	General purpose DUT digital output bit #2
J12-4	U39-14	DUT_OUT3	General purpose DUT digital output bit #3
J12-5	U39-15	DUT_OUT4	General purpose DUT digital output bit #4
J12-6	U39-16	DUT_OUT5	General purpose DUT digital output bit #5
J12-7	U39-17	DUT_OUT6	General purpose DUT digital output bit #6
J12-8	U39-18	DUT_OUT7	General purpose DUT digital output bit #7
J12-9	U33-11	DUT_IN0	General purpose DUT digital input bit #0
J12-10	U33-12	DUT_IN1	General purpose DUT digital input bit #1
J12-11	U33-13	DUT_IN2	General purpose DUT digital input bit #2
J12-12	U33-14	DUT_IN3	General purpose DUT digital input bit #3
J12-13	U33-15	DUT_IN4	General purpose DUT digital input bit #4
J12-14	U33-16	DUT_IN5	General purpose DUT digital input bit #5
J12-15	U33-17	DUT_IN6	General purpose DUT digital input bit #6
J12-16	U33-18	DUT_IN7	General purpose DUT digital input bit #7
J12-17	U32-11	DUT_IN8	General purpose DUT digital input bit #8
J12-18	U32-12	DUT_IN9	General purpose DUT digital input bit #9
J12-19	U32-13	DUT_IN10	General purpose DUT digital input bit #10
J12-20	U32-14	DUT_IN11	General purpose DUT digital input bit #11
J12-21	U32-15	DUT_IN12	General purpose DUT digital input bit #12
J12-22	U32-16	DUT_IN13	General purpose DUT digital input bit #13
J12-23	U32-17	DUT_IN14	General purpose DUT digital input bit #14
J12-24	U32-18	DUT_IN15	General purpose DUT digital input bit #15
J12-25	U40-18	DUT_IO0	General purpose DUT digital input/output bit #0
J12-26	U40-17	DUT_IO1	General purpose DUT digital input/output bit #1
J12-27	U40-16	DUT_IO2	General purpose DUT digital input/output bit #2
J12-28	U40-15	DUT_IO3	General purpose DUT digital input/output bit #3



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J12-29	U40-14	DUT_IO4	General purpose DUT digital input/output bit #4
J12-30	U40-13	DUT_IO5	General purpose DUT digital input/output bit #5
J12-31	U40-12	DUT_IO6	General purpose DUT digital input/output bit #6
J12-32	U40-11	DUT_IO7	General purpose DUT digital input/output bit #7
J12-33	U41-18	DUT_IO8	General purpose DUT digital input/output bit #8
J12-34	U41-17	DUT_IO9	General purpose DUT digital input/output bit #9
J12-35	U41-16	DUT_IO10	General purpose DUT digital input/output bit #10
J12-36	U41-15	DUT_IO11	General purpose DUT digital input/output bit #11
J12-37	U41-14	DUT_IO12	General purpose DUT digital input/output bit #12
J12-38	U41-13	DUT_IO13	General purpose DUT digital input/output bit #13
J12-39	U41-12	DUT_IO14	General purpose DUT digital input/output bit #14
J12-40	U41-11	DUT_IO15	General purpose DUT digital input/output bit #15
J13-1	U53-18	DUT_IO16	General purpose DUT digital input/output bit #16
J13-2	U53-17	DUT_IO17	General purpose DUT digital input/output bit #17
J13-3	U53-16	DUT_IO18	General purpose DUT digital input/output bit #18
J13-4	U53-15	DUT_IO19	General purpose DUT digital input/output bit #19
J13-5	U53-14	DUT_IO20	General purpose DUT digital input/output bit #20
J13-6	U53-13	DUT_IO21	General purpose DUT digital input/output bit #21
J13-7	U53-12	DUT_IO22	General purpose DUT digital input/output bit #22
J13-8	U53-11	DUT_IO23	General purpose DUT digital input/output bit #23
J13-9	U52-18	DUT_IO24	General purpose DUT digital input/output bit #24
J13-10	U52-17	DUT_IO25	General purpose DUT digital input/output bit #25
J13-11	U52-16	DUT_IO26	General purpose DUT digital input/output bit #26
J13-12	U52-15	DUT_IO27	General purpose DUT digital input/output bit #27
J13-13	U52-14	DUT_IO28	General purpose DUT digital input/output bit #28
J13-14	U52-13	DUT_IO29	General purpose DUT digital input/output bit #29
J13-15	U52-12	DUT_IO30	General purpose DUT digital input/output bit #30
J13-16	U52-11	DUT_IO31	General purpose DUT digital input/output bit #31
J13-17	U54-18	DUT_IO32	General purpose DUT digital input/output bit #32
J13-18	U54-17	DUT_IO33	General purpose DUT digital input/output bit #33
J13-19	U54-16	DUT_IO34	General purpose DUT digital input/output bit #34
J13-20	U54-15	DUT_IO35	General purpose DUT digital input/output bit #35
J13-21	U54-14	DUT_IO36	General purpose DUT digital input/output bit #36
J13-22	U54-13	DUT_IO37	General purpose DUT digital input/output bit #37
J13-23	U54-12	DUT_IO38	General purpose DUT digital input/output bit #38
J13-24	U54-11	DUT_IO39	General purpose DUT digital input/output bit #39

1.3.6 Programmable DUT Power Supply and Current monitor



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1.3.6.1 Power Supply and Current Monitor Components

The programmable power supply and current monitor consist of the following components:

1. An LM317 adjustable voltage regulator rated at 0.5amps at location U15.
2. Selectable voltage resistor ladder with 5 voltage settingsas follows:
+1.25Vdc (off state), +4.0Vdc, +6.0Vdc, +9.0Vdc & +12.0Vdc.
3. A power relay to switch between AC adapter power or battery power at location K3.
4. A power relay to remove power from the DUT at location K5. The relay is activated when +1.25Vdc is selected.
5. A current monitor circuit at locations U8A & U9A with programmable overcurrent trip level at U8A.

1.3.6.2 Power Supply Circuit Description and Table

The DUT programmable power supply is an adjustable power supply that supplies the power to test the DUT. The power supply has five power settings and is controlled by the housekeeping control port at U62. The power can be disabled by selecting the +1.25Vdc setting which in turn activates relay K5 which removes power from the DUT. The AC adapter (primary) power and the battery power are routed to the DUT through the power relay at K3 which can be switched between the two power sources as needed during the test process. The DUT power supply pinout and description table is as follows:

DUT Interface Pin #	Signal Name	Signal Description
J20-6	BUFF_VCC	DUT +5 Volt DC power
J20-8,10	DUT_PWR_JACK	DUT AC adapter power
J20-12	DUT_PWR_BAT	DUT battery power

1.3.6.3 Current Monitor Circuit Description

The current monitor circuit monitors the DUT power for any overcurrent condition. The current is sensed by measuring the voltage drop across R46, a 0.2 ohm power resistor. The voltage difference is then amplified by a factor of five through the Op Amp at U9A and applied to the negative input of comparator U8A. The input level is then compared against a threshold set by a DAC at location U14 If the input voltage level exceeds the set threshold, the



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comparator output goes active low which can then be read by the DUT control port at U64 and/or can trigger an interrupt event to the CGT.

1.3.7 DUT Serial Communications Interface

1.3.7.1 Synchronous Serial Communications Interface

The DUT synchronous serial communications interface is controlled by a TP3465V at U29, a microwire interface device (MID). This device can be configured to run in either the Master mode or in the Slave mode depending upon the test requirements of the DUT. The MID can drive two serial clock streams which enables the MID to communicate to two DUT serial devices. The MID is controlled by the CGT through the local data bus and control bus which converts parallel data to synchronous serial data during transmission and converts serial data to parallel data during reception. The housekeeping control port selects the MID and controls external gating logic at U25 and U26A to support either master or slave operation. An external 74HC74 at U48 shifts the serial data one half clock bit either on the negative edge or the positive edge of the serial clock depending on the DUT being tested. A tri-state buffer, a 74HC126 at U22 controls the direction of the main serial clock and also disables the serial interface when not being used.

1.3.7.2 Asynchronous Serial Communications Interface

The 82C51 is a USART at location U66 which enables asynchronous serial communication to the DUT. The device converts parallel data from the CGT into serial data during transmission and converts serial data into parallel data during reception. The USART is configured to operate at 4800 baud.

1.3.7.3 Serial Communications Table

DUT Interface Pin #	Signal Name	Signal Description
J13-32	SPI_CLK1	DUT Synchronous serial clock #1
J13-33	SPI_DATAOUT	DUT Synchronous serial data out
J13-34	SPI_DATAIN	DUT Synchronous serial data in
J13-35	SPI_CLK2	DUT Synchronous serial clock #2
J13-37	TXD	DUT asynchronous serial transmit
J13-38	DTR	Data terminal ready



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J13-39	RXD	DUT asynchronous serial receive
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1.3.8 DUT Key Matrix Port

1.3.8.1 Key Matrix Control Port Circuit Description

The DUT key matrix control port at location U31 is an 82C55 which has three 8-bit ports which can be configured as either inputs or outputs. The control port controls a bank of transistors which electrically duplicate the making and breaking of the mechanical switch key matrix of the DUT. The key matrix switches are configured in a 9 row by 4 column matrix which allows testing of all of the DTMF keys and all rows and column traces of the DUT. The activation of a key is as follows; to activate DTMF key number one, the control selects the electrical switch associated with key number one. The DUT senses the closed key and will send the key number to the Daughter Card over the serial bus where the CGT will read the key information from the MID and verify that the correct key was sensed.

A secondary function of the control port is to enable and control a bank of four LED drivers. See a description of the LED drivers under 1.3.5.4 above.

1.3.8.2 Key Matrix Control Port Signal Description Table

Port Pin #	Port Name	Signal Name	Signal Description
U31-43	PA0	SW1	Electrical switch control #1, Row 0, Column 0
U31-42	PA1	SW2	Electrical switch control #2, Row 1, Column 0
U31-41	PA2	SW3	Electrical switch control #3 Row 2, Column 0
U31-40	PA3	SW4	Electrical switch control #4 Row 3, Column 0
U31-38	PA4	SW5	Electrical switch control #5 Row 0, Column 1
U31-37	PA5	SW6	Electrical switch control #6 Row 1, Column 1
U31-36	PA6	SW7	Electrical switch control #7 Row 2, Column 1
U31-35	PA7	SW8	Electrical switch control #8 Row 3, Column 1
U31-14	PB0	SW9	Electrical switch control #9 Row 0, Column 2
U31-15	PB1	SW10	Electrical switch control #10 Row 1, Column 2
U31-16	PB2	SW11	Electrical switch control #11, Row 2, Column 2
U31-18	PB3	SW12	Electrical switch control #12, Row 3, Column 2
U31-19	PB4	SW13	Electrical switch control #13, Row 0, Column 3
U31-20	PB5	SW14	Electrical switch control #14, Row 0, Column 3
U31-21	PB6	SW15	Electrical switch control #15, Row 0, Column 3



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U31-23	PB7	SW16	Electrical switch control #16, Row 4, Column 2
U31-9	PC0	SW17	Electrical switch control #17, Row 5, Column 2
U31-10	PC1	SW18	Electrical switch control #18, Row 6, Column 2
U31-11	PC2	SW19	Electrical switch control #19, Row 7, Column 2
U31-13	PC3	SW20	Electrical switch control #20, Row 8, Column 2
U31-8	PC4	LED_EN8	Enable LED driver number 8
U31-7	PC5	LED_EN7	Enable LED driver number 7
U31-6	PC6	LED_EN6	Enable LED driver number 6
U31-5	PC7	LED_EN5	Enable LED driver number 5

1.3.8.3 Key Matrix to DUT Interface Table

1.3.9 Digital to Analog Output Port

DUT I/F Pin #	Signal Name	Signal Description
J14-13	COL1	Key matrix column 1
J14-14	COL0	Key matrix column 0
J14-15	COL3	Key matrix column 3
J14-16	COL2	Key matrix column 2
J14-17	ROW1	Key matrix row 1
J14-18	ROW0	Key matrix row 0
J14-19	ROW3	Key matrix row 3
J14-20	ROW2	Key matrix row 2
J14-21	ROW5	Key matrix row 5
J14-22	ROW4	Key matrix row 4
J14-23	ROW7	Key matrix row 7
J14-24	ROW6	Key matrix row 6
J14-26	ROW8	Key matrix row 8

1.3.9.1 Digital to Analog Output Port Circuit Description

The digital to analog (DAC) output port at U14 has seven analog output channels with two of the signals controlled by an analog switch at S2C and S2D. Two of the output signals are used by the Daughter Card, one of the signals, SYSTST, is used to verify that the analog measurement circuit is working correctly and the other signal, DUT_ISET, is used to set the overcurrent threshold limit at comparator U8A of the current monitor. The DAC values are input via the CGT serial bus and latched into the DAC by toggling the signal, -DAC_LD from the housekeeping control port.



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1.3.9.2 DAC Output Port Signal Table

DUT I/F Pin #	Signal Name	Signal Description
J18-34	PDAC3	General purpose analog output signal #3
J18-35	PDAC1	General purpose analog output signal #1
J18-36	PDAC2	General purpose analog output signal #2
J18-37	ANA_OP1	General purpose switched analog output signal #1
J18-38	ANA_OP2	General purpose switched analog output signal #2
None	DUT_ISET	Overcurrent threshold setting
None	SYSTST	Analog measurement circuit test signal

1.3.10 FSK Signal Attenuator Block

1.3.10.1 FSK Signal Attenuator Signal Block Components

1. Unity gain buffer and FSK signal active filter at location U13B.
2. Serial 12-bit digital to analog converter at location U12.
3. DAC output unity gain filter and signal buffer at location U13A.
4. Two channel analog switch at location S2A and S2B.
5. Singled-ended to differential unity gain buffer at location U50A and U50B.

1.3.10.2 FSK Signal Attenuator Block Circuit Description

The FSK signal attenuator block is comprised of a 12-bit serial DAC8043 at location U14. The signal to be attenuated is applied to the VREF input of the DAC. The output value of the DAC is based on the range of the signal applied to the VREF input of the DAC and the value loaded into the DAC. The value is loaded into the DAC from the CGT over the serial bus and is latched into the DAC by the signal, -LD_ATT, controlled by the housekeeping control port. Input filtering of the FSK signal is done by the active filter and unity gain buffer at U13B. Output filtering of the DAC signal is done by the active filter and unity gain buffer at U13A. Analog switches at locations S2A and S2B provide steering control of the output signal from the DAC to the DUT and the signal is also provided unswitched to the DUT or other useage. The unswitched single-ended FSK output signal is also converted to a differential signal at U50A and U50B and is available for general purpose useage.

1.3.10.3 FSK Signal Attenuator Block Signal Description Table



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DUT I/F Pin #	Signal Name	Signal Description
J17-1	FSK_SIGNAL	Unswitched attenuated FSK signal
J17-3	FSK_SIG1	Switched attenuated FSK signal number 1
J17-5	FSK_SIG2	Switched attenuated FSK signal number 2
J17-7	FSK_AMP+	Positive differential attenuated FSK signal
J17-9	FSK_AMP-	Negative differential attenuated FSK signal

1.3.11 Hook Switch Relay

1.3.11.1 Hook Switch Relay Circuit Description

The electronic hook switch relay at location K4 is a DPST relay which provides electrical control of the DUT hook switch. The mechanical fixture has to hold the DUT hook switch in the open (on-hook) position in order for the Daughter Card to electrically control the opening (on-hook) and closing (off-hook) of the hook switch during the test process. The signal to control the relay, EN_HKSW, drives a transistor at location Q9 which switches K4 on or off. The signal, EN_HKSW, is controlled by the housekeeping control port.

1.3.11.2 Hook Switch Relay Signal Table

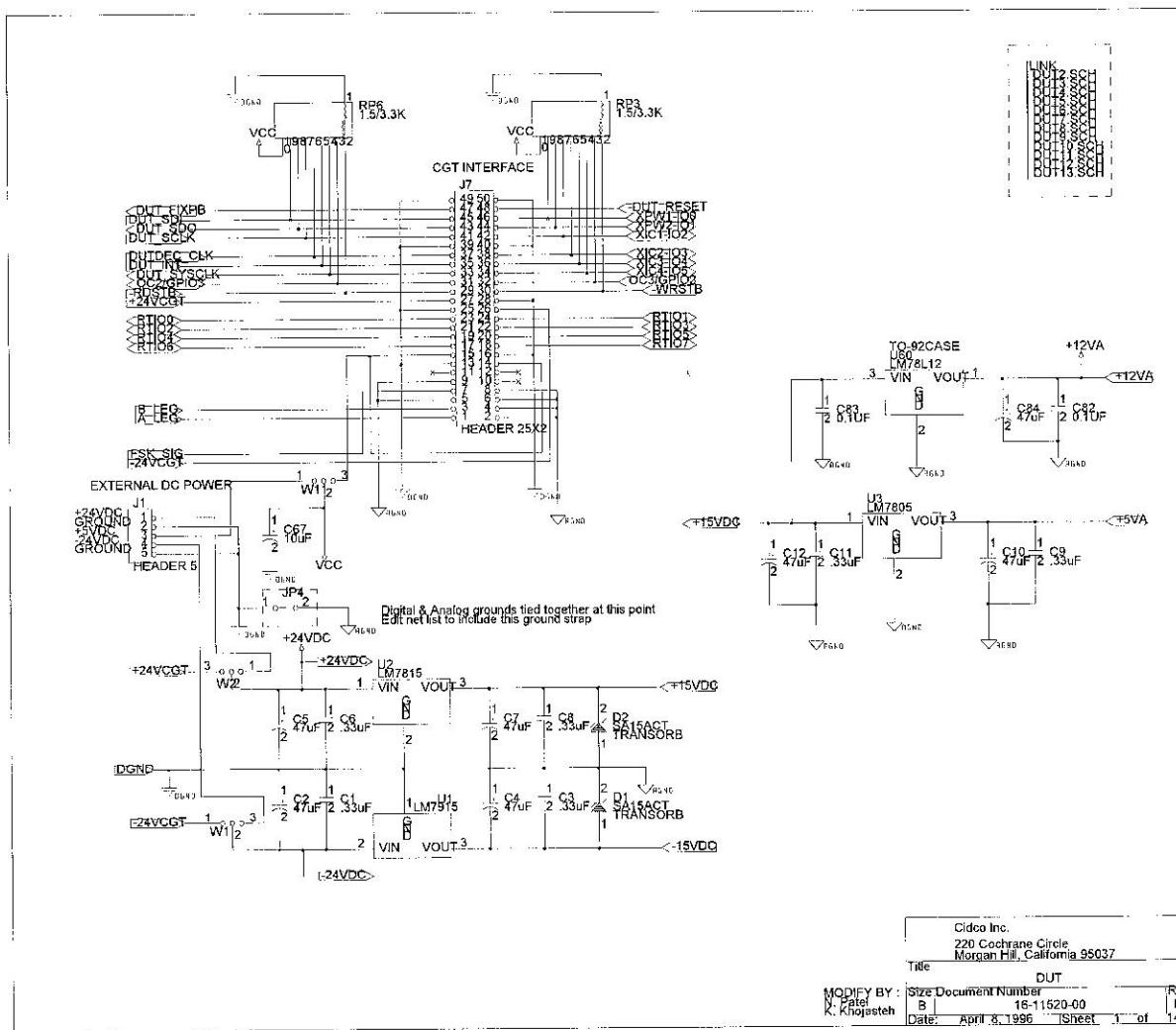
DUT I/F Pin #	Signal Name	Signal Description
J14-9	+HK_SW1	DUT positive hook switch side #1 control
J14-10	-HK_SW1	DUT negative hook switch side #1 control
J14-11	+HK_SW2	DUT positive hook switch side #2 control
J14-12	-HK_SW2	DUT negative hook switch side #2 control

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1.4 Daughter Card Schematics

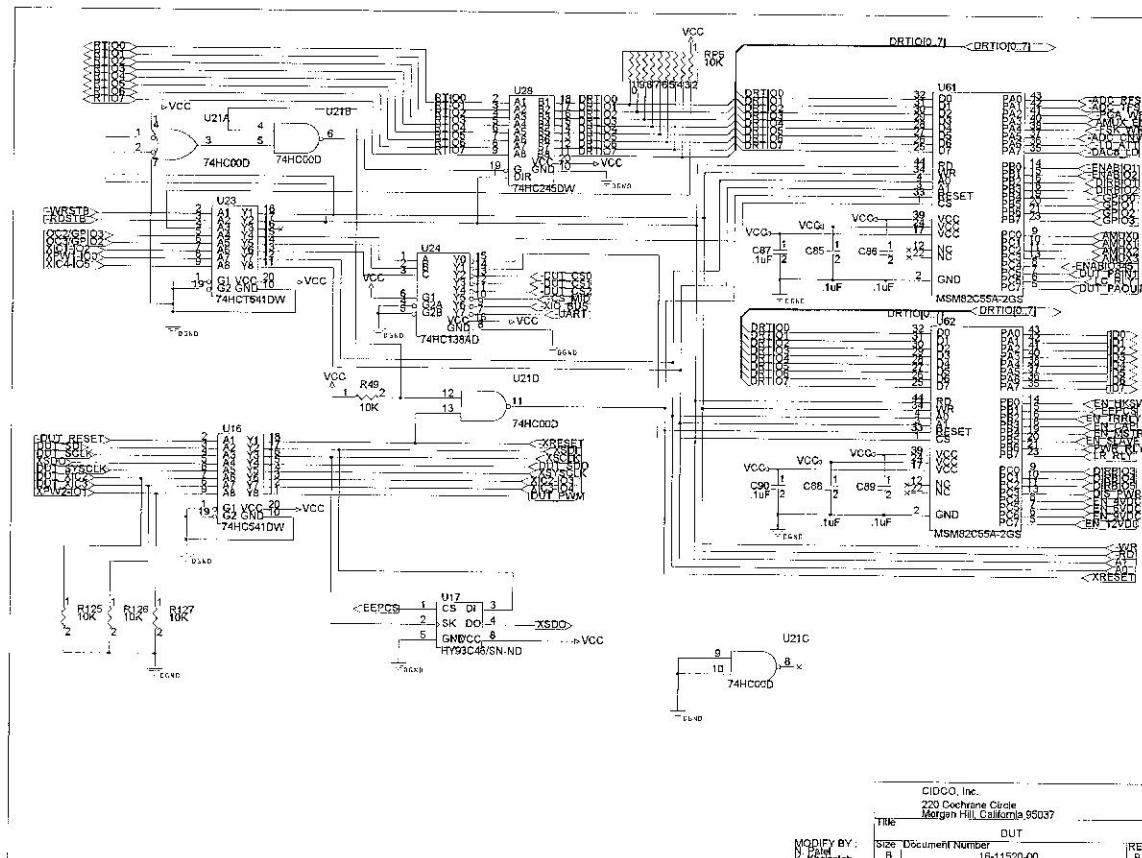
1.4.1 Sheet 1 of the schematics: CGT Interface and power supplies



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1.4.2 Sheet 2 of the schematics: CGT interface buffers, Address decode, EEPROM and Housekeeping Control Ports.

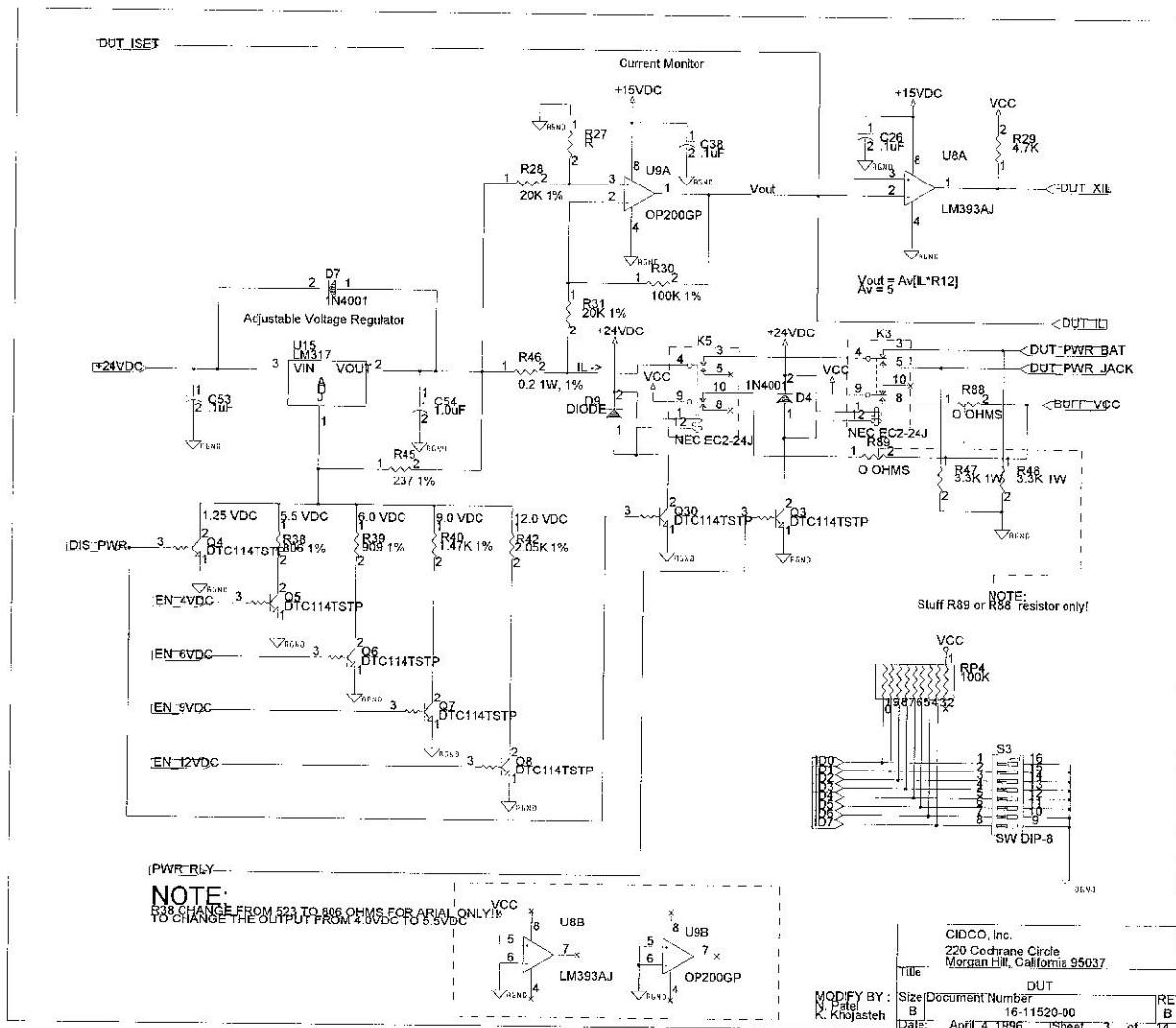


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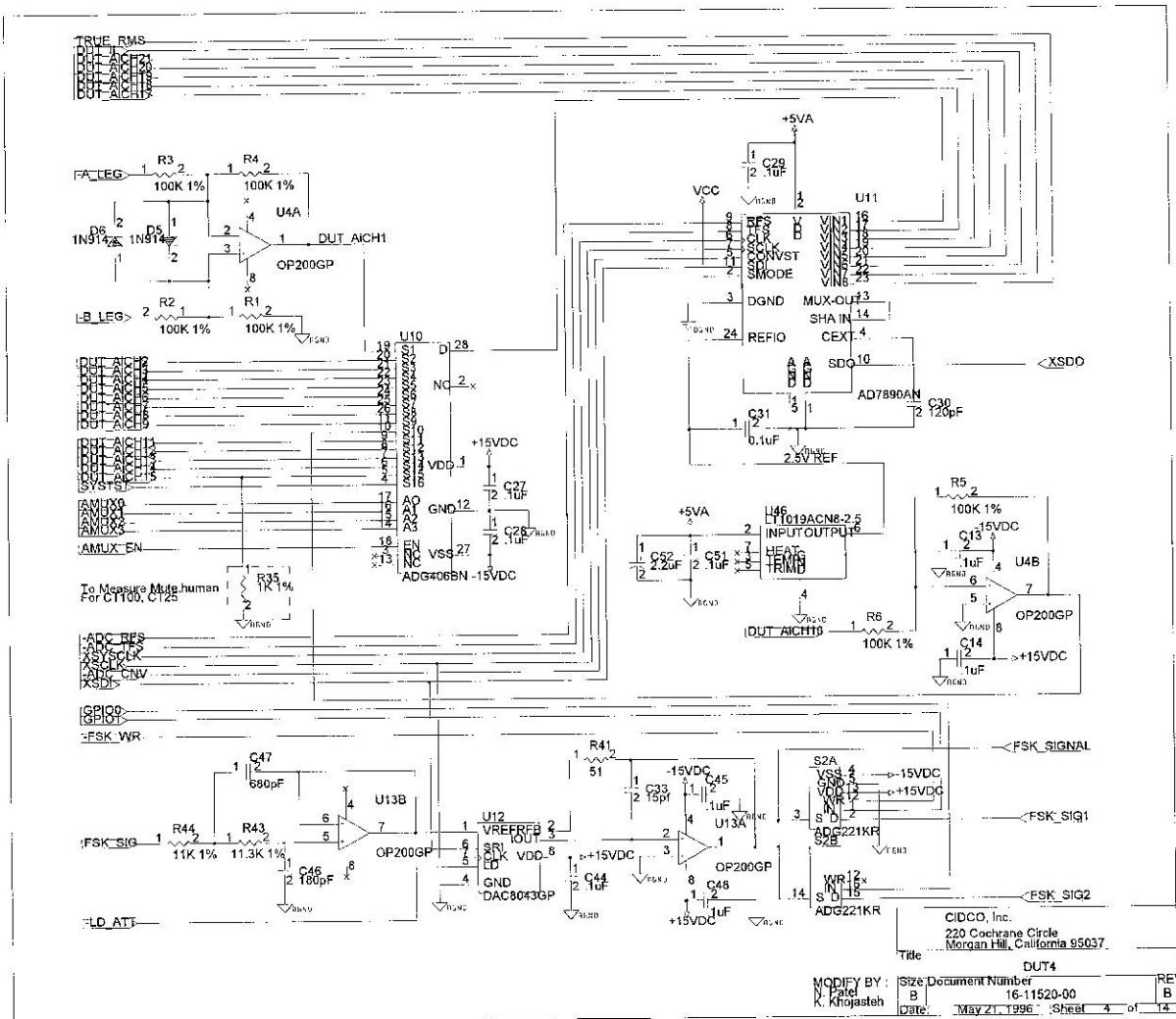
1.4.3 Sheet 3 of the schematics: Programmable DUT Power Supply and Current Monitor.



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1.4.4 Sheet 4 of the schematics: 8-channel/12-bit serial analog to digital converter, 16-channel single-ended analog multiplexer and a three channel FSK signal attenuator with two switched outputs.



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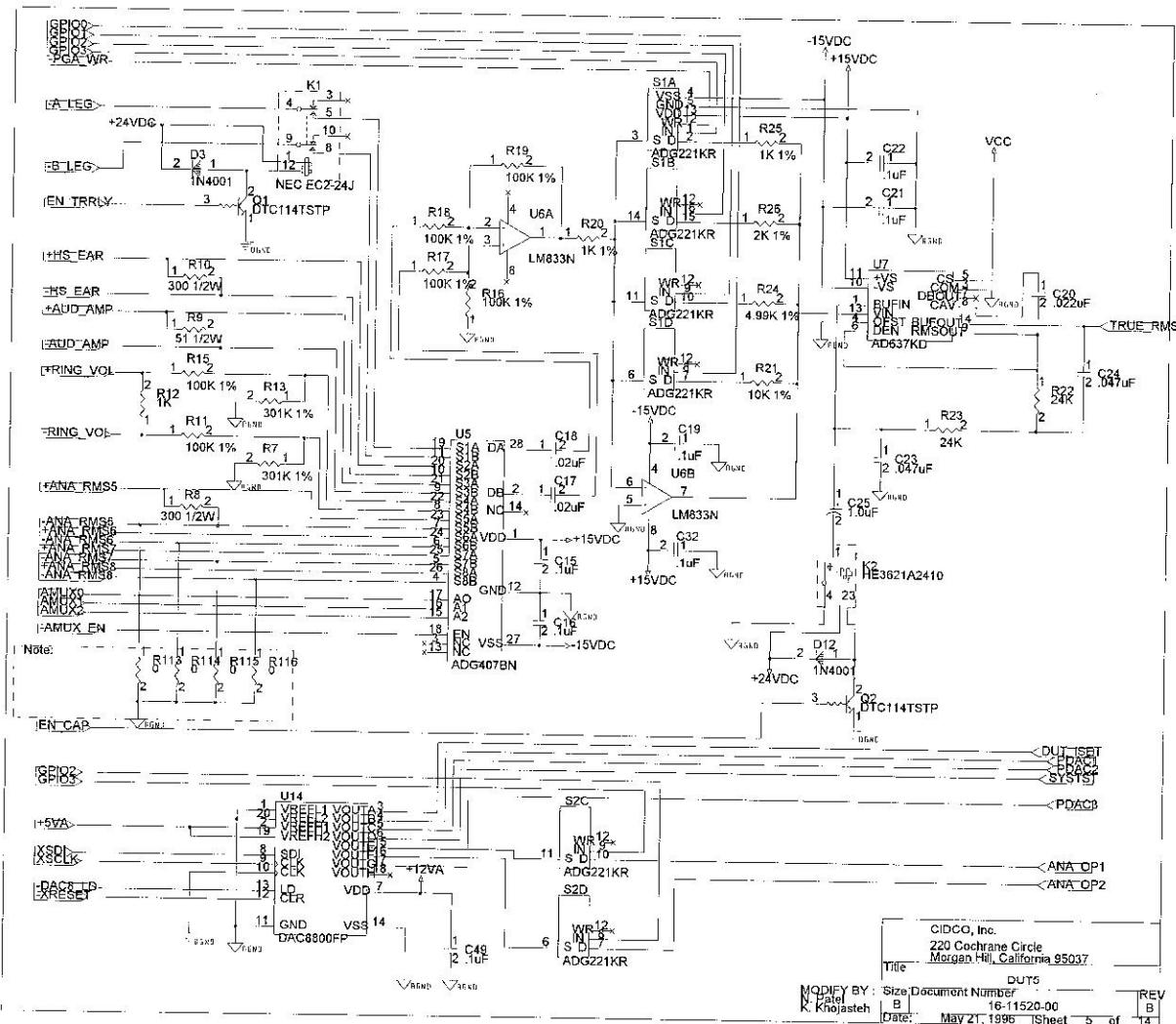
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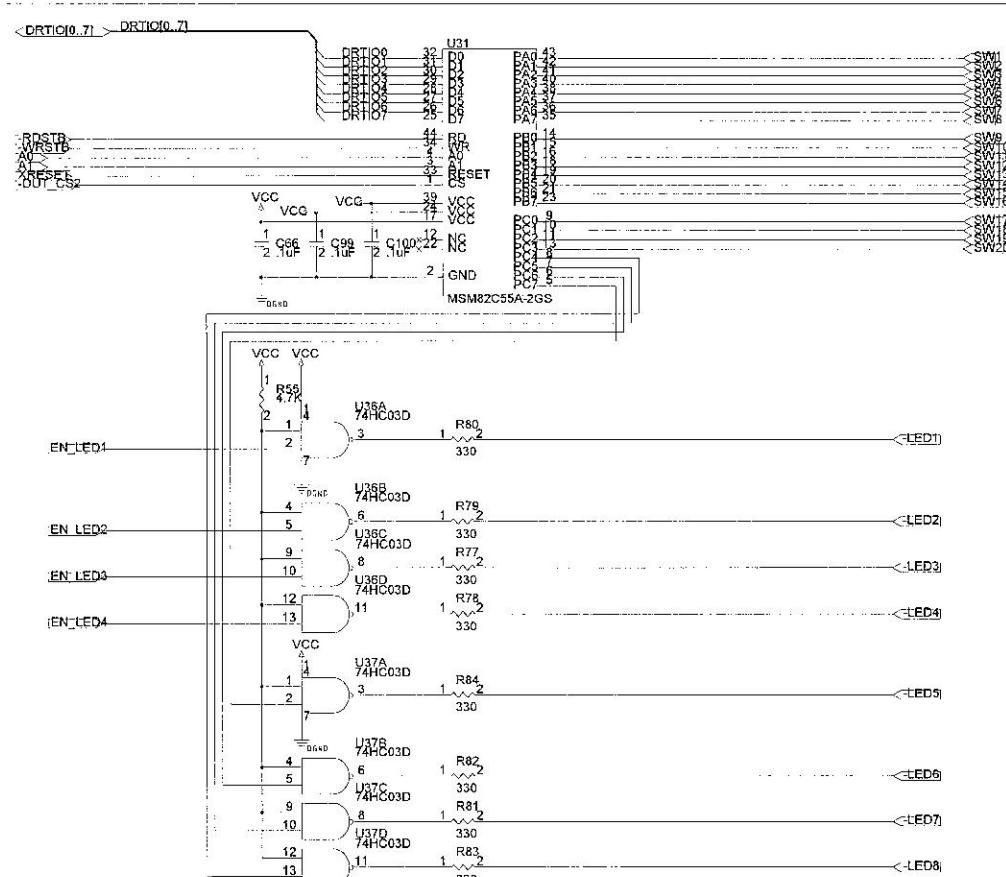
1.4.5 Sheet 5 of the schematics: 8-channel analog multiplexer, differential to single-ended converter, programmable gain stage, RMS to DC converter and a 4-channel DAC with two switched outputs.



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1.4.6 Sheet 6 of the schematics: Key matrix control port and an eight channel LED driver ports.



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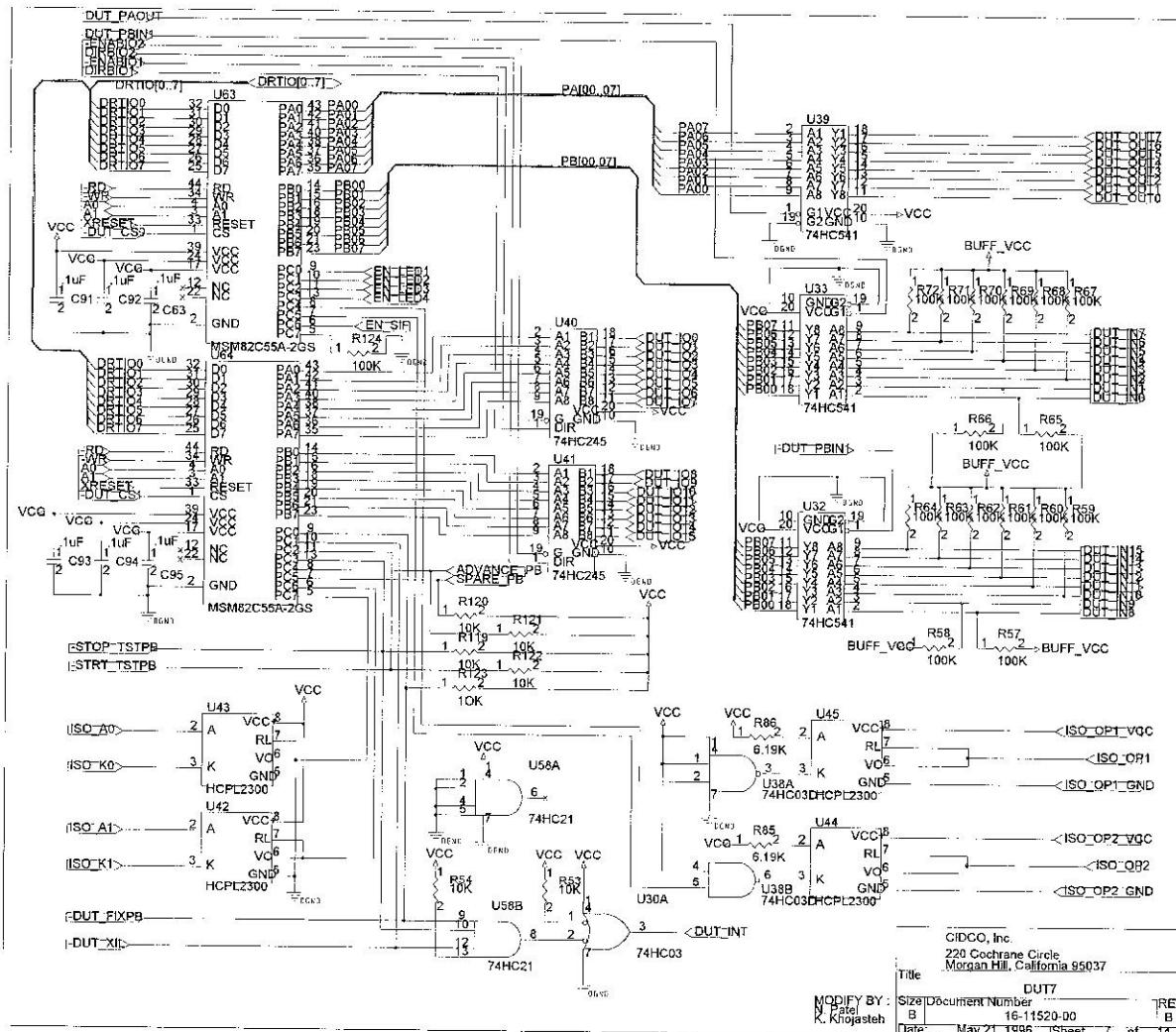


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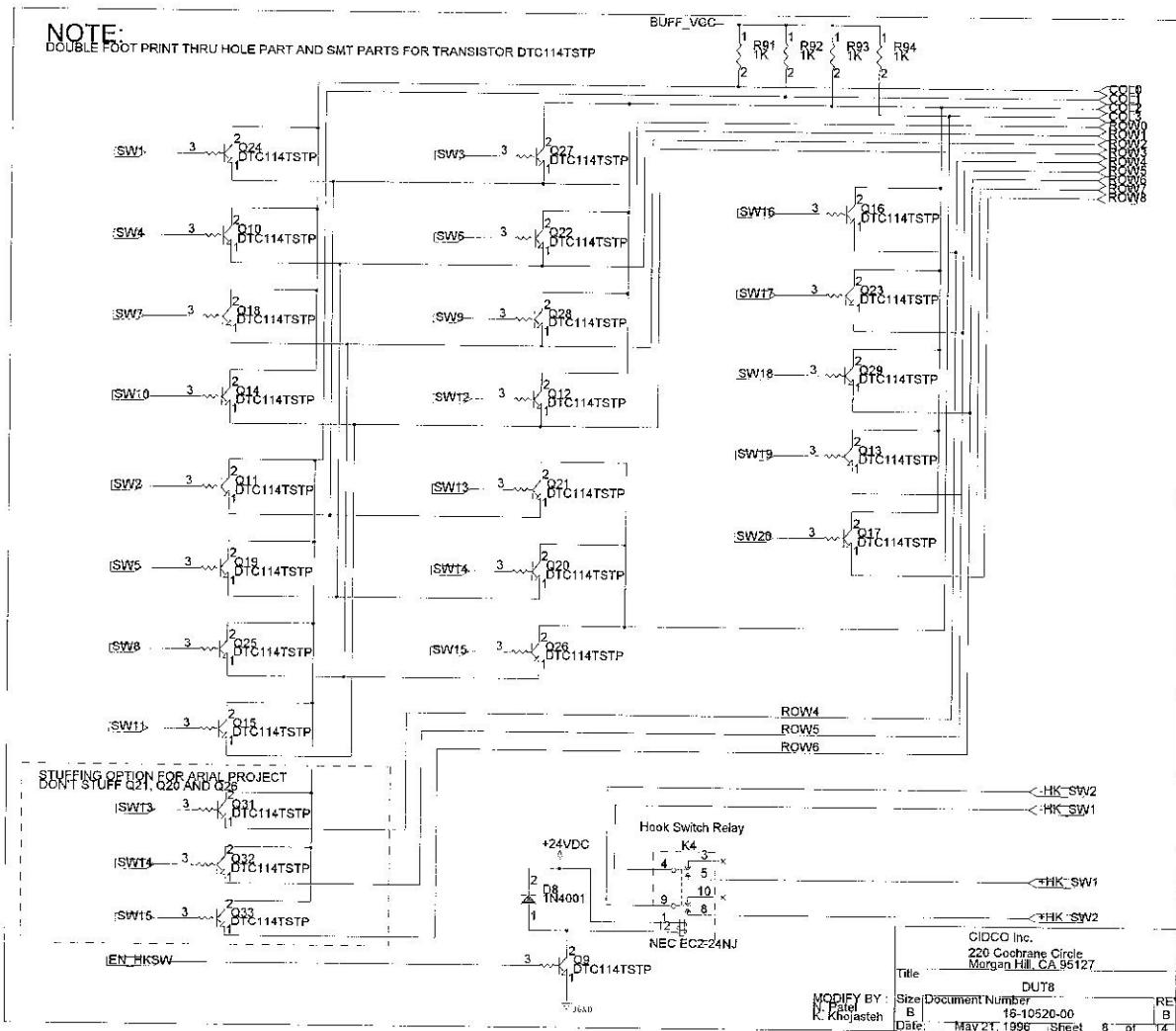
1.4.7 Sheet 7 of the schematics: DUT input/output output interface control port, DUT interface output and input buffers, dual input and output opto-isolated ports, fixture switches and pushbutton scan port and an external interrupt port.



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1.4.8 Sheet 8 of the schematics: DUT key matrix electrical switches and an electrical hook switch control.





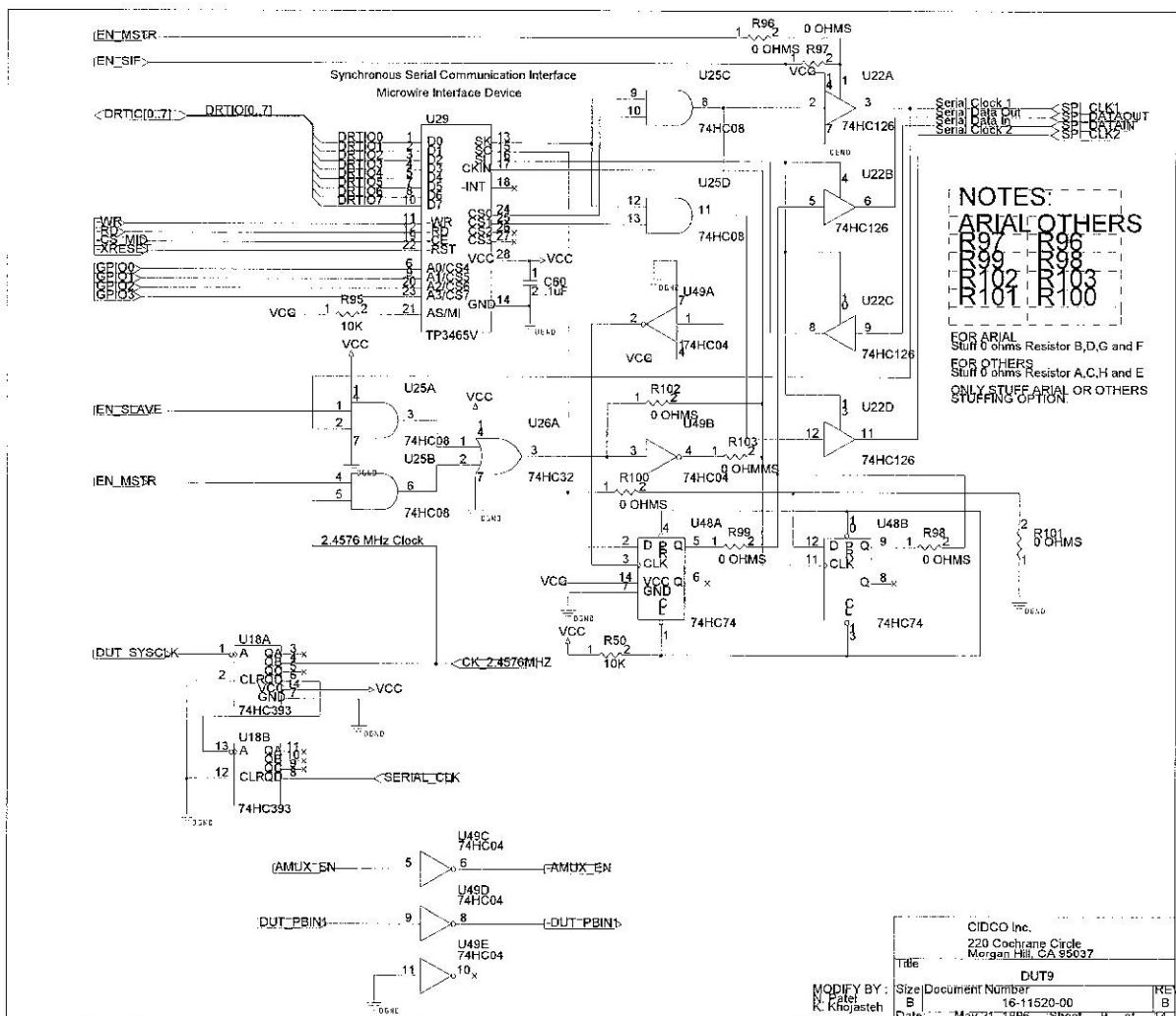
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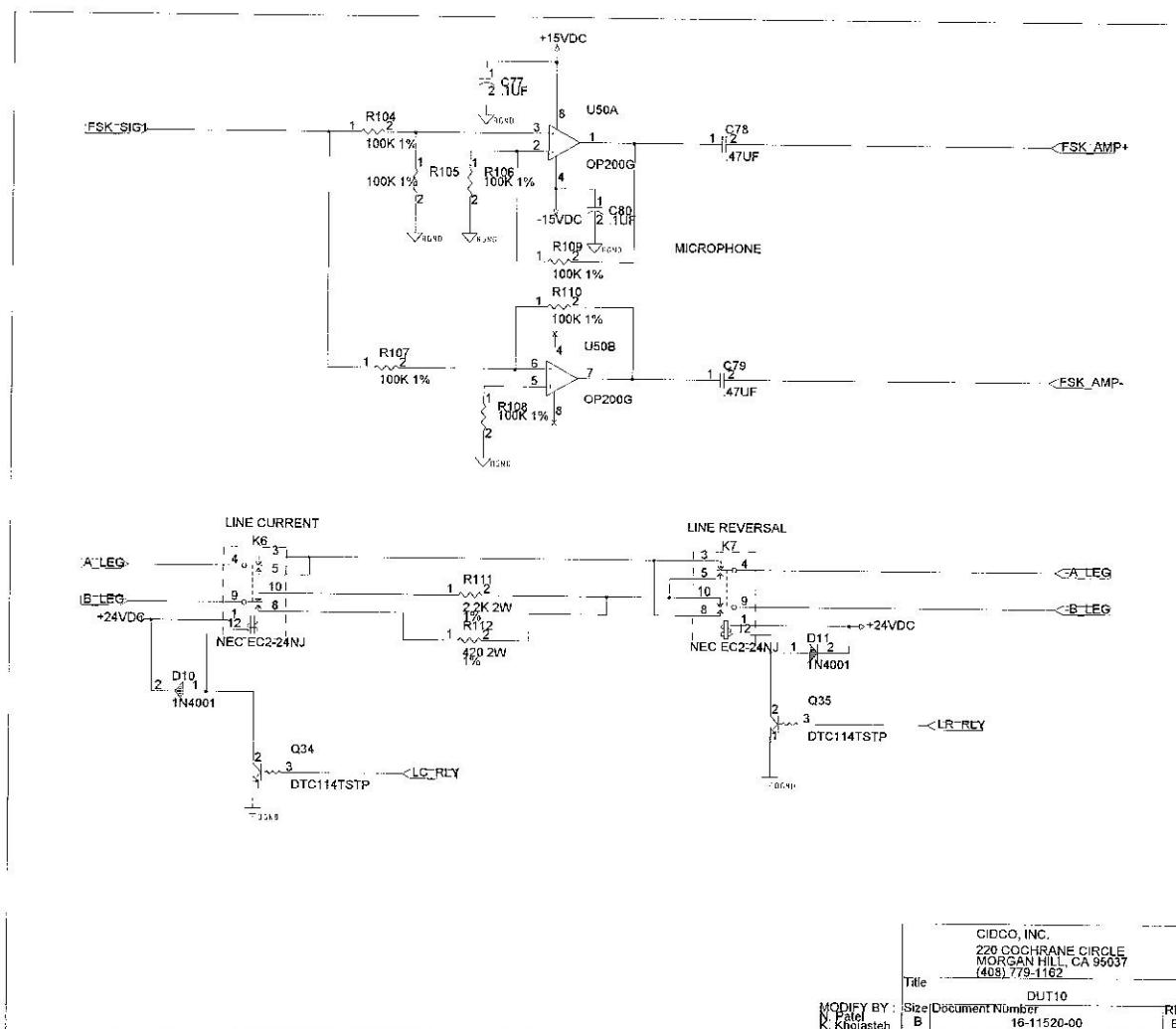
1.4.9 Sheet 9 of the schematics: DUT serial communications interface port.



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1.4.10 Sheet 10 of the schematics: FSK single-ended to differential driver stage, a line current switching relay and a line reversal relay.



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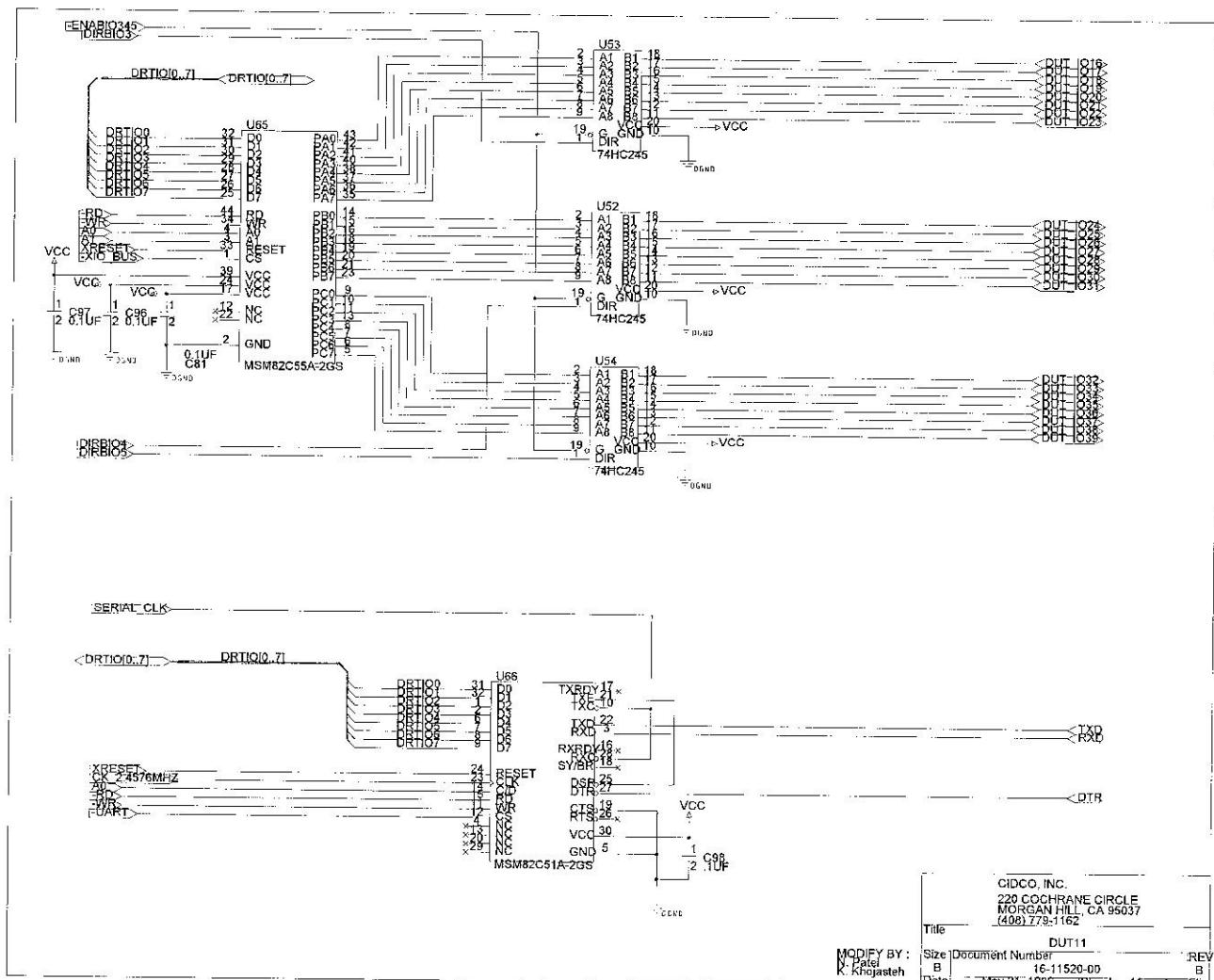
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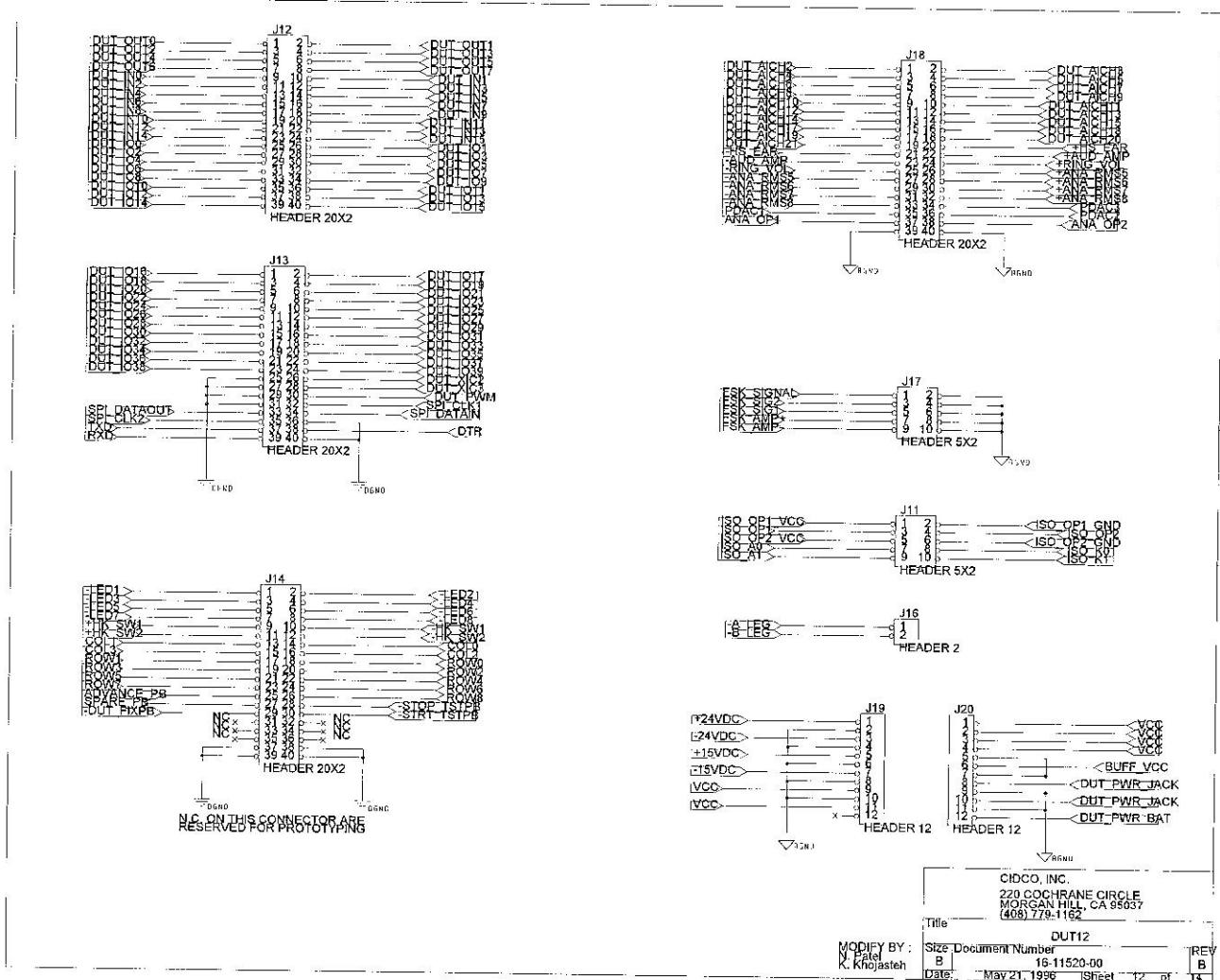
1.4.11 Sheet 11 of the schematics: DUT input/output control port with three interface buffers and a UART (asynchronous serial interface) controller.



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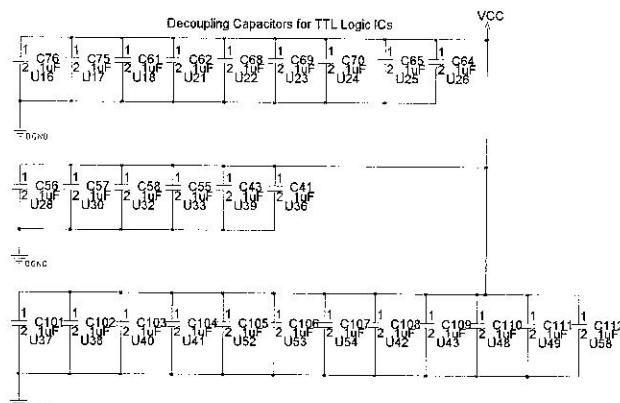
1.4.12 Sheet 12 of the schematics: DUT interface interconnects.



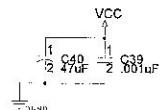
**CGT TESTER DAUGHTER CARD
HARDWARE DESIGN SPECIFICATION**

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1.4.13 Sheet 13 of the schematics: Decoupling capacitors.



ALL BYPASS CAPS ARE SMT-1206 CASE



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