

Environment Setup for Vivado

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What is vivado?

- **Vivado is software developed by Xilinx**
- **Vivado is used for FPGA design, development, and programming**
- **Vivado is widely used in industries and academia for developing FPGA-based solutions**

Download Vivado

- You can download Vivado via AMD XILINX Homepage
<https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools.html>
- Recommend downloading the Vivado ML Edition (2023.1)
 - To download it, you will need to sign up
 - Windows Version Installer
 - Linux Version installer

AMD Unified Installer for FPGAs & Adaptive SoCs 2023.1: Windows Self Extracting Web Installer (EXE - 199.47 MB)

MD5 SUM Value : 4c6a1e5d5cf7c44c3f201c9056b6cf45

Download Verification ⓘ

Digests

Signature

Public Key

AMD Unified Installer for FPGAs & Adaptive SoCs 2023.1: Linux Self Extracting Web Installer (BIN - 265.94 MB)

MD5 SUM Value : e47ad71388b27a6e2339ee82c3c8765f

Download Verification ⓘ

Digests

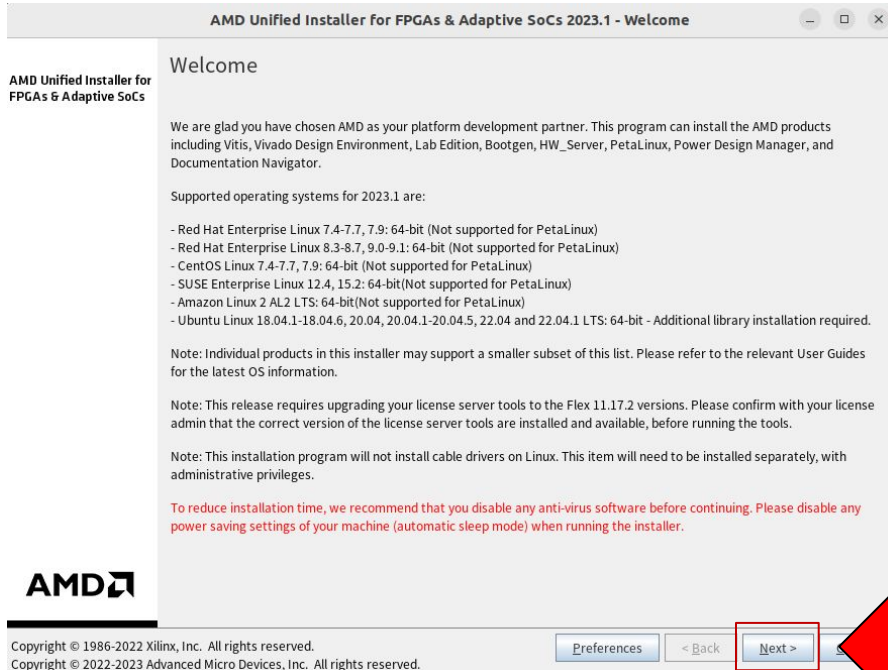
Signature

Public Key

Install Vivado (Linux / Windows)

```
$> chmod +x Xilinx_XXX_xxx.bin
```

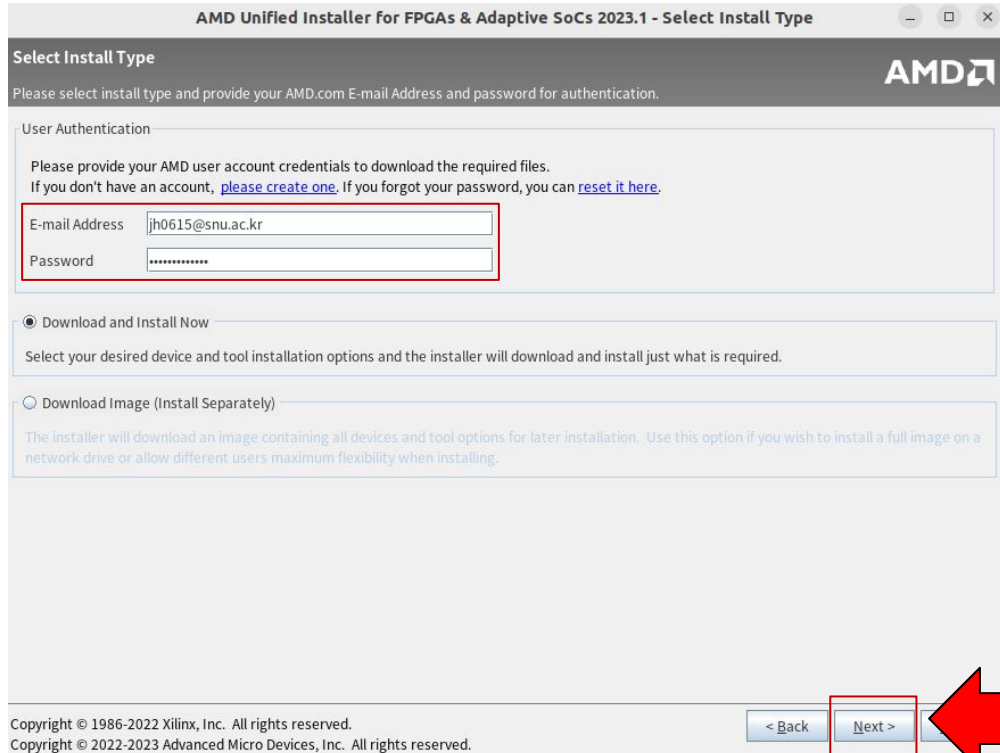
```
$> ./Xilinx_XXX_xxx.bin
```



Click Next Button

Install Vivado (Linux / Windows)

Use the email address and password used **when signing up**



AMD Unified Installer for FPGAs & Adaptive SoCs 2023.1 - Select Install Type

Select Install Type

Please select install type and provide your AMD.com E-mail Address and password for authentication.

User Authentication

Please provide your AMD user account credentials to download the required files.
If you don't have an account, [please create one](#). If you forgot your password, you can [reset it here](#).

E-mail Address

Password

☒ Download and Install Now

Select your desired device and tool installation options and the installer will download and install just what is required.

☐ Download Image (Install Separately)

The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.

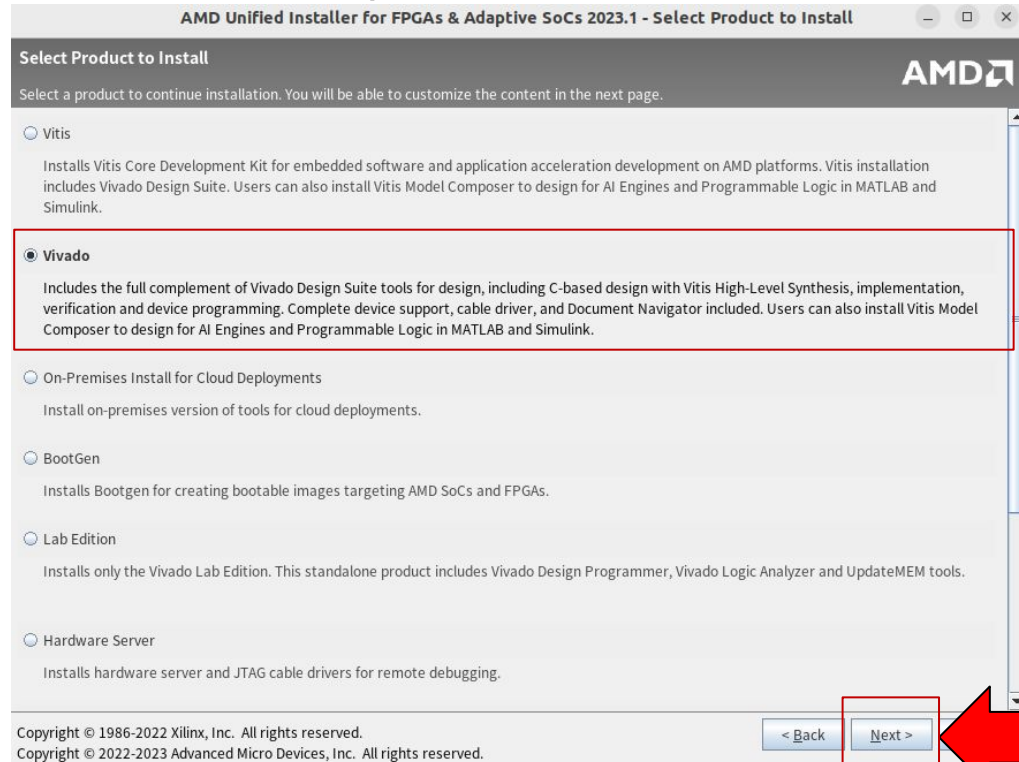
Copyright © 1986-2022 Xilinx, Inc. All rights reserved.
Copyright © 2022-2023 Advanced Micro Devices, Inc. All rights reserved.

< Back Next >

Then, Click Next Button

Install Vivado (Linux / Windows)

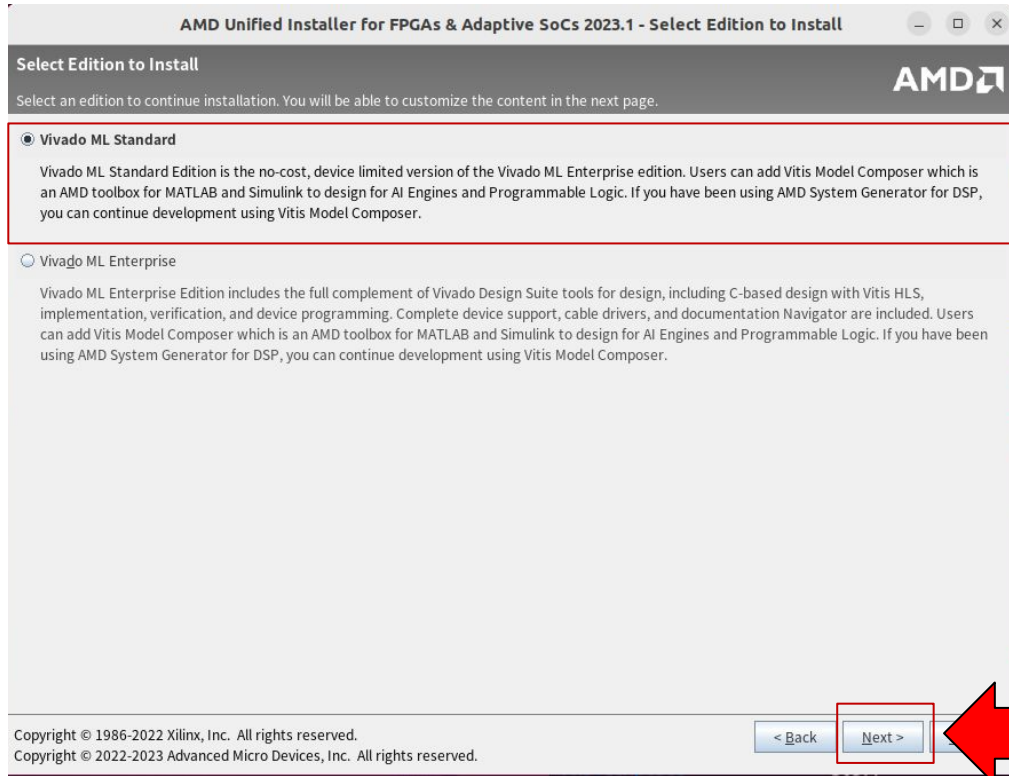
Select **vivado** as product to install



Then, Click Next Button

Install Vivado (Linux / Windows)

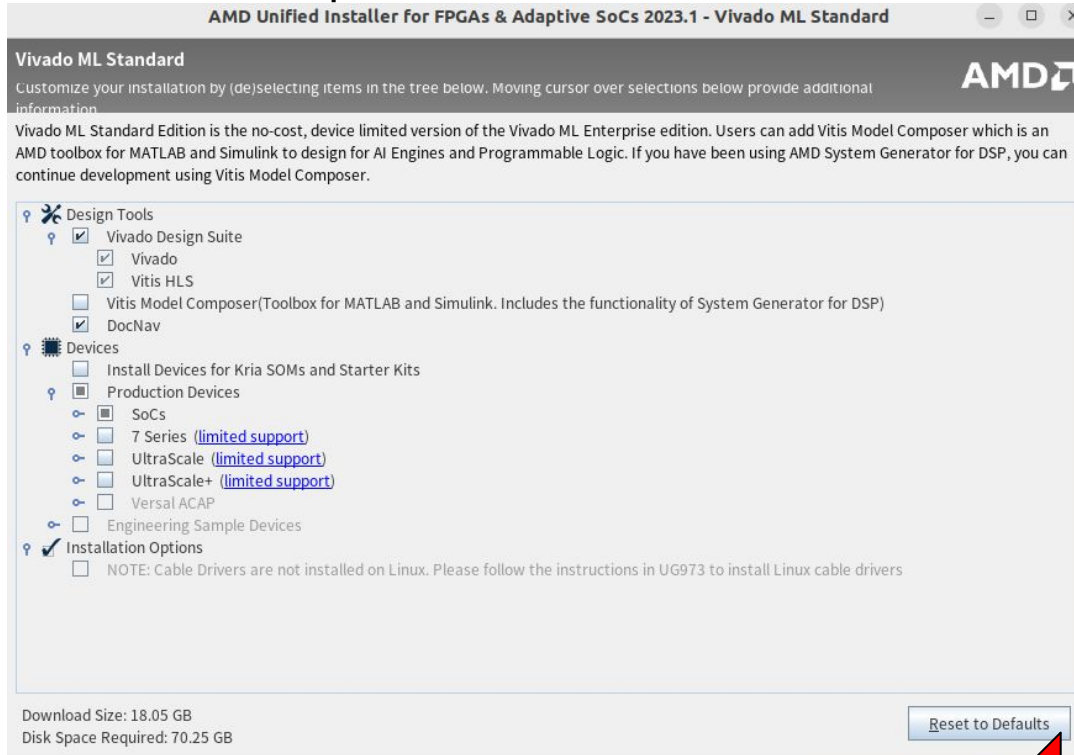
Select **vivado ML Standard** edition



Then, Click Next Button

Install Vivado (Linux / Windows)

Select minimal option to install

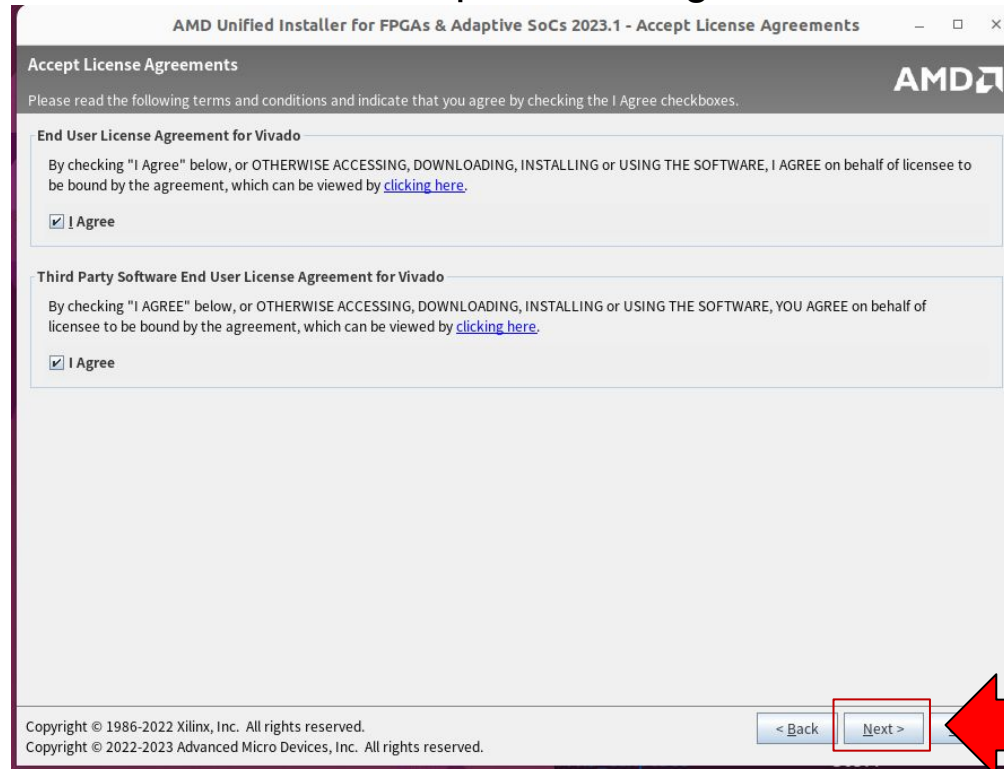


< Back Next >

Then, Click Next Button

Install Vivado (Linux / Windows)

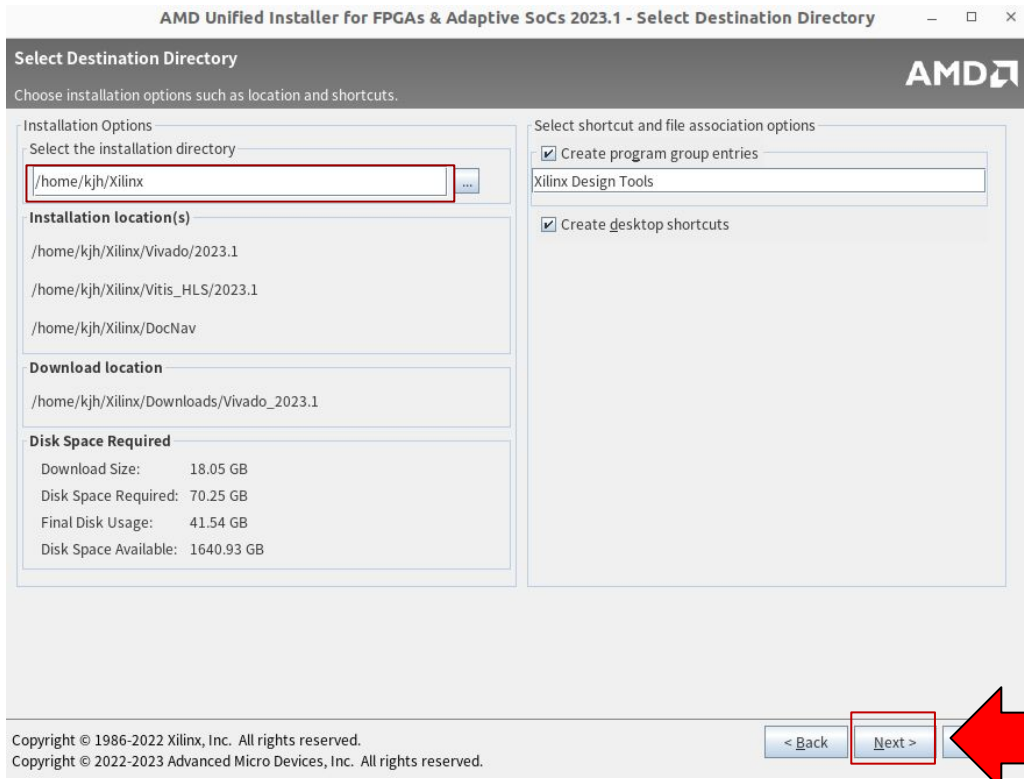
Please check for accept license agreements



Then, Click Next Button

Install Vivado (Linux / Windows)

Recommend to change installation directory path.



Then, Click Next Button

Install Vivado (Linux / Windows)

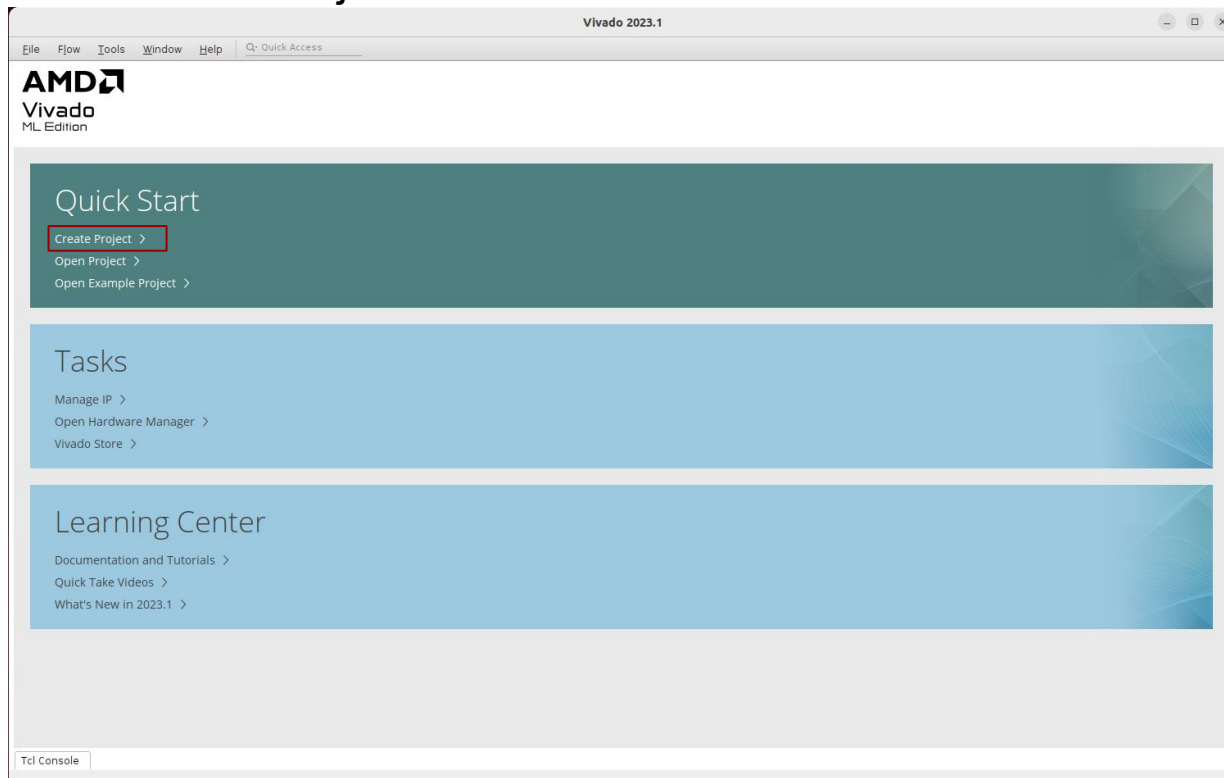
Please reserve required space for installation



Then, Click Install Button

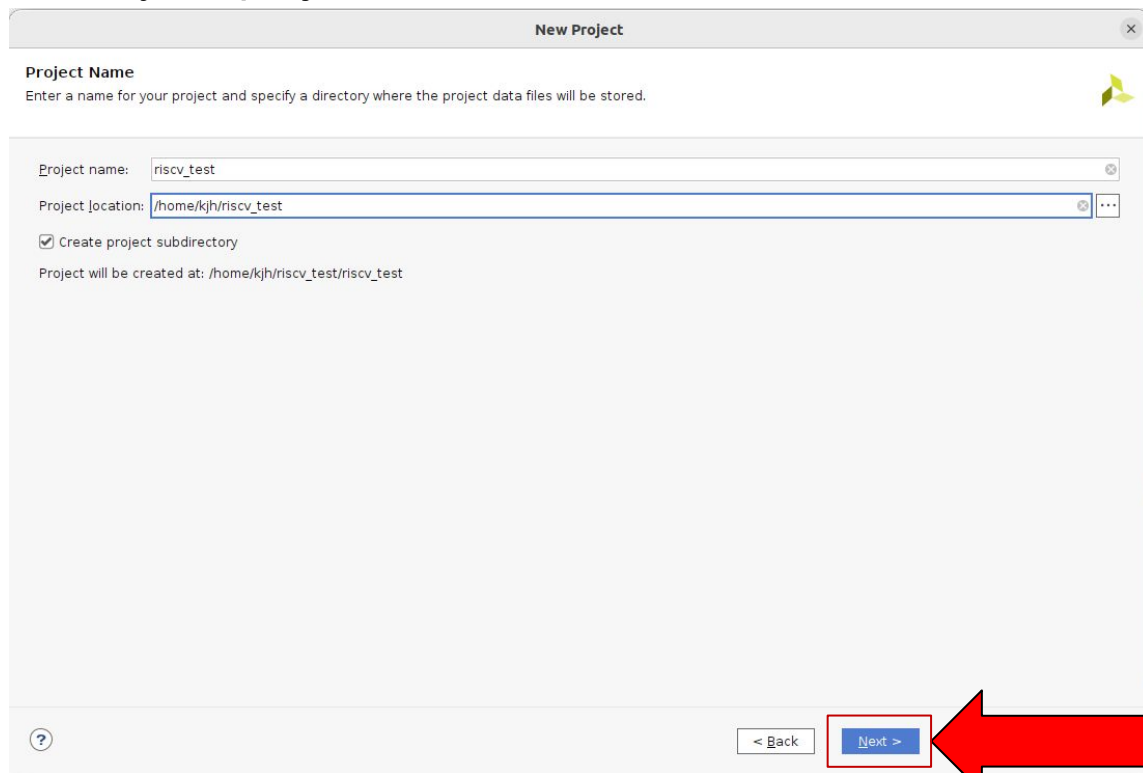
Create Project

Click Create Project



Create Project

Enter your project name



New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name: riscv_test

Project location: /home/kjh/riscv_test

☒ Create project subdirectory

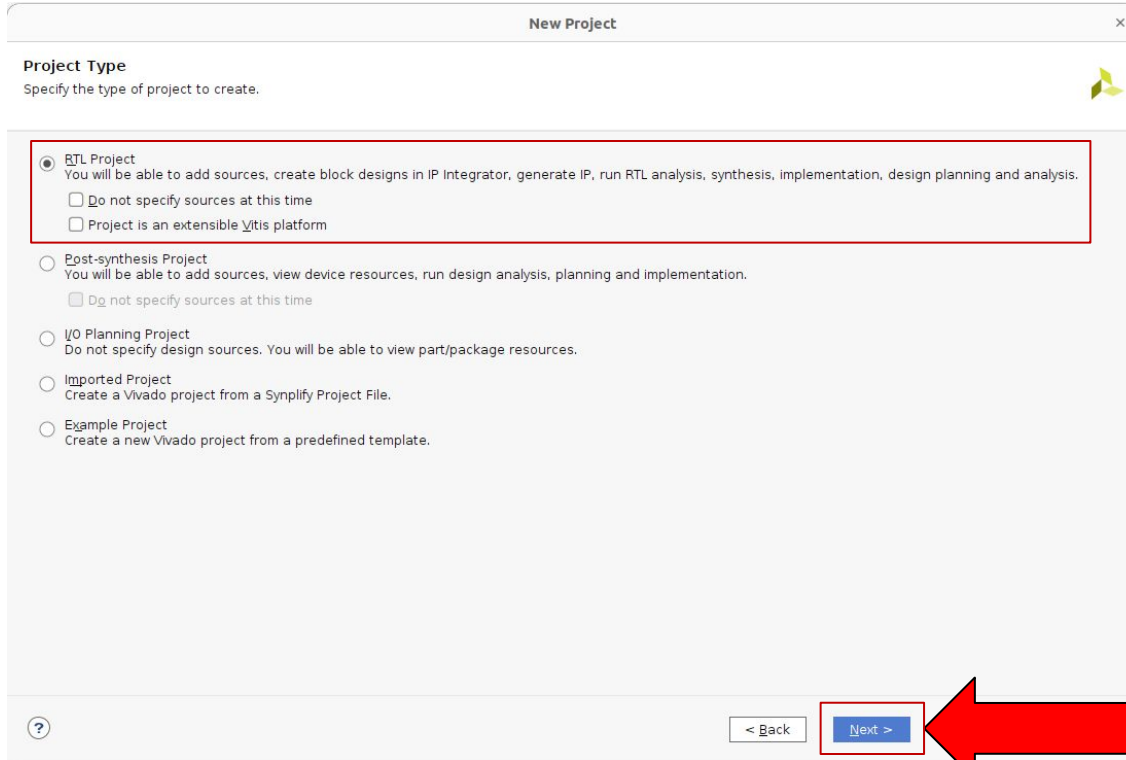
Project will be created at: /home/kjh/riscv_test/riscv_test

? < Back Next >

Then, Click Next Button

Create Project

Select RTL Project Type



New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☐ Do not specify sources at this time
☐ Project is an extensible Vitis platform

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify Project File.

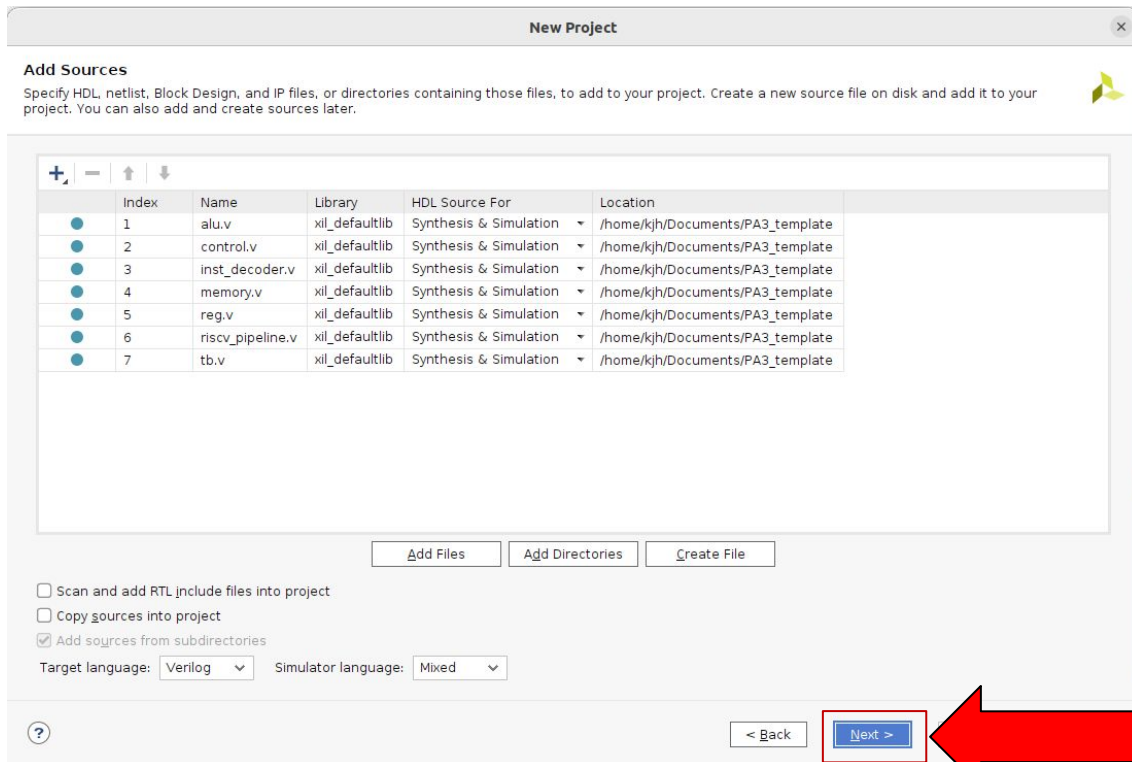
☐ **Example Project**
Create a new Vivado project from a predefined template.

? < Back Next >

Then, Click Next Button

Create Project

Add source files you need (You can add to the project after it's created)



New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

	Index	Name	Library	HDL Source For	Location
●	1	alu.v	xil_defaultlib	Synthesis & Simulation	/home/kjh/Documents/PA3_template
●	2	control.v	xil_defaultlib	Synthesis & Simulation	/home/kjh/Documents/PA3_template
●	3	inst_decoder.v	xil_defaultlib	Synthesis & Simulation	/home/kjh/Documents/PA3_template
●	4	memory.v	xil_defaultlib	Synthesis & Simulation	/home/kjh/Documents/PA3_template
●	5	reg.v	xil_defaultlib	Synthesis & Simulation	/home/kjh/Documents/PA3_template
●	6	riscv_pipeline.v	xil_defaultlib	Synthesis & Simulation	/home/kjh/Documents/PA3_template
●	7	tb.v	xil_defaultlib	Synthesis & Simulation	/home/kjh/Documents/PA3_template

☐ Scan and add RTL include files into project

☐ Copy sources into project

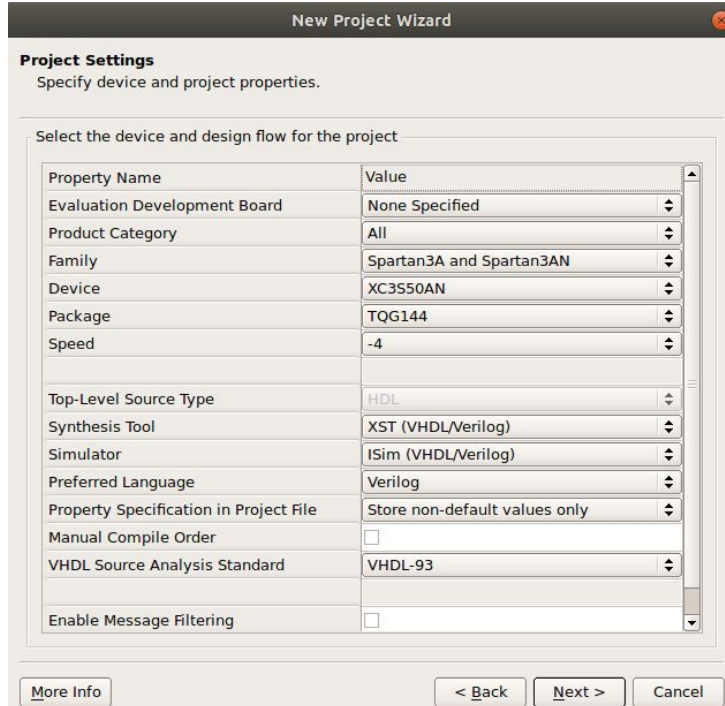
☒ Add sources from subdirectories

Target language: Verilog Simulator language: Mixed

Then, Click Next Button

Create Project (Xilinx ISE)

If you want to use Xilinx ISE Program, create project using the following method



The screenshot shows the 'New Project Wizard' dialog box in Xilinx ISE, specifically the 'Project Settings' step. The title bar reads 'New Project Wizard'. Below the title bar, the text 'Project Settings' is followed by the instruction 'Specify device and project properties.'.

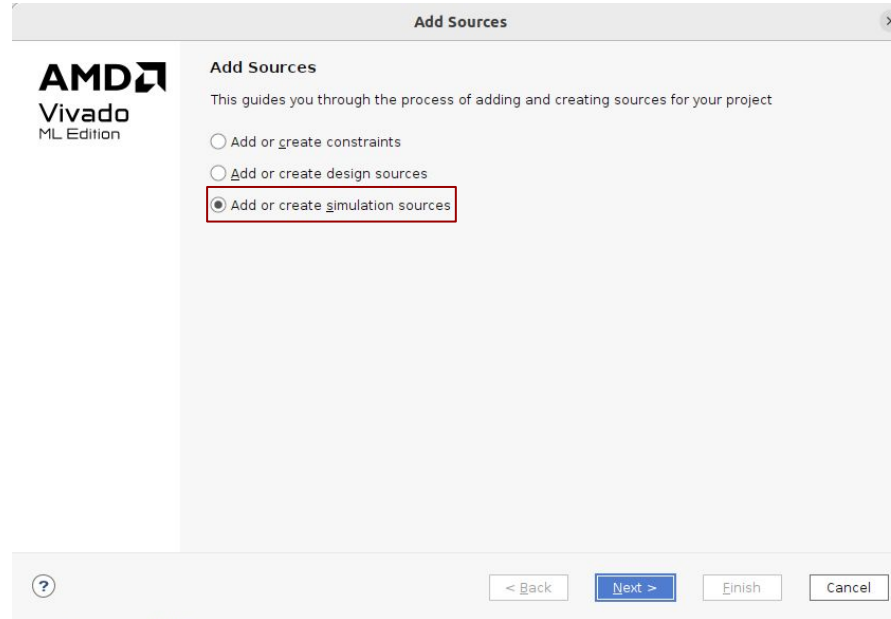
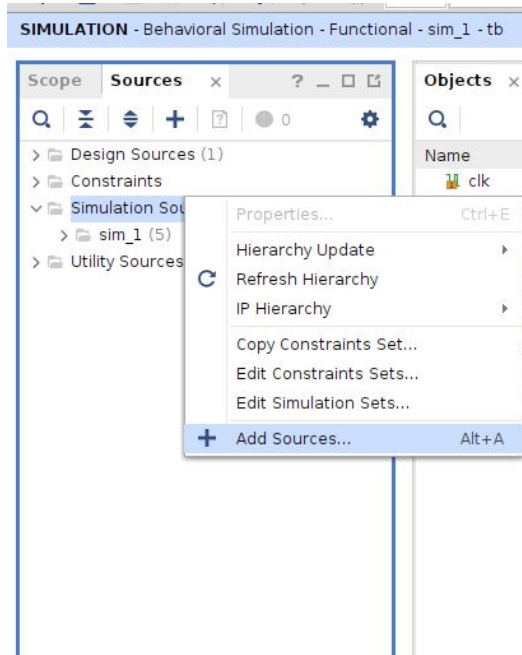
The main area is titled 'Select the device and design flow for the project'. It contains a table with two columns: 'Property Name' and 'Value'.

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3A and Spartan3AN
Device	XC3S50AN
Package	TQG144
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store non-default values only
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

At the bottom of the dialog box, there are four buttons: 'More Info', '< Back', 'Next >', and 'Cancel'.

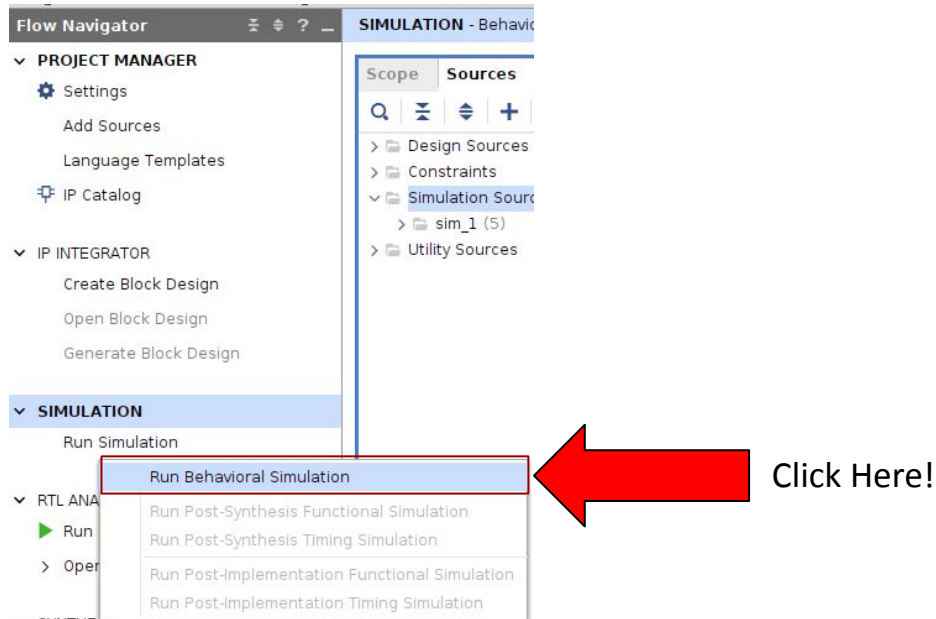
Add Files to project

To access the provided sample data file, you need to add it to the project.



Running Simulation

Click Run Behavioral Simulation to start simulation



Running Simulation

You can check result via console and waveform

The screenshot shows the Xilinx Vivado IDE interface during a simulation. The left pane, titled 'Tcl Console', displays the following log messages:

```
Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
Copyright 2022-2023 Advanced Micro Devices, Inc. All Rights Reserved.
Running: /home/kjh/Xilinx/Vivado/2023.1/bin/unwrapped/launch.sh
Using 8 slave threads.
Starting static elaboration
Pass Through NonSizing Optimizer
Completed static elaboration
INFO: [XSIM 43-4323] No Change in HDL. Linking previous
INFO: [USF-XSim-69] 'elaborate' step finished in '1' seconds
Time resolution is 1 ps
WARNING: Too many words specified in data file bit.dat
reg[ 1] = 0x0ff00113
reg[ 2] = 0x000000ff
reg[ 3] = 0x00000084
reg[ 4] = 0x00000000
reg[ 5] = 0x00000000
reg[ 6] = 0x00000000
reg[ 7] = 0x00000000
M[ 1] = 0x00000000
M[ 2] = 0x00000000
M[ 3] = 0x00000000
M[ 4] = 0x00000000
```

The right pane shows a waveform viewer with three signals: `clk`, `reset`, and `data_out[31:0]`. The `clk` signal is a periodic square wave. The `reset` signal is a single pulse. The `data_out[31:0]` signal shows the output data, with values `00803083`, `Off...`, and `084...` visible. The waveform is plotted against time from 0.000 ns to 60.0 ns.