6 MMC/SD SPI protocol

6.1 Initialization procedure

After power on reset, MMC/SDC enters are native operating modes.

The card will enter SPI mode if the CS signal is low during the reception of the reset command (CMD0) and it will respond with SPI mode R1 response.

The only way to return to the multimedia card mode is by a power cycle (turn the power off and on).

Since CMD0 has no arguments, the content of all the fields plus the CRC (not calculated by the card) field are constant.

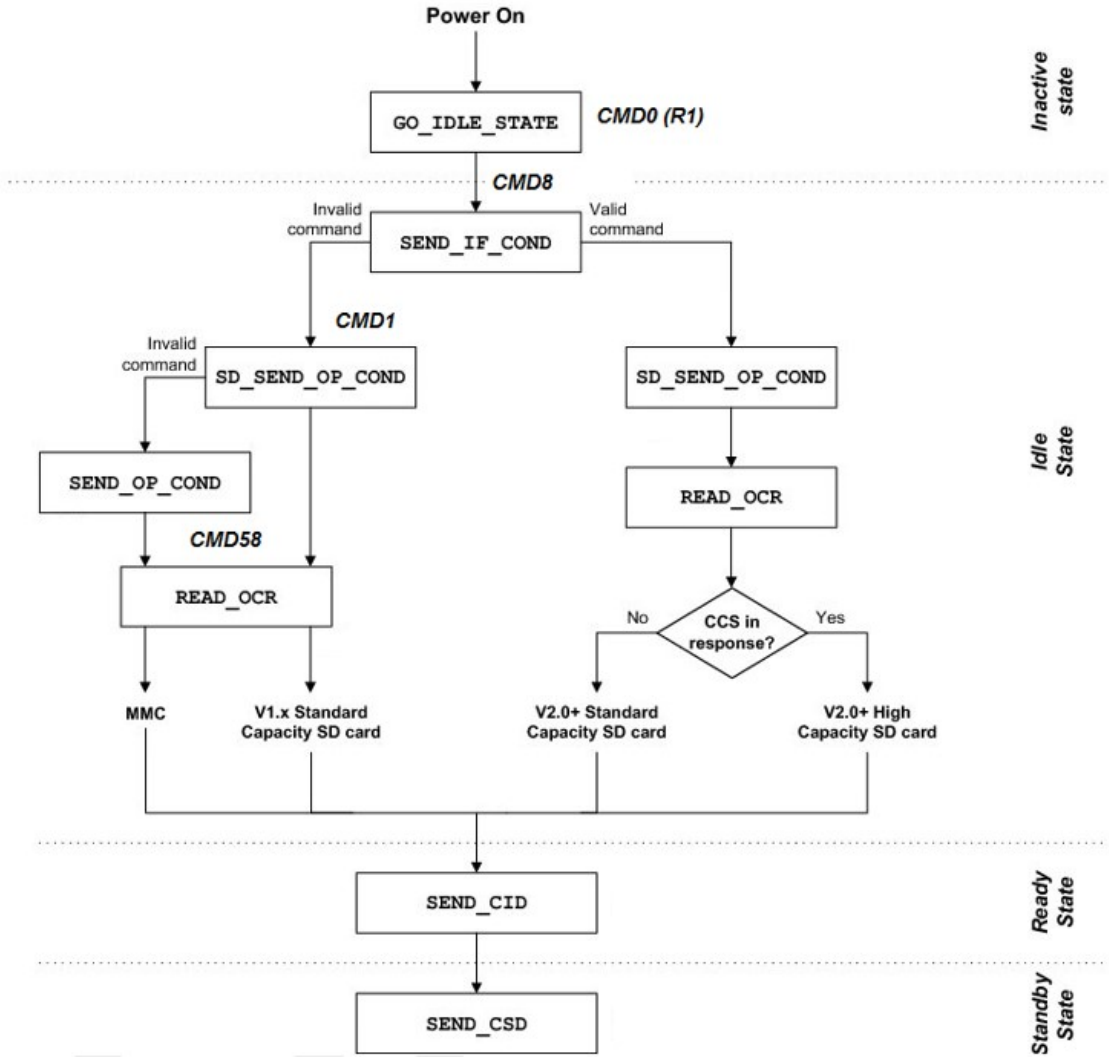
Reset command:`0x40, 0x0, 0x0, 0x0, 0x0, 0x95`

In idle state, the card accepts only CMD0, CMD1, ACMD41, CMD58 and CMD59.

Note that all cards work at supply voltage range of 2.7 to 3.6 V at least, so that the host controller doesn't need to check the OCR if the supply voltage is in this range.

In SPI mode the CMD1 has no operands and does not return the contents of the OCR register. Instead, the host may use CMD58 (only in SPI mode) to read the OCR.

Figure 4. Example of initialization flow chart



6.2 Clock control

The SPI bus clock signal can be used to put the card into energy saving mode or to control the data flow.

There are a few restrictions the SPI host must follow:

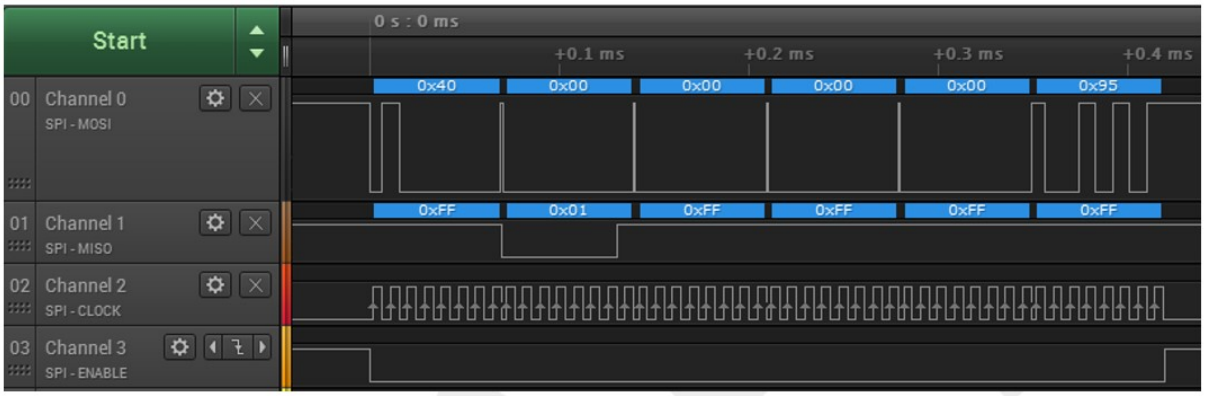
- The frequency can be changed at any time
- After the last SPI bus transaction, the host is required to provide 8 clock cycles for the card to complete the operation before shutting down the clock.
- A command / response sequence, 8 clocks after the card response end bit. The CS signal can be asserted or de-asserted during these 8 clocks.
- A read data transaction, 8 clocks after the end bit of the last data block.
- A write data transaction, 8 clocks after the CRC status token.
- The host can shut down the clock of a “busy” card

6.3 CMD0 and R1 response

Host controller sends the CMD0 reset command:

`0x40, 0x0, 0x0, 0x0, 0x0, 0x95`

Figure 5. CMD0 reset command



Card R1 response: `0x1 (IDLE_STATE)`

Figure 6. R1 response