Recommended PSoC Pin Mapping

Pinouts

The following is the pin-list for the PSoC 4200. Port 2 comprises of the high-speed Analog inputs for the SAR Mux. P1.7 is the optional external input and bypass for the SAR reference. Ports 3 and 4 contain the Digital Communication channels. All pins support CSD Capsense and Analog Mux Bus connections.

Pins		44-TQFP	40-QFN		28-SSOP		Alternate Functions for Pins					Pin Description
Name	Type	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
VSSD	Power	1(DN)	VSS	DN	–	DN	–	–	–	–	–	–	Digital Ground
P2.0	GPIO	2	P2.0	1	P2.0	–	–	sarmux.0	–	–	–	–	Port 2 Pin 0: gpio, lcd, csd, sarmux
P2.1	GPIO	3	P2.1	2	P2.1	–	–	sarmux.1	–	–	–	–	Port 2 Pin 1: gpio, lcd, csd, sarmux
P2.2	GPIO	4	P2.2	3	P2.2	5	P2.2	sarmux.2	–	–	–	–	Port 2 Pin 2: gpio, lcd, csd, sarmux
P2.3	GPIO	5	P2.3	4	P2.3	6	P2.3	sarmux.3	–	–	–	–	Port 2 Pin 3: gpio, lcd, csd, sarmux
P2.4	GPIO	6	P2.4	5	P2.4	7	P2.4	sarmux.4	tcpwm0_p[1]	–	–	–	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm
P2.5	GPIO	7	P2.5	6	P2.5	8	P2.5	sarmux.5	tcpwm0_n[1]	–	–	–	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm
P2.6	GPIO	8	P2.6	7	P2.6	9	P2.6	sarmux.6	tcpwm1_p[1]	–	–	–	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm
P2.7	GPIO	9	P2.7	8	P2.7	10	P2.7	sarmux.7	tcpwm1_n[1]	–	–	–	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm
–	–	10(DN)	VSS	9(DN)	VSS	–	–	–	–	–	–	–	Package pin to lead frame paddle downbond
P3.0	GPIO	11	P3.0	10	P3.0	11	P3.0	–	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
P3.1	GPIO	12	P3.1	11	P3.1	12	P3.1	–	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
P3.2	GPIO	13	P3.2	12	P3.2	13	P3.2	–	tcpwm1_p[0]	–	swd_io	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
P3.3	GPIO	14	P3.3	13	P3.3	14	P3.3	–	tcpwm1_n[0]	–	swd_clk	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
P3.4	GPIO	15	P3.4	14	P3.4	–	–	–	tcpwm2_p[0]	–	–	scb1_spi_ssel_1	Port 3 Pin 4: gpio, lcd, csd, pwm, scb1
P3.5	GPIO	16	P3.5	15	P3.5	–	–	–	tcpwm2_n[0]	–	–	scb1_spi_ssel_2	Port 3 Pin 5: gpio, lcd, csd, pwm, scb1
P3.6	GPIO	17	P3.6	16	P3.6	–	–	–	tcpwm3_p[0]	–		scb1_spi_ssel_3	Port 3 Pin 6: gpio, lcd, csd, pwm, scb1
P3.7	GPIO	18	P3.7	17	P3.7	–	–	–	tcpwm3_n[0]	–		–	Port 3 Pin 7: gpio, lcd, csd, pwm
VDDD	Power	19	VDDD	–	–	–	–	–	–	–	–	–	Digital Supply. 1.8 - 5.5 V
P4.0	GPIO	20	P4.0	18	P4.0	15	P4.0	–	–	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0
P4.1	GPIO	21	P4.1	19	P4.1	16	P4.1	–	–	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0
P4.2	GPIO	22	P4.2	20	P4.2	17	P4.2	csd_c_mod	–	–	–	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0
P4.3	GPIO	23	P4.3	21	P4.3	18	P4.3	csd_c_sh_tank	–	–	–	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0
P0.0	GPIO	24	P0.0	22	P0.0	19	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
P0.1	GPIO	25	P0.1	23	P0.1	20	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
P0.2	GPIO	26	P0.2	24	P0.2	21	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
P0.3	GPIO	27	P0.3	25	P0.3	22	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
P0.4	GPIO	28	P0.4	26	P0.4	–	–	–	–	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1
P0.5	GPIO	29	P0.5	27	P0.5	–	–	–	–	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1
P0.6	GPIO	30	P0.6	28	P0.6	23	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
P0.7	GPIO	31	P0.7	29	P0.7	24	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup

Pins		44-TQFP		40-QFN		28-SSOP		Alternate Functions for Pins					Pin Description
Name	Type	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
XRES	XRES	32	XRES	30	XRES	25	XRES	–	–	–	–	–	Chip reset, active low
VCCD	Power	33	VCCD	31	VCCD	26	VCCD	–	–	–	–	–	Regulated supply, connect to 1 µF cap or 1.8 V
VDDD	Power	34	VDDD	32	VDDD	27	VDD	–	–	–	–	–	Digital Supply, 1.8 - 5.5 V
VDDA	Power	35	VDDA	33	VDDA	27	VDD	–	–	–	–	–	Analog Supply, 1.8 - 5.5 V, equal to VDDD
VSSA	Power	36	VSSA	34	VSSA	28(DN)	VSS	–	–	–	–	–	Analog Ground
P1.0	GPIO	37	P1.0	35	P1.0	1	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
P1.1	GPIO	38	P1.1	36	P1.1	2	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm
P1.2	GPIO	39	P1.2	37	P1.2	3	P1.2	ctb.oa0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
P1.3	GPIO	40	P1.3	38	P1.3	–	–	ctb.oa1.out	tcpwm3_n[1]	–	–	–	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
P1.4	GPIO	41	P1.4	39	P1.4	–	–	ctb.oa1.inm	–	–	–	–	Port 1 Pin 4: gpio, lcd, csd, ctb
P1.5	GPIO	42	P1.5	–	–	–	–	ctb.oa1.inp	–	–	–	–	Port 1 Pin 5: gpio, lcd, csd, ctb
P1.6	GPIO	43	P1.6	–	–	–	–	ctb.oa0.inp_alt	–	–	–	–	Port 1 Pin 6: gpio, lcd, csd
P1.7	GPIO	44	P1.7	40	P1.7	4	P1.7	ctb.oa1.inp_alt ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

Descriptions of the Pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin).

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin.

VCCD: Regulated Digital supply (1.8 V ±5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following packages are supported: 44-pin TQFP, 40-pin QFN, and 28-pin SSOP.

Figure 6. 44-pin TQFP Part Pinout