



LD1071

16 Channel Output LED Driver with 14 bit PWM Controller

LD1071

16 Channel Output LED Driver with 14 bit PWM
Controller

Ver. 1.0 / Mar. 2009

This document is a general product description and is subject to change without notice.
LDT Inc. does NOT assume any responsibility for use of circuits described.



LD1071 Revision History

| Version | Contents | Transfer Date |
|---------|-----------------|---------------|
| 1.0 | - First Version | 2009.03.12 |

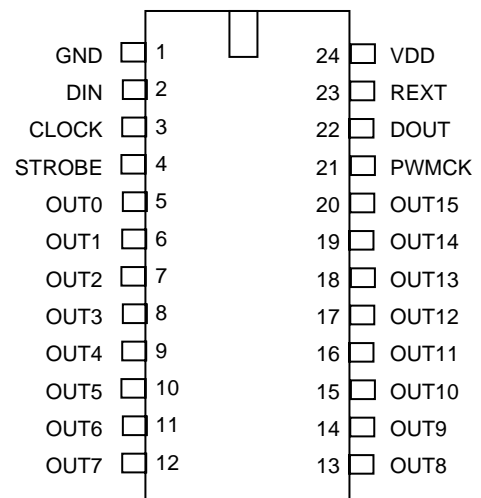
DESCRIPTION

The LD1071 is specifically designed for LED and LED display applications using PWM(Pulse Width Modulation) control with 14 bit color depth. The LD1071 provides a constant output current for driving the LEDs against for the variation of LED forward voltage(V_f). The constant output current can be preset through an external resistor. Moreover, the preset output current with external resistor can be programmed up to 256 levels for LED global brightness adjustment. The LD1071 consists of 16 bit shift registers, latches, and-gates, constant current driver and 14 bit PWM controller.

FEATURES

- Output current : set-up at 5mA to 45mA with an external resistor
(when VDD=3.3V, I_{out} : 5mA ~ 30mA)
- Include error detection circuit
- 16 constant current output channels
- 14 bit gray scale PWM control
- 8 bit programmable output current control
- Constant current accuracy
 - Pin to pin deviation : < $\pm 3\%$ (Max)
 - Chip to chip deviation : < $\pm 6\%$ (Max)
- 3.3V / 5V CMOS compatible input
- Package : LD1071-SP (SOP-24), LD1071-SS (SSOP-24)
- Maximum CLOCK input frequency : 25MHz
- Maximum PWMCK input frequency : 25MHz

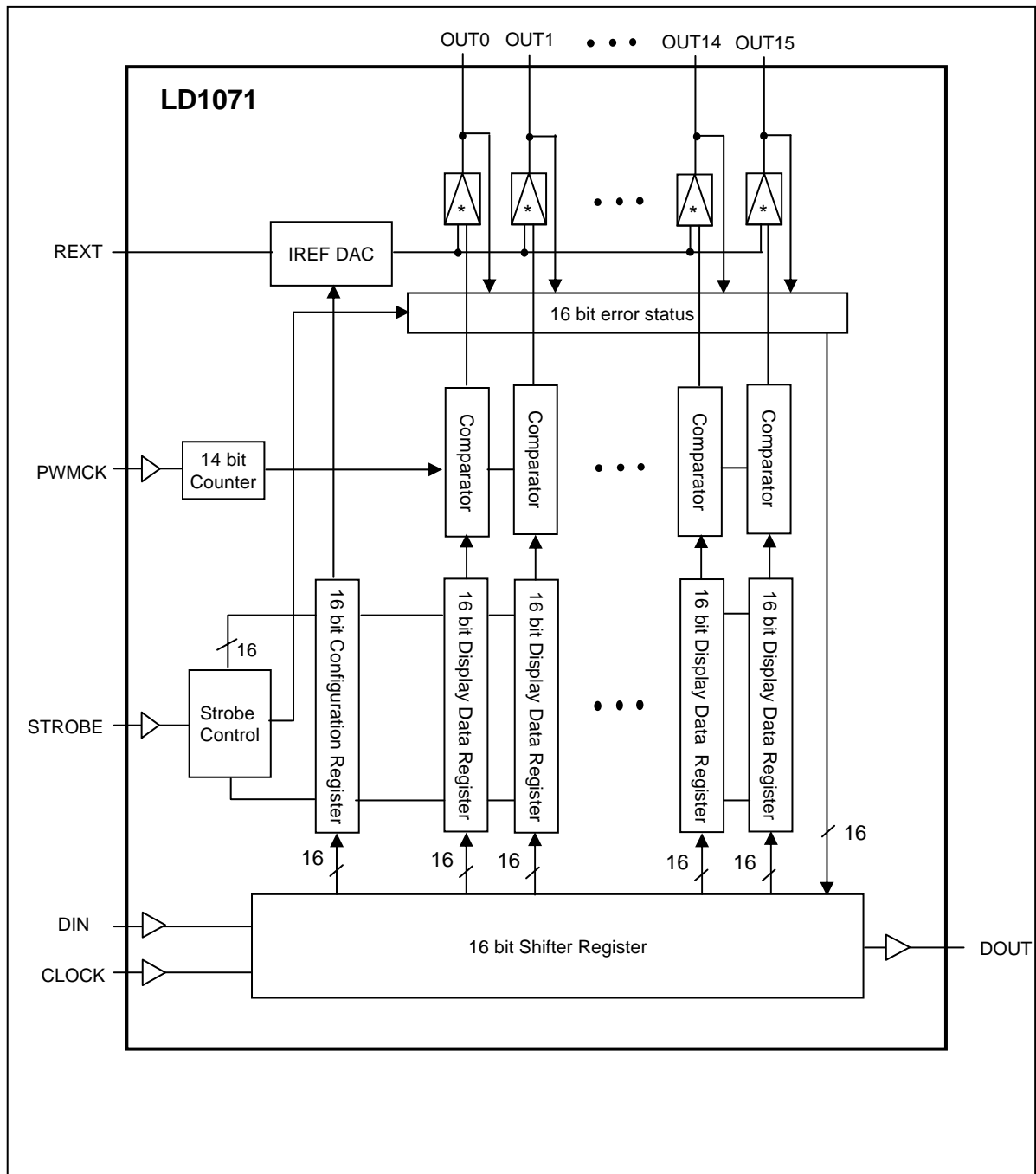
PIN CONFIGURATION



PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---------------|----------|---|
| 1 | GND | Ground signal |
| 2 | DIN | Serial input data |
| 3 | CLOCK | Shift input clock for serial input data DIN(Rising Edge Clocking) |
| 4 | STROBE | Data strobe signal. This pin is a pull-down type. |
| 5~12 13~20 | OUTn | Constant current outputs, n = 0 ~ 15 |
| 21 | PWMCK | PWM gray scale clock signal. This pin is a pull-up type. |
| 22 | DOUT | Serial data output |
| 23 | REXT | Connect the resistor between this pin and GND to set up the constant output current for all the OUTn. |
| 24 | VDD | Power supply signal (3.3V/5V) |

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

| PARAMETER | | SYMBOL | RATING | UNIT |
|---|------|----------------------|---------------------------|------|
| Supply Voltage | | V _{DD} | 0~7.0 | V |
| Output Voltage | | V _{OUT} | -0.5~13.5 | V |
| Output Current | | I _{OUT} | 450 | mA |
| Input Voltage | | V _{IN} | -0.4~V _{DD} +0.4 | V |
| GND Terminal Current | | I _{GND} | 960 | mA |
| CLOCK Frequency | | f _{CK} | 25 | MHz |
| PWMCK Frequency | | f _{PWMCK} | 25 | MHz |
| Power Dissipation | SOP | P _D | 1.67 | W |
| | SSOP | | 1.48 | |
| Thermal Resistance (On PCB, TA = 25) | SOP | R _{th(j-a)} | 75 | /W |
| | SSOP | | 85 | |
| Operating Temperature | | T _{opr} | -40~85 | °C |
| Storage Temperature | | T _{stg} | -55~150 | °C |

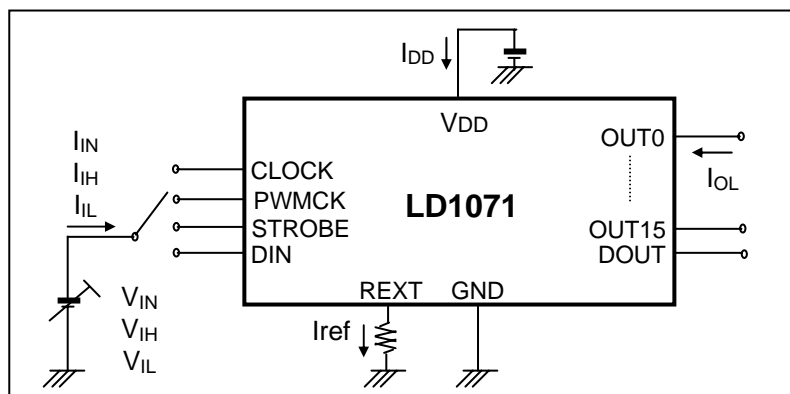
RECOMMENDED OPERATING CONDITIONS

| DC CHARACTERISTICS | | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--------------------------------------|-----------|-------------------------------------|--------------------|------|--------------------|------|
| Supply Voltage | | V _{DD} | 4.5 | 5 | 5.5 | V |
| LED Driver Output Voltage | | V _{OUT} | | | 13.5 | V |
| Input Voltage | “H” Level | V _{IH} | 0.8V _{DD} | - | V _{DD} | V |
| | “L” Level | V _{IL} | GND | - | 0.2V _{DD} | |
| Output Voltage | DOUT | V _{OL} | - | - | 0.2V _{DD} | V |
| | | V _{OH} | 0.8V _{DD} | - | - | |
| High Level Output Current | | I _{OH} | | | -1 | mA |
| Low Level Output Current | | I _{OL} | | | 1 | mA |
| LED Driver Output Current | | I _{OUT} | | | 20 | mA |
| Operating Free-air Temperature Range | | | -40 | | 85 | °C |
| AC CHARACTERISTICS | | SYMBOL | MIN. | TYP. | MAX. | UNIT |
| CLOCK Frequency | | f _{CK} | | | 25 | MHz |
| PWMCK Frequency | @5V | f _{PWMCK} | | | 25 | MHz |
| | @3.3V | f _{PWMCK} | | | 20 | MHz |
| Pulse Width | CLOCK | t _{WH0} / t _{WL0} | 20 | | | ns |
| | PWMCK | t _{WH1} | 40 | | | ns |
| | STROBE | t _{WH2} | 40 | | | ns |
| Setup Time | | t _{setup} | 15 | | | ns |
| Hold Time | | t _{hold} | 15 | | | ns |

ELECTRICAL CHARACTERISTICS (VDD = 5V, Ta = 25°C)

| Parameter | | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---------|--------|---|--------|------|--------|------|
| Input Voltage | H Level | VIH | - | 0.7VDD | | VDD | V |
| | L Level | VIL | - | GND | | 0.3VDD | |
| Output Leakage Current | | IOZ | VOH=6.0V | | | 1 | uA |
| Output Voltage | DOUT | VOL | IOL=1mA | | | 0.2VDD | V |
| | | VOH | IOH=1mA | 0.8VDD | | | |
| Output Current1 Pin to Pin Deviation | | IOLPP1 | REXT=500 IOUT=40mA, VOUT=1.5V | | ±1.5 | ±3.0 | % |
| Output Current1 Chip to Chip Deviation | | IOLCC1 | REXT=500 IOUT=40mA, VOUT=1.5V | | ±3.0 | ±6.0 | % |
| Output Current vs. Supply Voltage Regulation | | %/VDD | REXT=500 IOUT=40mA, VOUT=1.5V | | ±0.5 | ±1.0 | %/V |
| Pull Up Resistor | | RINUP | - | 100 | 200 | 400 | kΩ |
| Pull Down Resistor | | RINDN | - | 100 | 200 | 400 | |
| Supply Current | | IOFF1 | REXT=Open, OUTn=OFF REF=FFh, PWM=Gray0 | - | 0.4 | 0.8 | mA |
| | | IOFF2 | REXT=500 , OUTn=OFF REF=FFh, PWM=Gray0 | - | 4.5 | 7.0 | |

(Note) REF : Constant Current Control Value (CR[7:0] of Configuration Register)

DC CHARACTERISTIC TEST CIRCUIT


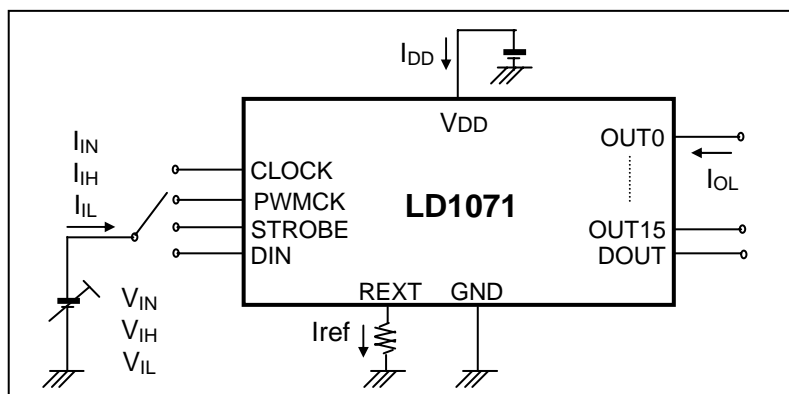
ELECTRICAL CHARACTERISTICS

(VDD = 3.3V, Ta = 25°C)

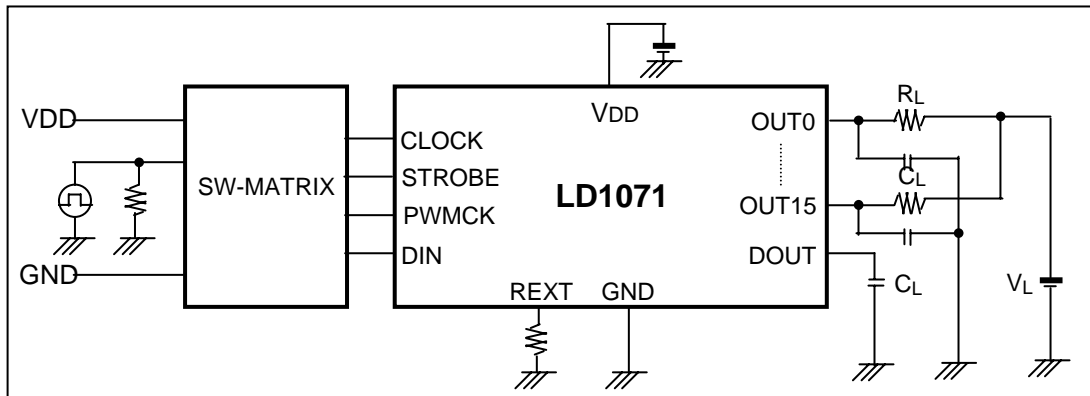
| Parameter | | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---------|--------|---|--------|-------|--------|------|
| Input Voltage | H Level | VIH | - | 0.7VDD | | VDD | V |
| | L Level | VIL | - | GND | | 0.3VDD | |
| Output Leakage Current | | IOZ | VOH=6.0V | | | 1 | uA |
| Output Voltage | DOUT | VOL | IOL=1mA | | | 0.2VDD | V |
| | | VOH | IOH=1mA | 0.8VDD | | | |
| Output Current1 Pin to Pin Deviation | | IOLPP1 | REXT=500 IOUT=36mA, VOUT=1.5V | | ± 1.5 | ± 3.0 | % |
| Output Current1 Chip to Chip Deviation | | IOLCC1 | REXT=500 IOUT=36mA, VOUT=1.5V | | ± 3.0 | ± 6.0 | % |
| Output Current vs. Supply Voltage Regulation | | %/VDD | REXT=500 IOUT=36mA, VOUT=1.5V | | ± 0.5 | ± 1.0 | %/V |
| Pull Up Resistor | | RINUP | - | 150 | 300 | 500 | kΩ |
| Pull Down Resistor | | RINDN | - | 150 | 300 | 500 | |
| Supply Current | | IOFF1 | REXT=Open, OUTn=OFF REF=FFh, PWM=Gray0 | - | 0.4 | 0.6 | mA |
| | | IOFF2 | REXT=500 , OUTn=OFF REF=FFh, PWM=Gray0 | - | 4.5 | 7.0 | |

(Note) REF : Constant Current Control Value (CR[7:0] of Configuration Register)

DC CHARACTERISTIC TEST CIRCUIT



AC CHARACTERISTIC TEST CIRCUIT



SWITCHING CHARACTERISTICS

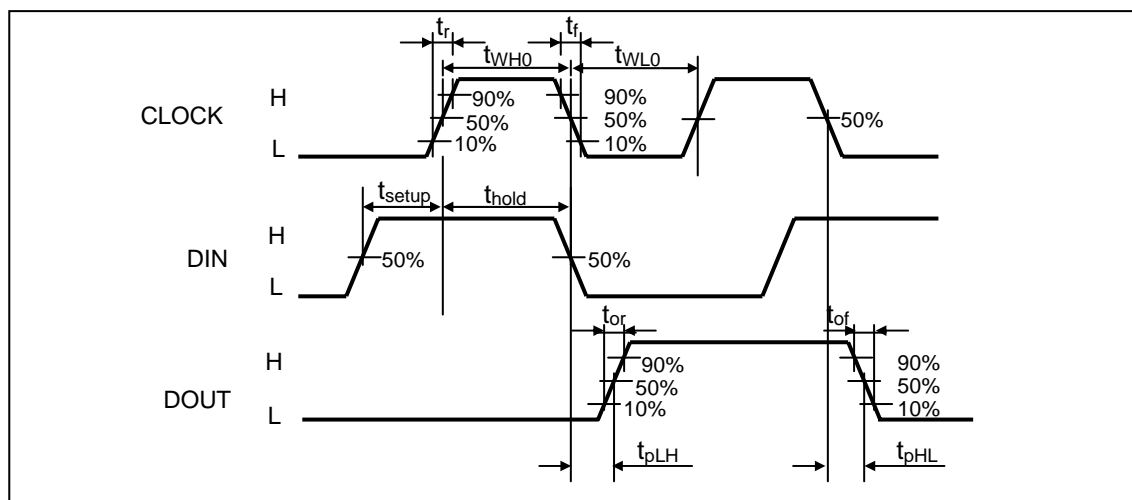
(Ta = 25°C unless otherwise noted)

| PARAMETER | | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|------------|-------------------------------------|---|------|------|------|------|
| Propagation Delay Time (“L” to “H”) | CLOCK-DOUT | t _{pLH} | V _{DD} = 5.0V V _{IH} = VDD V _{IL} = GND f _{CK} = 10MHz R _{EXT} = 1590 I _{OUT} = 19.1mA C _L = 10.0pF R _L = 150 V _L = 4.5V | - | 10 | 20 | ns |
| | PWMCK-OUTn | | | - | - | 50 | |
| Propagation Delay Time (“H” to “L”) | CLOCK-DOUT | t _{pHL} | | - | 10 | 20 | ns |
| | PWMCK-OUTn | | | - | - | 30 | |
| Maximum CLOCK Frequency | | f _{CKMAX} (*1) | | - | 10 | 25 | MHz |
| Maximum PWMCK Frequency | | f _{PWMCKMAX} (*1) | | - | 8 | 25 | MHz |
| Pulse Width | CLOCK | t _{WH0} / t _{WL0} | | 15 | 20 | - | ns |
| | PWMCK | t _{WH1} | | 15 | 20 | - | ns |
| | STROBE | t _{WH2} | | 15 | 20 | - | ns |
| Data Set Up Time | | t _{setup} (D) | | 10 | 15 | - | ns |
| Data Hold Time | | t _{hold} (D) | | 10 | 15 | - | |
| STROBE Set Up Time | LH | t _{STBsetup} | | 10 | 15 | - | ns |
| | HL | | | 10 | 15 | - | |
| STROBE Hold Time | LH | t _{STBhold} | | 10 | - | - | ns |
| | HL | | | 10 | - | - | |
| Maximum Clock Rise Time | | t _r | | - | - | 30 | ns |
| Maximum Clock Fall Time | | t _f | | - | - | 30 | |
| Output Rise Time (OUTn) | | t _{or} | | - | - | 30 | ns |
| Output Fall Time (OUTn) | | t _{of} | | - | - | 30 | |
| Global Latch Set Up Time | | tg _{lc} | | 20 | - | - | ns |

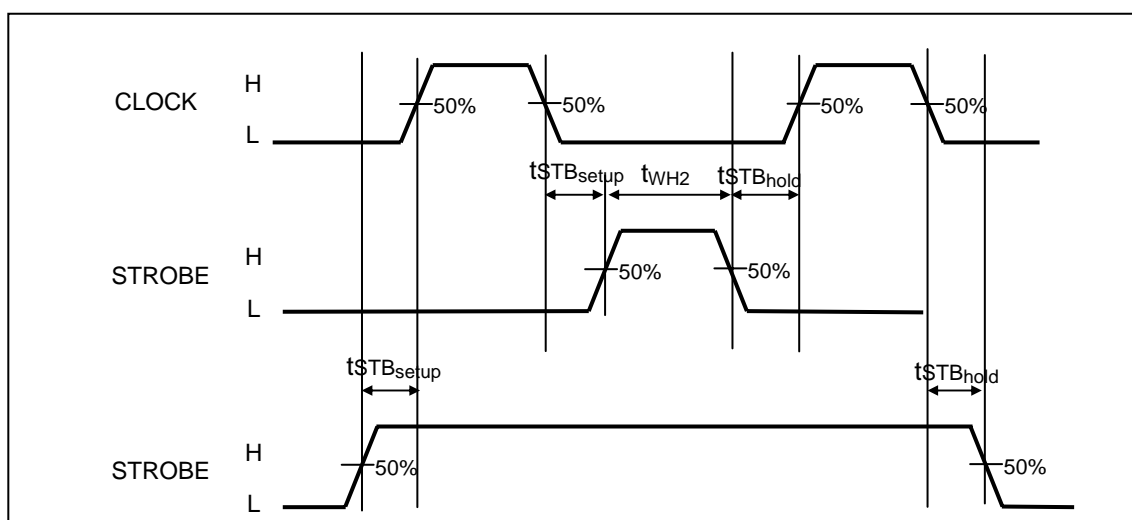
*1 : Cascade Operation

TIMING WAVEFORM

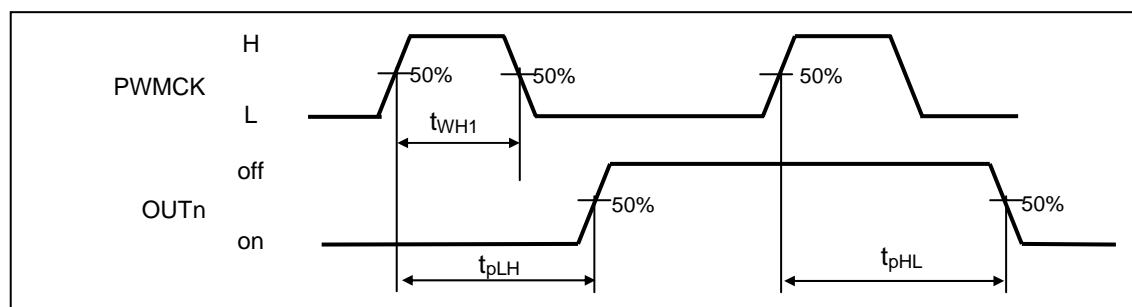
CLOCK-DIN-DOUT



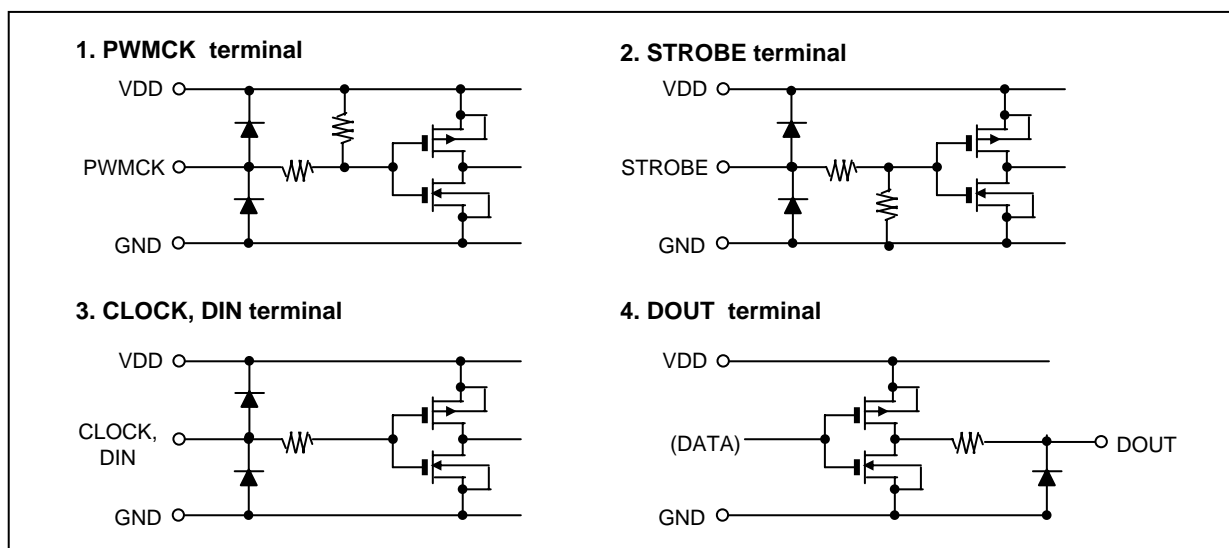
CLOCK-STROBE



PWMCK-OUTn



EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS



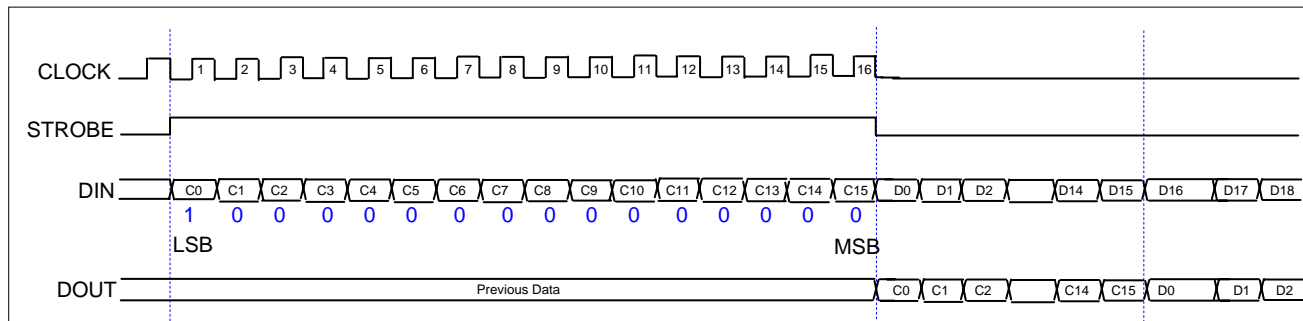
FUNCTIONAL DESCRIPTION

COMMAND TABLE

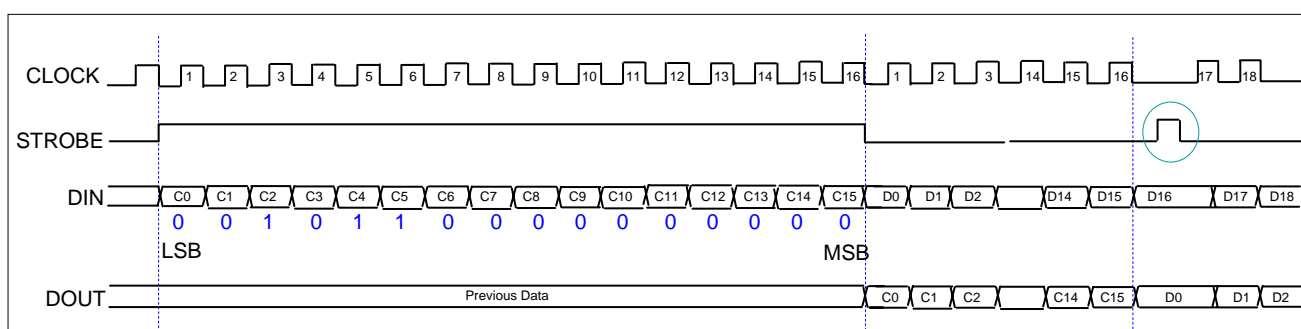
| Command Name | Command Value | Description |
|--------------------------------------|---------------|--|
| Software Reset Command | 0001h | This command should be issued after power supply input. The Configuration Register, internal shift register, Display Data Register will be cleared with '0' states. |
| Configuration Register Write Command | 0034h | This command is used to update the contents of Configuration Register. |
| Configuration Register Read Command | 0038h | This command is used to read the status of Configuration Register. |
| Error Status Read Command | 003Ch | This command is used to check the 'Open/Short' error status of LED. |
| Display Data Write Command | 0084h | This command is used to write the display image data into LED driver IC for display system. |
| Global Latch Command | - | <p>This command is used to deliver the internal display data register outputs latched by Display Data Write Command to the internal PWM comparator to make an output current.</p> <p>The Global Latch Command should be transferred after sending the final display data you want.</p> <p>The Global Latch Command has no command value but it needs a special execution sequence.</p> |

TIMING DIAGRAM OF COMMAND CONTROL

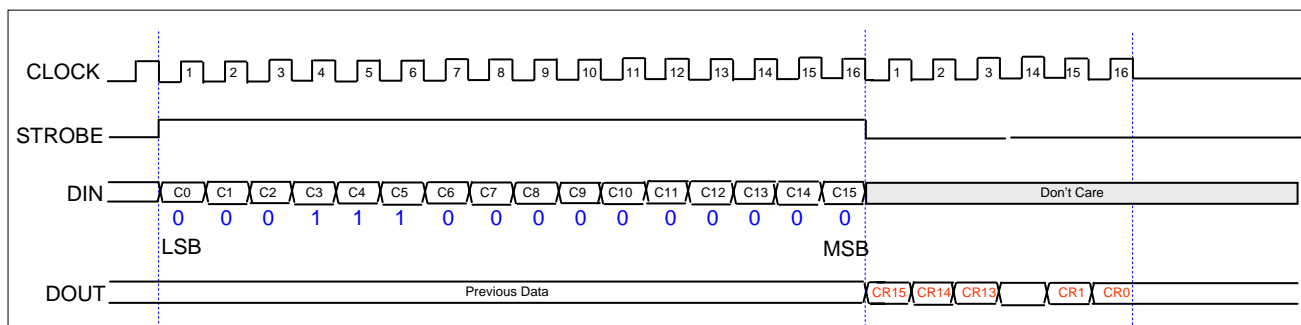
Software Reset Command (0001h)



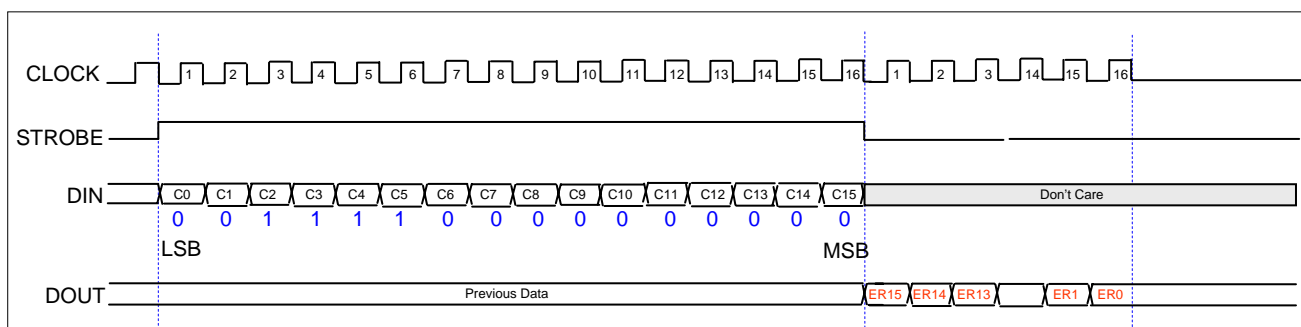
Configuration Register Write Command (0034h)



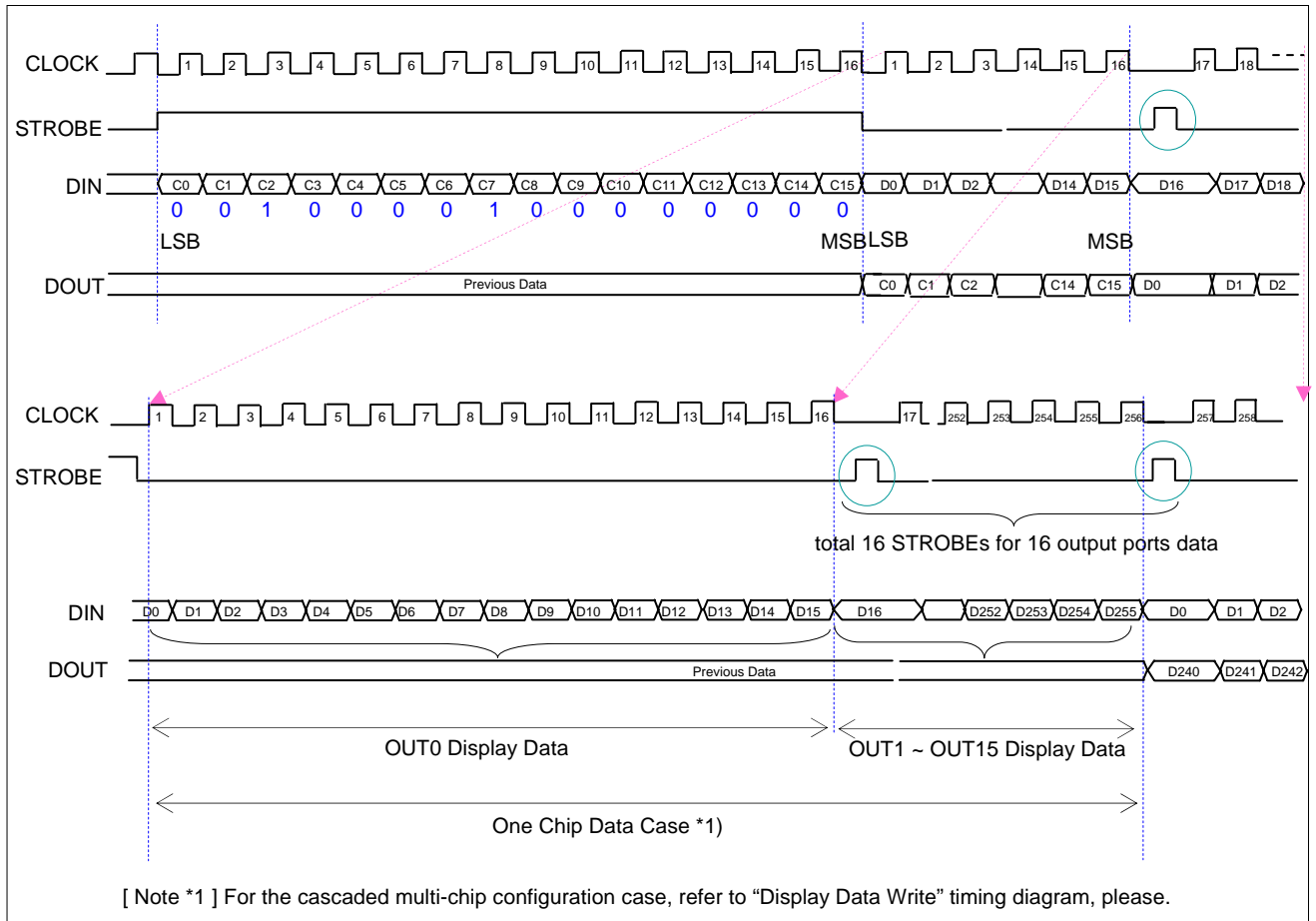
Configuration Register Read Command (0038h)



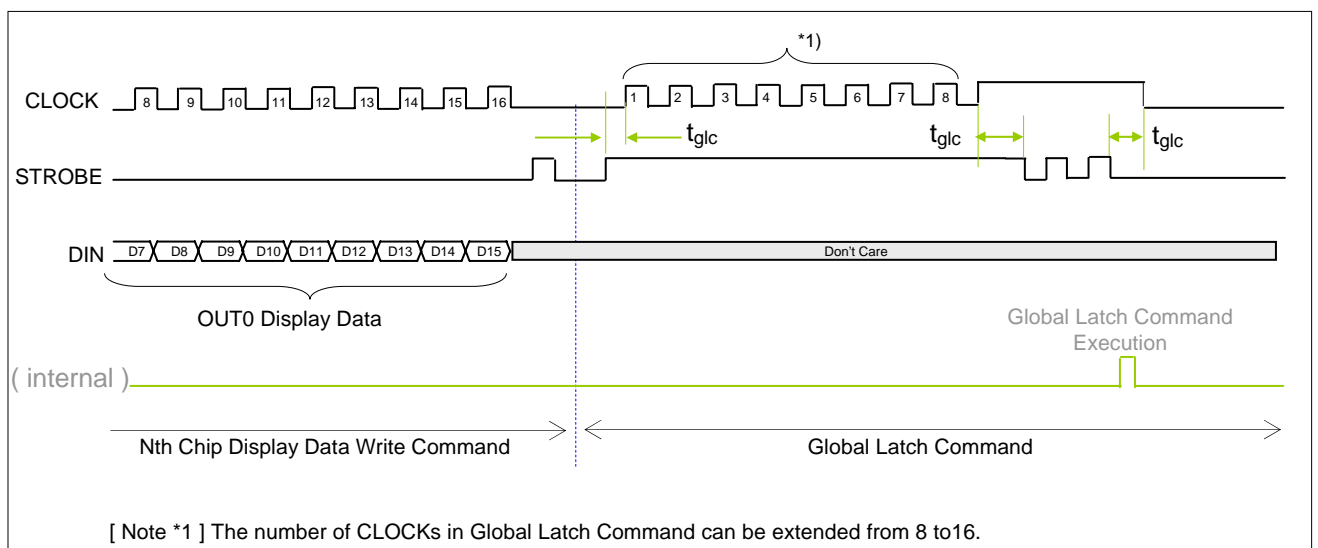
Error Status Read Command (003Ch)



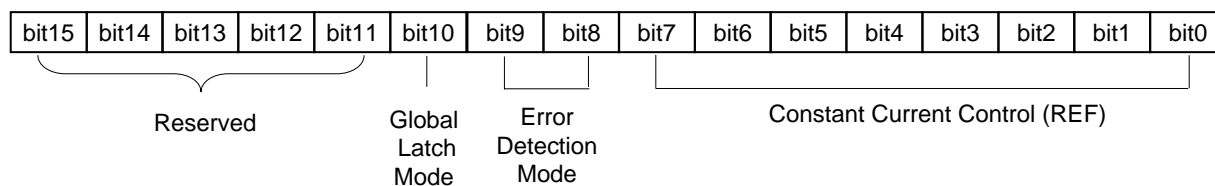
Display Data Write Command (0084h)



Global Latch Command



CONFIGURATION REGISTER (CR[15:0])



Constant Current Control (CR[7:0] Default 00h)

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Current Value |
|------|------|------|------|------|------|------|------|---------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IOUT/256 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | IOUT*2/256 |
| - | - | - | - | - | - | - | - | - |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | IOUT*128/256 |
| - | - | - | - | - | - | - | - | - |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | IOUT*255/256 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | IOUT |

The IOUT is a constant current of OUTn port which is determined by REXT resistor.

Error Detection Mode (CR[9:8] Default 00b)

| bit9 | bit8 | Error Mode |
|------|------|---------------|
| 0 | 0 | Check Disable |
| 0 | 1 | Open Check |
| 1 | 0 | Short Check |
| 1 | 1 | Check Disable |

Global Latch Mode (CR[10] Default 0b)

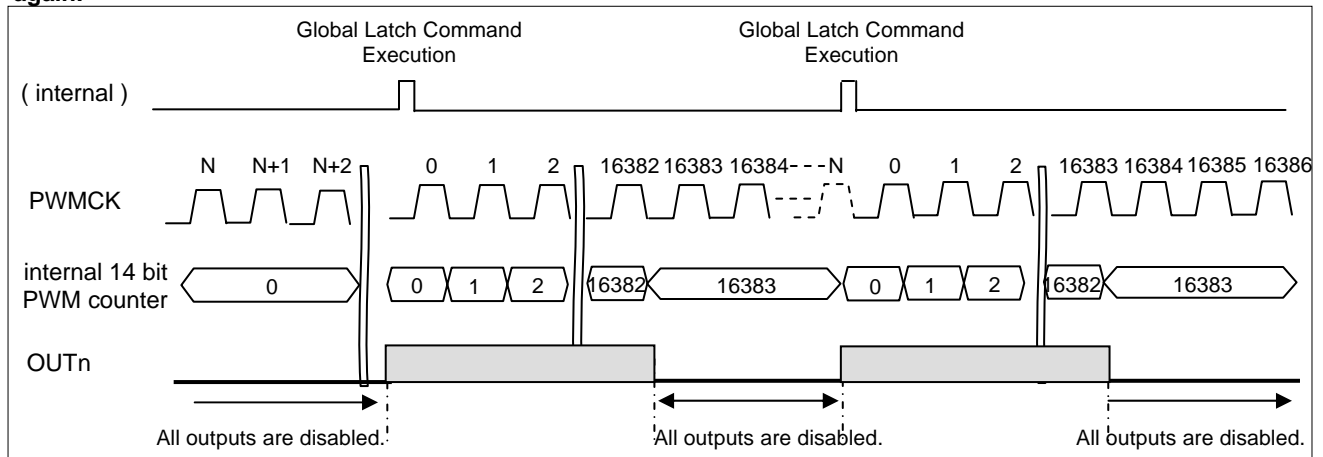
| bit10 | Global Latch Mode |
|-------|---------------------------|
| 0 | One Shot |
| 1 | Automatic Synchronization |

SYNCHRONIZATION FOR PWM COUNTING

The LD1071's Global Latch Command supports two kinds of synchronization mode for PWM counting. The default mode is One Shot Mode(Configuration Register bit10=0) and the other mode is Automatic Synchronization Mode(Configuration Register bit10=1).

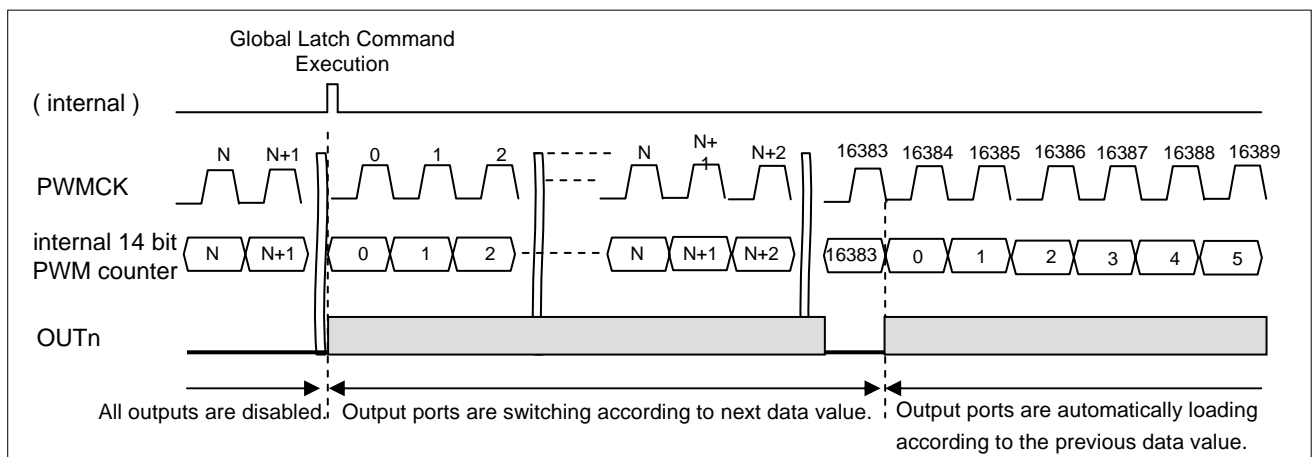
One Shot Mode (Default)

When Global Latch Command is executed in this mode, the LD1071 will update the next image data into output ports immediately, no matter what the counting status of previous image data is. The 14 bit internal PWM Counter is initialized with 0000h and the internal PWM counter starts counting with PWMCK clock. When the internal PWM counter value is reached to FFFFh, the internal PWM counter stops the counting even next PWMCK clock is inputting continuously. As a result, all the outputs will be stopped after finishing one internal PWM display cycle (16384 PWMCK clocks). Only the next Global Latch Command can initialize the counting again.



Automatic Synchronization Mode

When Global Latch Command is executed in this mode(Global Latch Mode=1), the LD1071 will update the next image data into output ports immediately, no matter what the counting status of previous image data is. When the internal PWM counter value is reached to FFFFh, if there is no Global Latch Command, the LD1071 automatically loads the previous image data into output ports at next 16384th PWMCK clock again. So in this mode, output ports will be automatically updated at every 16384 PWMCK clocks with previous data.



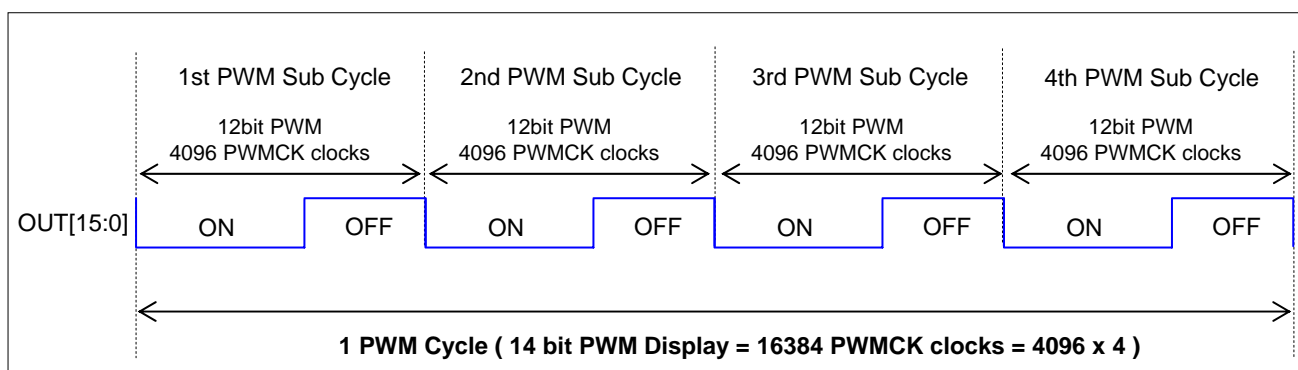
WRITING THE DISPLAY DATA

With the 16 bit data, all output ports can be built with 16,384 gray scales. The 16-bit input shift register latches 16 times of gray scale data into each data buffer with Display Data Write Command sequentially . Finally Global Latch Command will load the 256 bit internal data buffers with LSB first into from output port 15(OUT15) to output port 0(OUT0). Even 16 bit display data for each port should be transferred, only 14 bits data are valid for gray scale image (bit[13:0]) and the high 2bits(bit[15:14]) are reserved. For the detail timing and sequence, refer to “Display Data Write Command” and “Global Latch Command” which is described on page 14, please.

PWM DISPLAY CYCLE

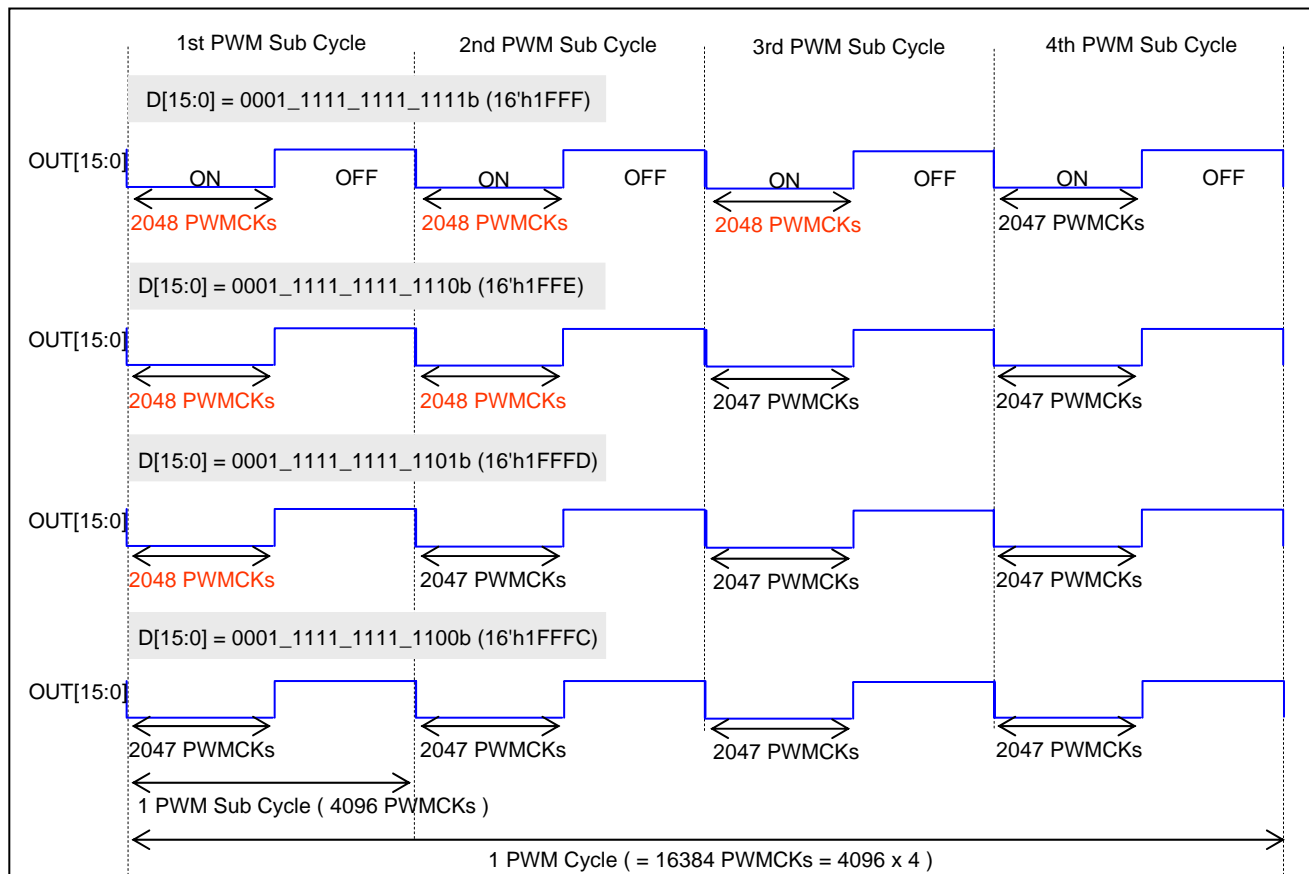
The LD1071 implements the 14 bit gray level of each output port using the 4 PWM sub cycles. Each PWM sub cycle is consisted of 12 bit PWMCK clocks. This enhancement provides a excellent energy distribution in lighting the LED and increases the visual refresh rate and reduces the flickers.

| | |
|------------|---|
| D[15:14] | : Reserved |
| D[13:0] | : Display Data(14 bit Gray Scale Data) |
| bit[13:2] | : 12bit PWM Comparing Data |
| bit[1: 0] | : PWM Insert data |
| 1 1 | : one pulse is inserted in 1st, 2nd and 3rd PWM Sub Cycle |
| 1 0 | : one pulse is inserted in 1st and 2nd PWM Sub Cycle |
| 0 1 | : one pulse is inserted in 1st PWM Sub Cycle |
| 0 0 | : Not inserted |

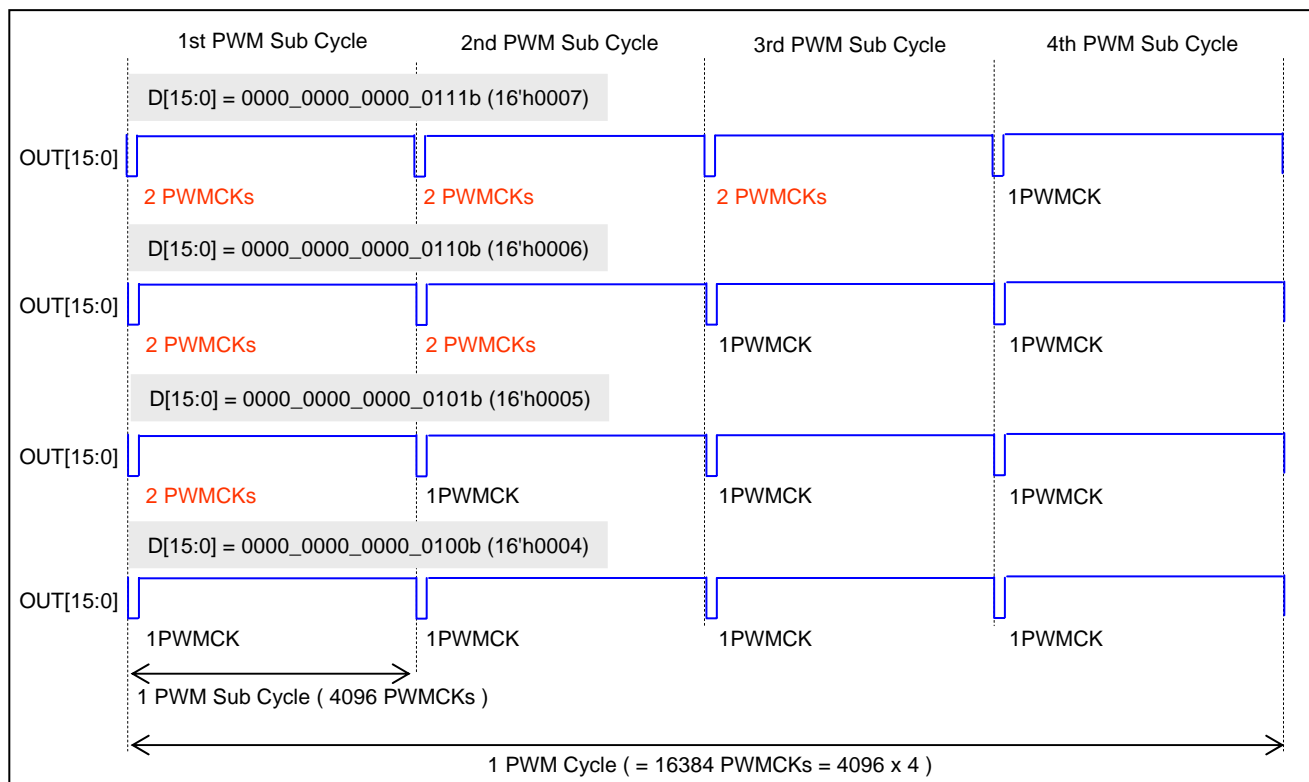


The following examples show the PWM timing diagram for different display data.

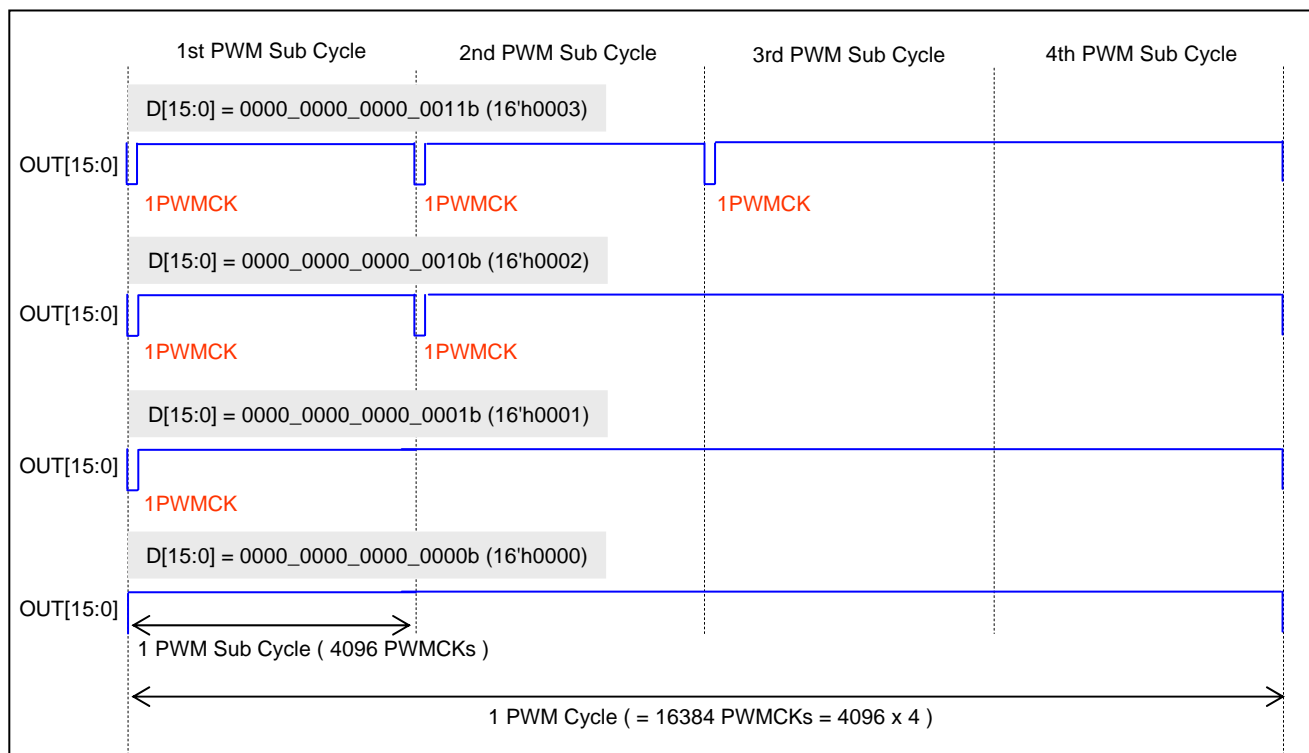
(Case 1)

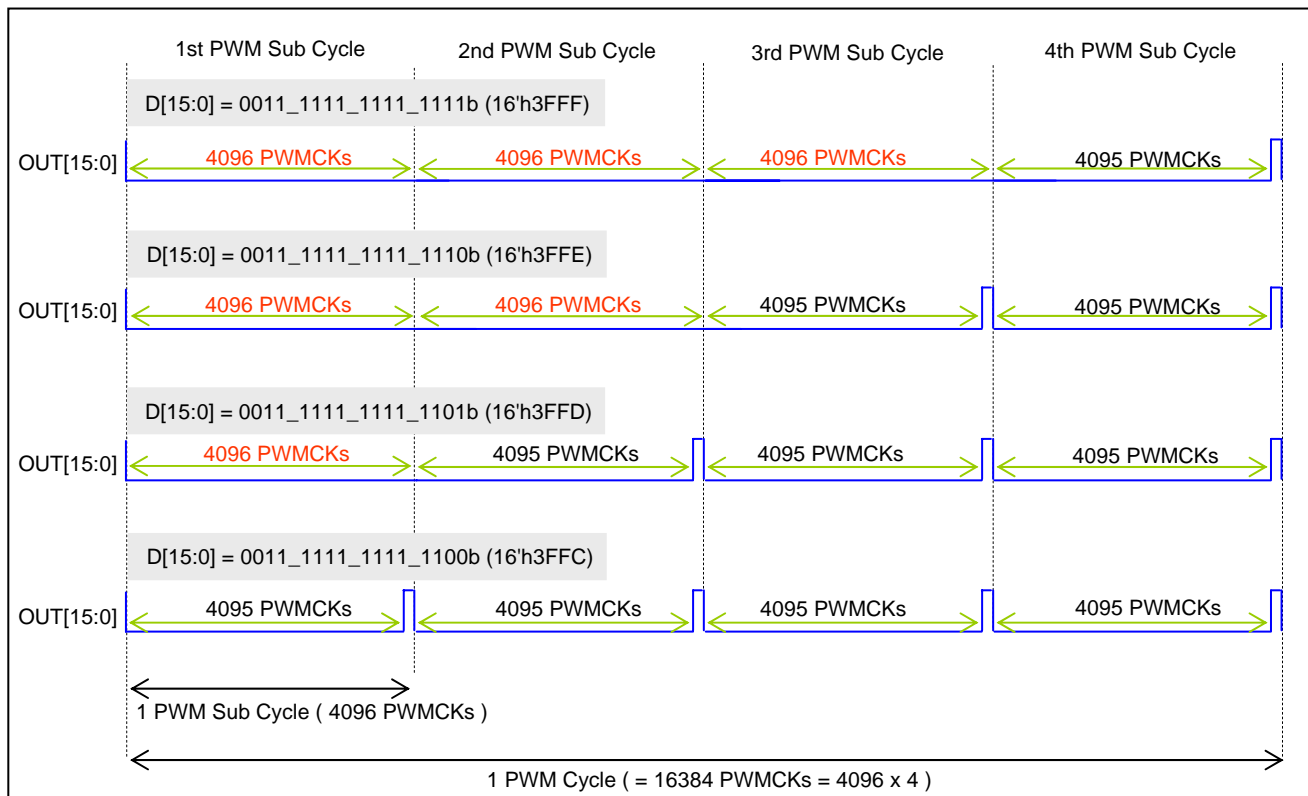
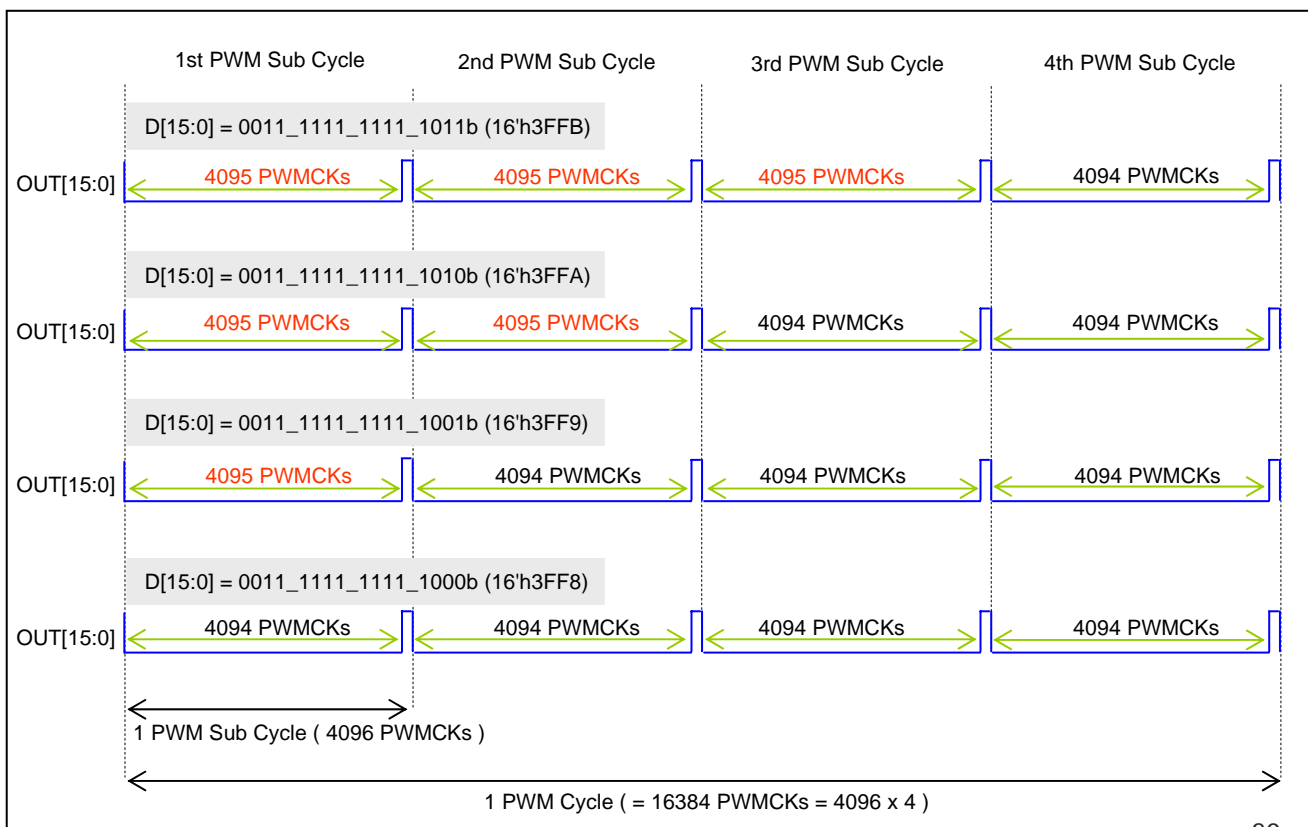


(Case 2)



(Case 3)



(Case 4)

(Case 5)


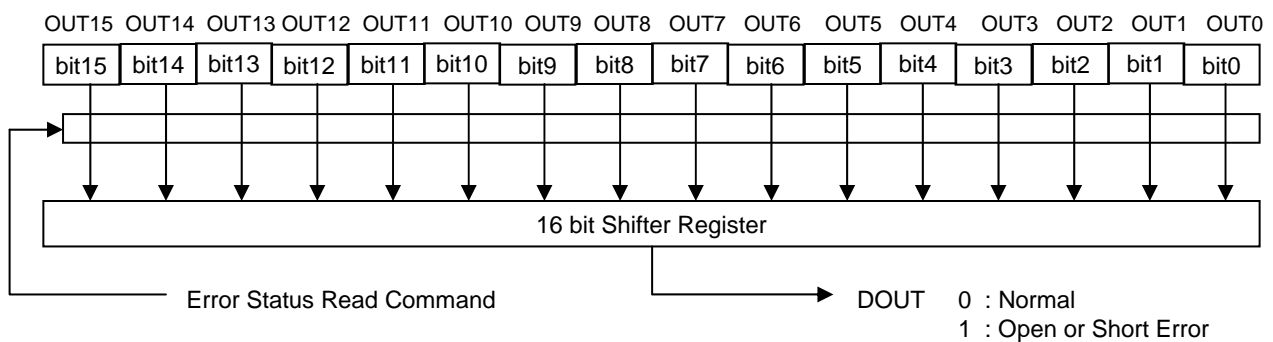
ERROR DETECTION

The LD1071 will be able to detect the error status of LED such as open/short error. This function can be entered by setting the bits of Error Detection Mode(CR[9:8]) as 01b(Open Detection) or 10b(Short Detection). The correct meaning of error is defined as follows;

- Open Error : Output port(OUTn) is not connected to LED.
- Short Error : Output port(OUTn) is shorted to GND.

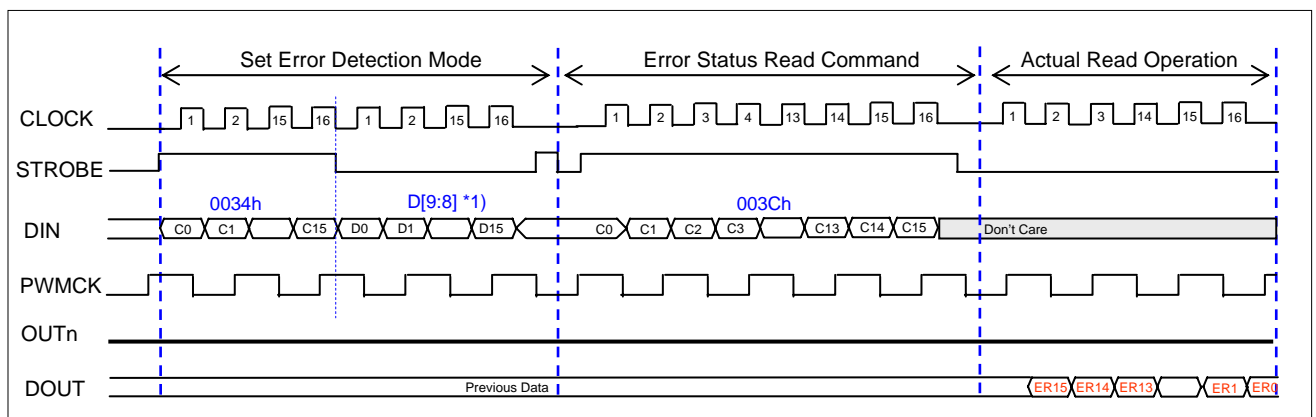
| Error Detection Code | | | |
|----------------------|--------------------|-------------------------|-------------|
| | Output Port status | Error Detection Voltage | Meaning |
| Open Check | OFF | OUT Voltage > 0.8V | Normal |
| | | OUT Voltage < 0.8V | Open Error |
| Short Check | OFF | OUT Voltage > 0.8V | Normal |
| | | OUT Voltage < 0.8V | Short Error |

Error Status Register (ER[15:0])

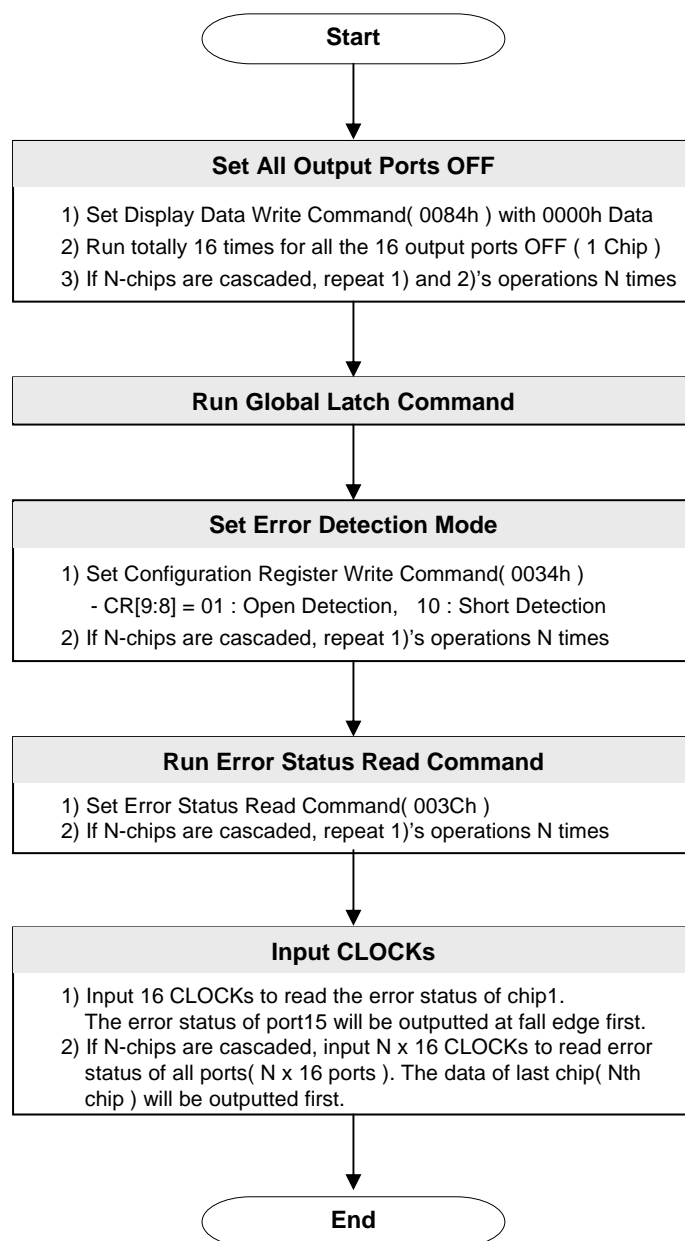


Timing Diagram of Error Status Check

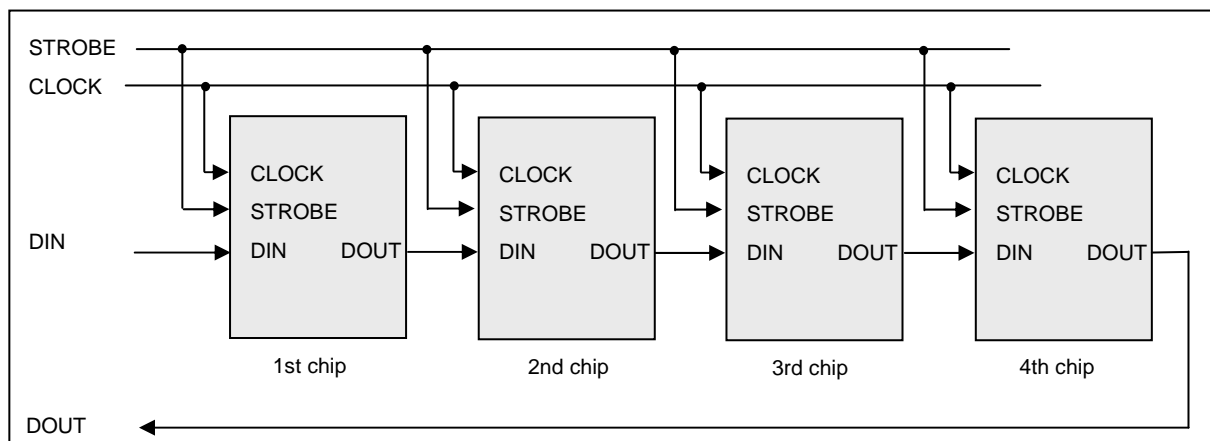
The next timing diagram shows the sequence of error status read operation. The actual error status is read with MSB first after execution of Error Status Read Command. First of all, in order to read the error status, all the output ports (OUT15~OUT0) should be off. So you need some pre-processing for error status read. The flow chart will be provided on next page.



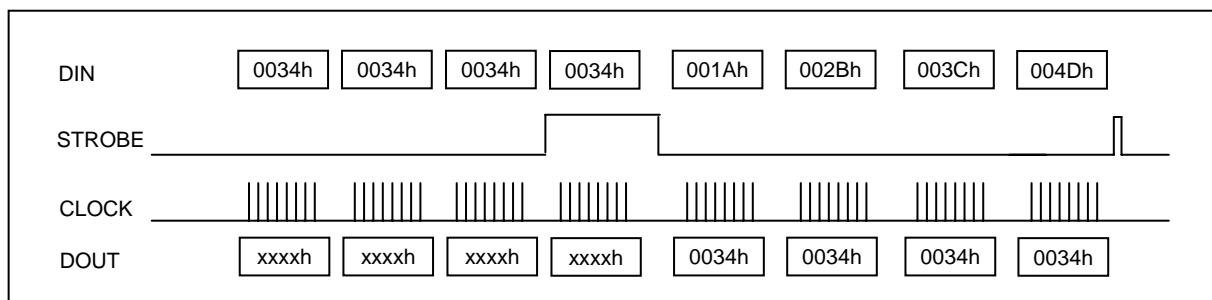
Note *1) In order to keep the Constant Current Value(CR[7:0]) and Global Latch Mode(CR[10]) correctly, maybe you need to read the Configuration Register through the Configuration Register Read Command(0038h) prior to set Error Detection Mode.


Flow Chart of Error Status Check

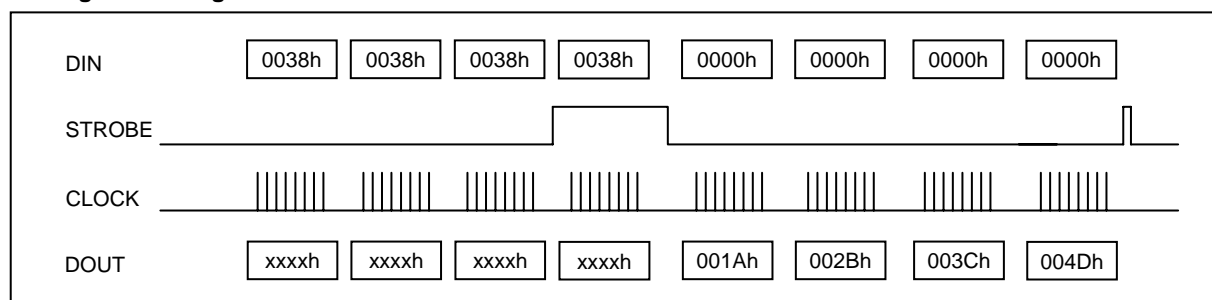
COMMAND SETTING GUIDE FOR MULTI-CHIP CASCADE CONFIGURATION



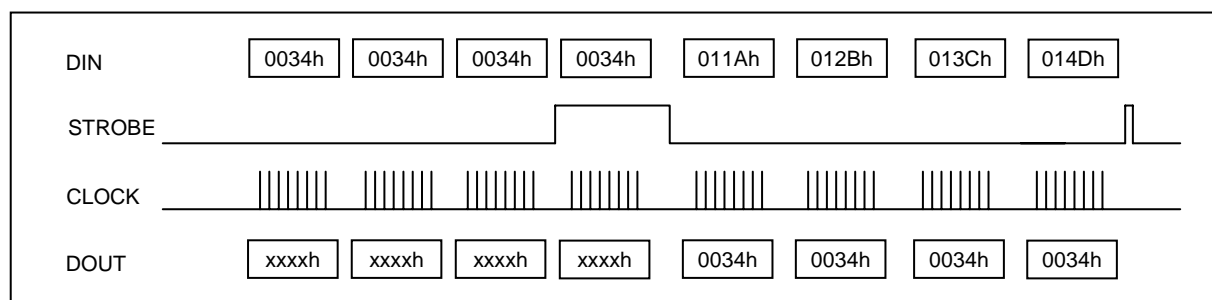
Configuration Register Write(Current Control)



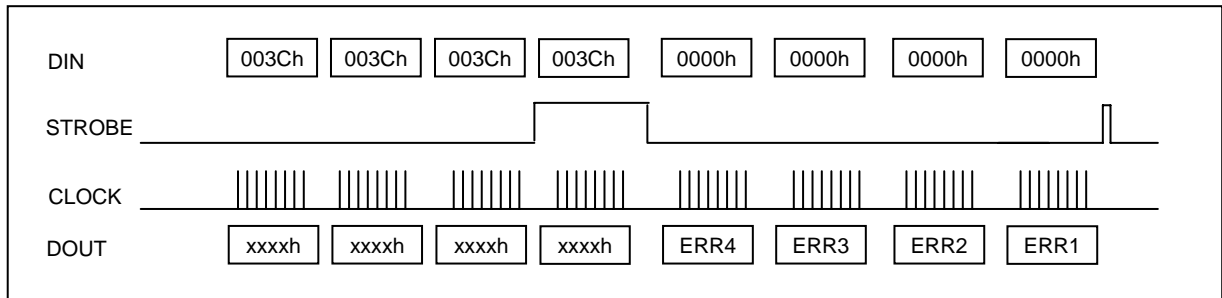
Configuration Register Read



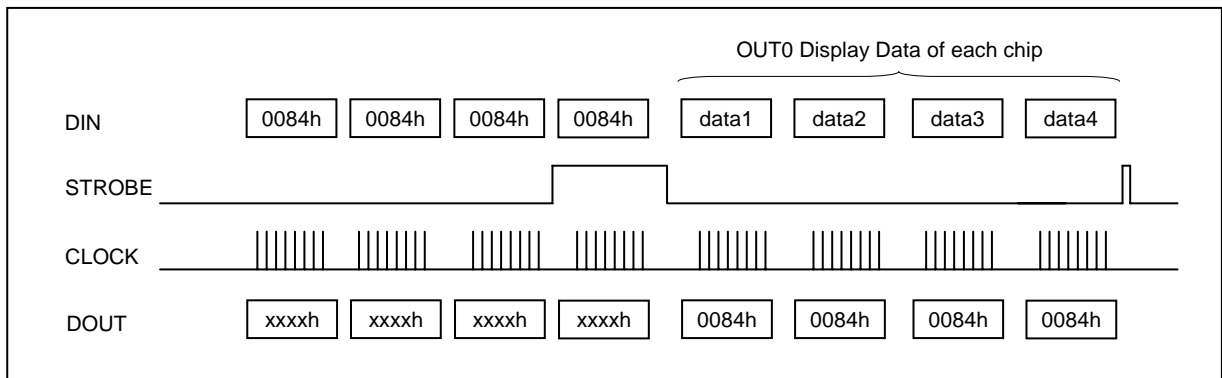
Configuration Register Write (Error Detection Enable)



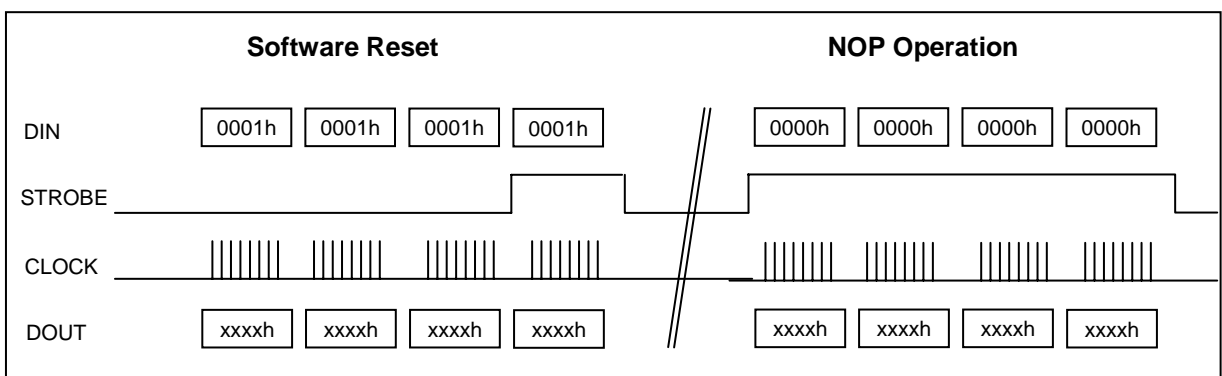
Error Status Read



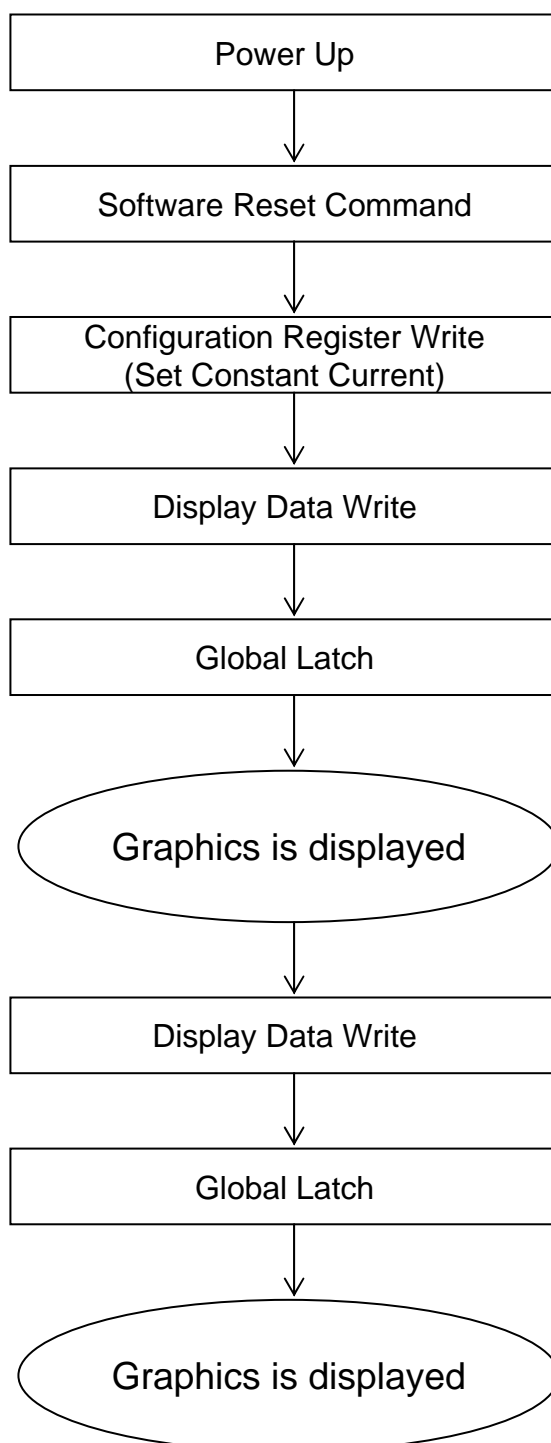
Display Data Write



Software Reset & NOP Operation



RECOMMENDATION OF GLOBAL SEQUENCE



The first command should be issued after 0.1ms from Power-Up.

SETTING OUTPUT CURRENT

The output current is determined by an external resistor. The relationship between I_{OUT} and R_{EXT} is as follows;

When $V_{DD} = 5V$

$$I_{OUT}[A] = \{1.06/(120+R_{EXT})\} * S * 61.4$$

where $S = (REF+1)/512$

When $V_{DD} = 3.3V$

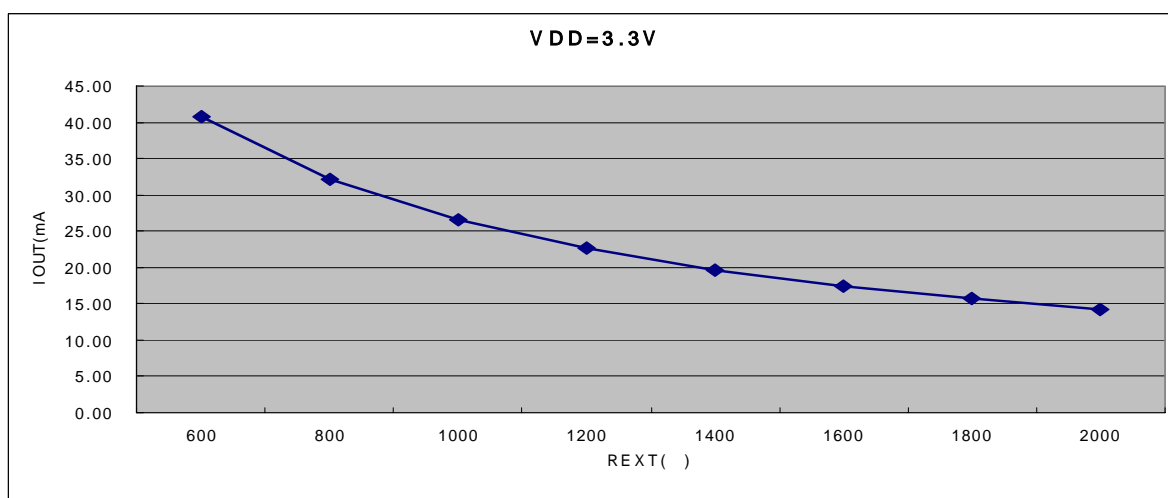
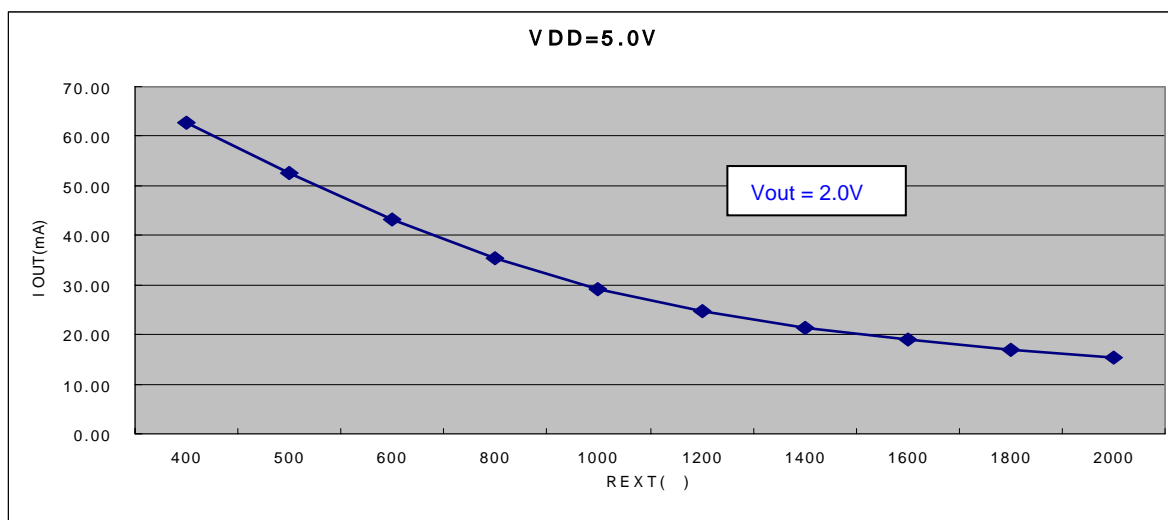
$$I_{OUT}[A] = \{1.06/(150+R_{EXT})\} * S * 57.6$$

where $S = (REF+1)/512$

- R_{EXT} : External Resistor[Ω]

- REF : Constant Current Control (0 ~ 255, CR[7:0] of Configuration Register)

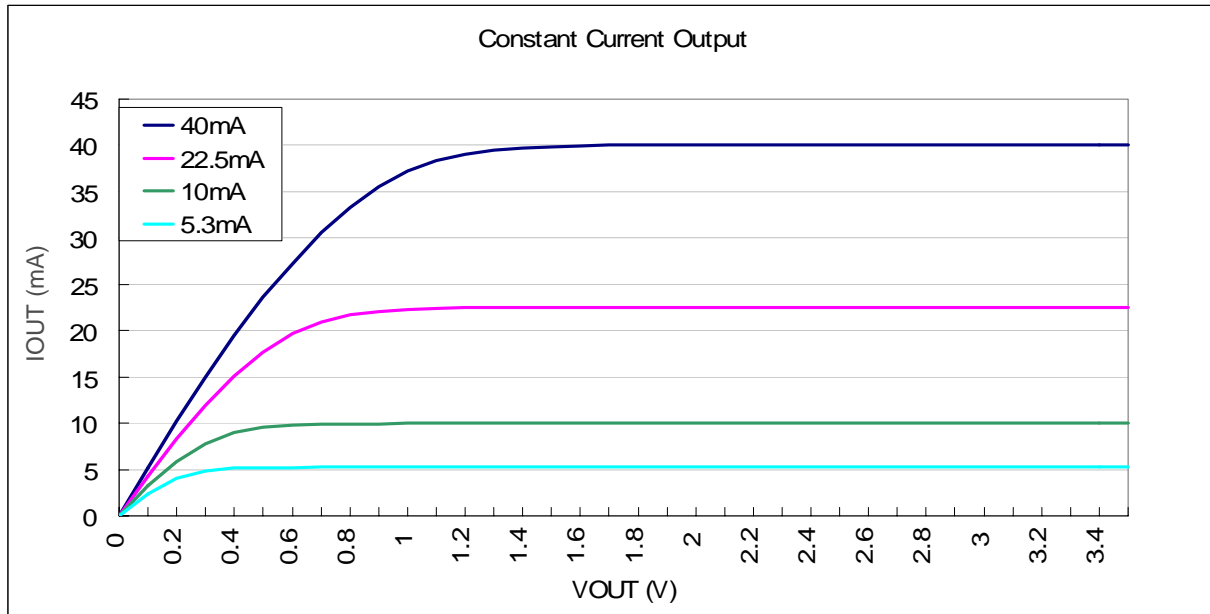
Because the default REF value(CR[7:0]) of Configuration Register(0034h) for current control is 00h, if you want to set the output current through changing the R_{EXT} value with following graph, do not forget to write the CR[7:0] of Configuration Register with 'FFh', please.



[Note] When VDD is 3.3V, in order to guarantee the accurate output current, do not set the Iout to over 40mA, please.

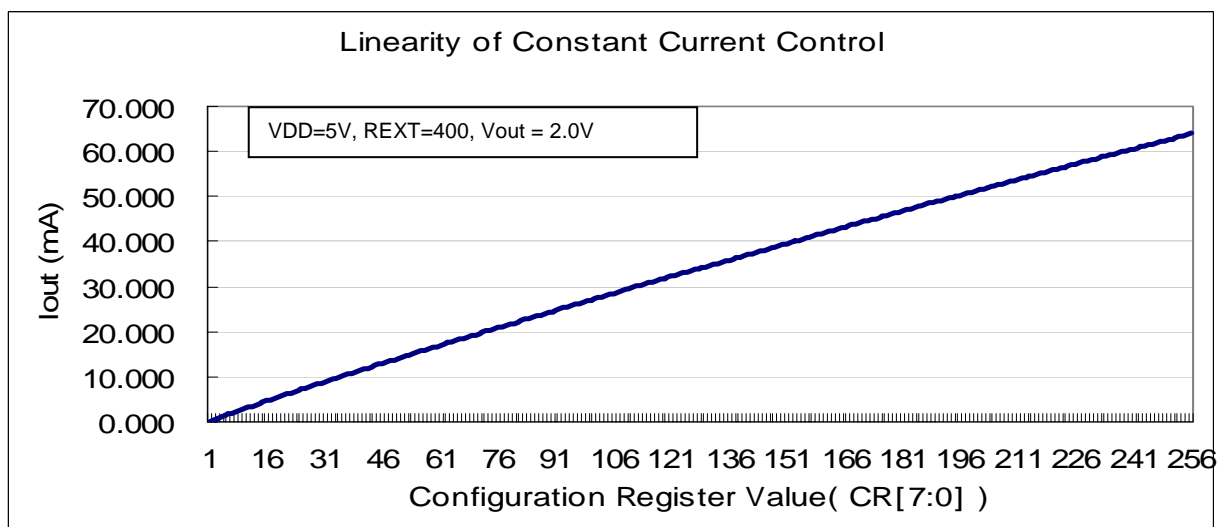
CONSTANT OUTPUT CURRENT

The LD1071 provides a constant current output characteristics for LED display application. The pin to pin deviation is max +/- 3% and chip to chip deviation is max +/- 6%.

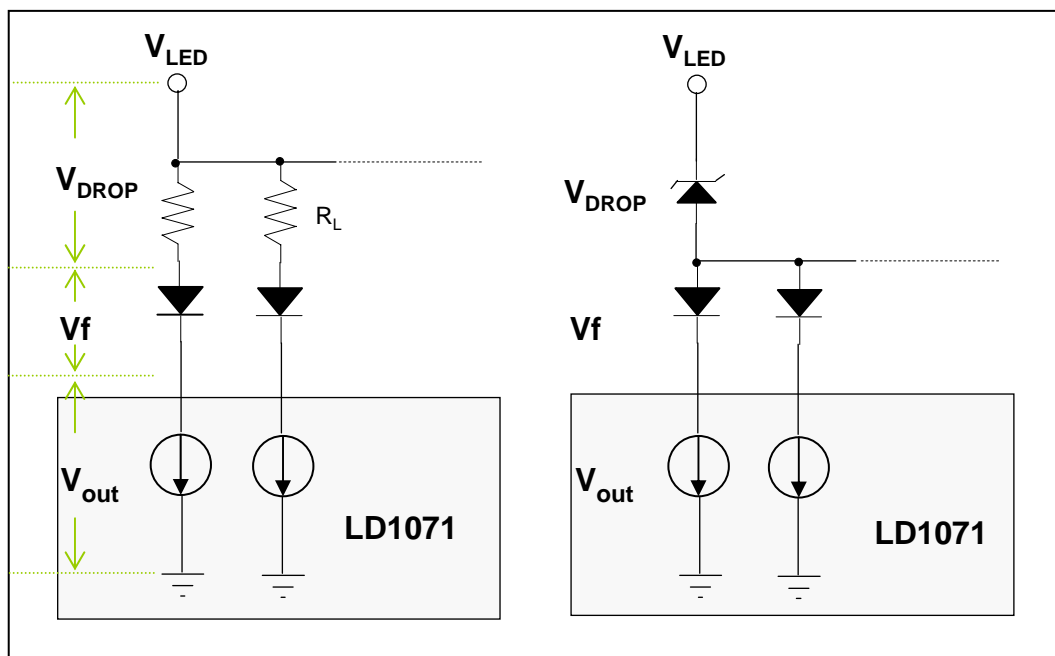


CONSTANT CURRENT CONTROL

The LD1071 provides a excellent Iout linearity by setting the Configuration Register for global brightness control. The following graph shows the linearity example under the condition at VDD=5V, REXT=400 ohms and Vout = 2.0V.



LED SUPPLY VOLTAGE(VLED)



It is very important to select the proper value of Load Resistor(R_L). Because the optimal V_{OUT} value guarantees the constant output current and long life time of LED driver IC without over power consumption.

For example, let's calculate the Load Resistor value at V_{LED}=5V, I_{out}=20mA, LED Forward Voltage(V_f)=3V.

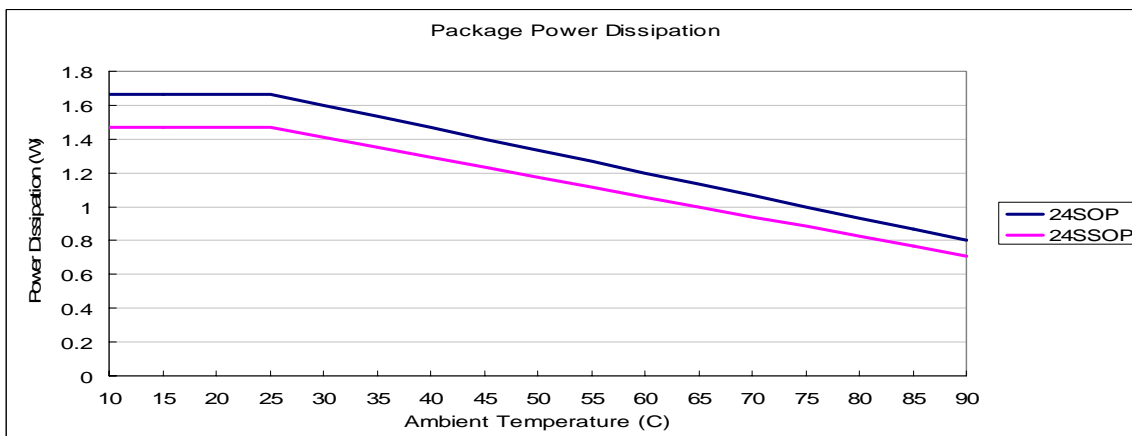
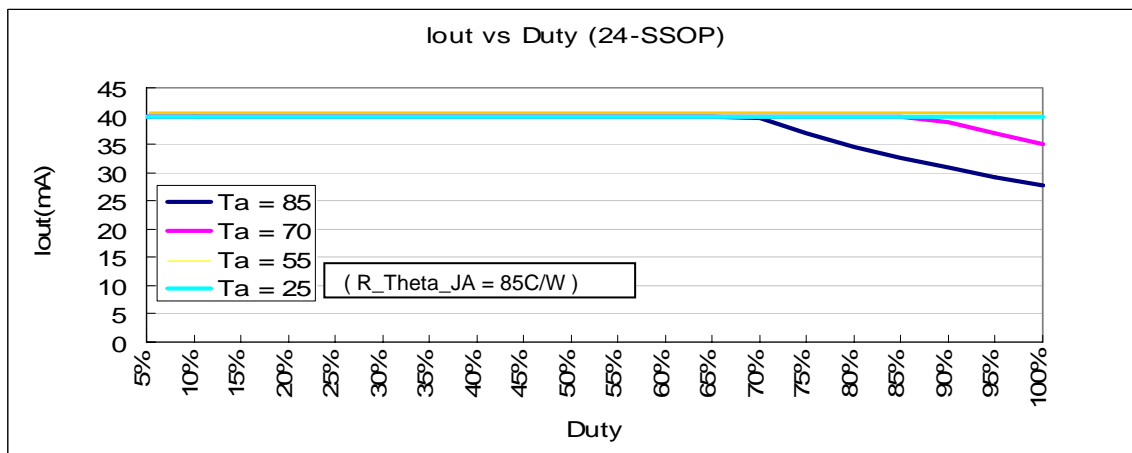
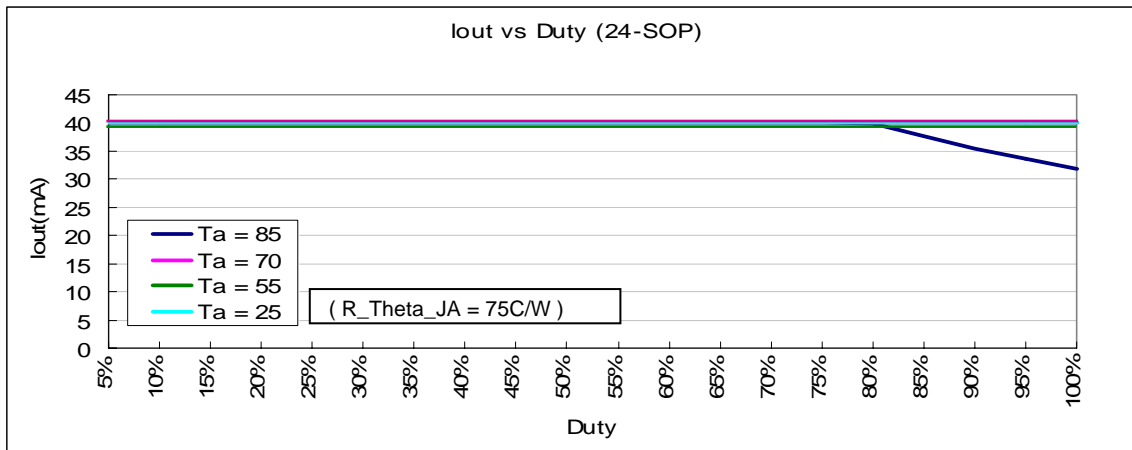
- 1) The full current of LD1018 = 20mA x 16 (channels) = 320mA
- 2) The power consumption is 320mA x V_{OUT} voltage.
 - when V_{OUT} = 1V, the power consumption is 320mW.
 - when V_{OUT} = 2V, the power consumption is 640mW.

$$\begin{aligned}
 \text{Therefore, the Load Resistor (R}_L\text{)} &= (V_{LED} - V_{OUT} - V_f) / I_{out} \\
 &= (5V - V_{OUT} - 3V) / 20mA \\
 &= \underline{40} \text{ (When V}_{OUT} = 1.2V\text{)}
 \end{aligned}$$

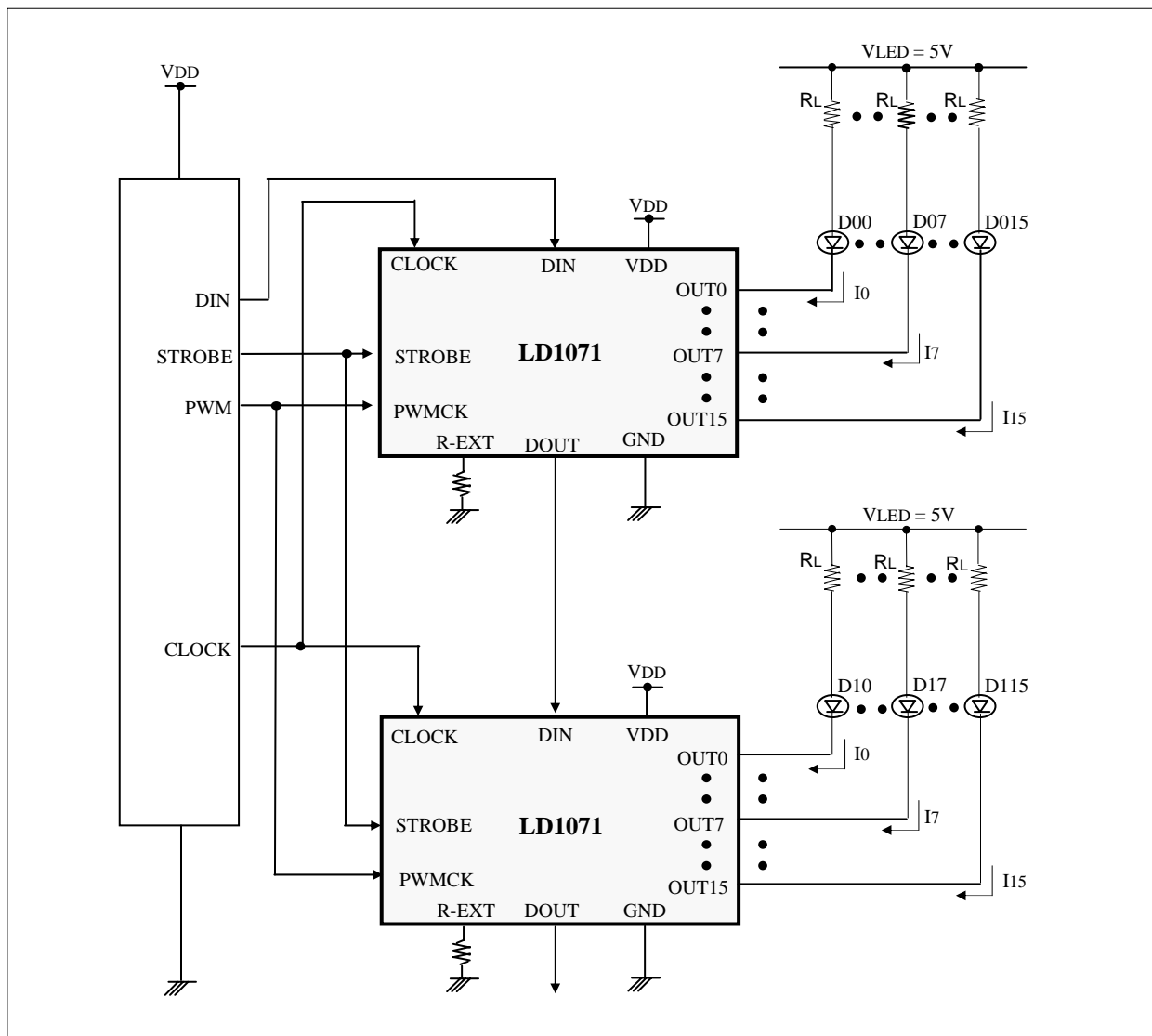
PACKAGE POWER DISSIPATION(PD)

The LD1071 provides many package options such as 24-SOP package and 24-SSOP package. The maximum allowable package power dissipation is determined as $PD(max) = (T_j - T_a) / R_{\theta JA}$. When 16 output ports are turned on simultaneously, the actual power package dissipation is $PD(act) = (I_{DD} \times V_{DD}) + (I_{OUT} \times Duty \times V_{OUT} \times 16)$. Therefore, to keep that $PD(act)$ is less equal than $PD(max)$. The maximum allowable output current as a function of duty cycle is:

$$I_{OUT} = \{[(T_j - T_a) / R_{\theta JA}] - (I_{DD} \times V_{DD})\} / V_{OUT} / Duty / 16 \quad \text{where } T_j = 150^\circ\text{C}$$

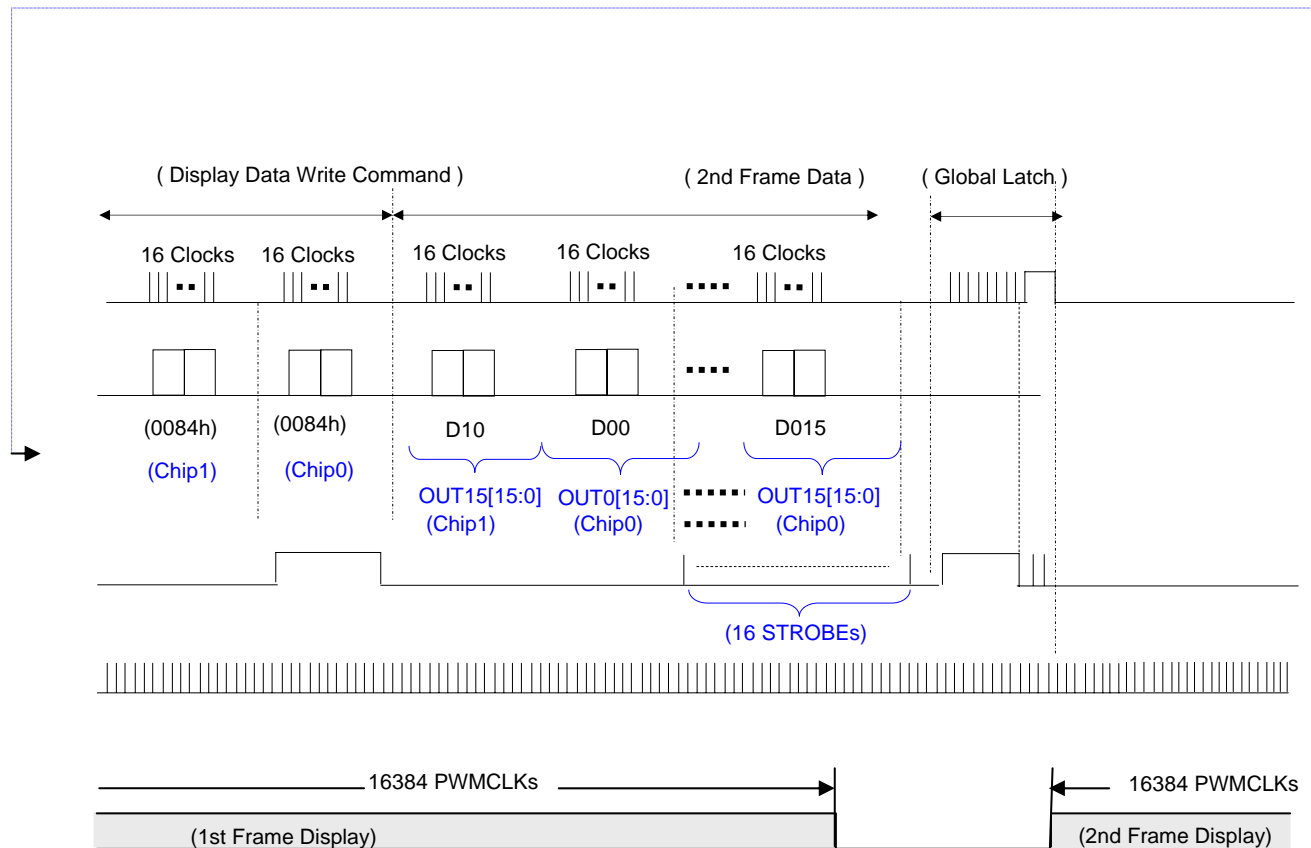
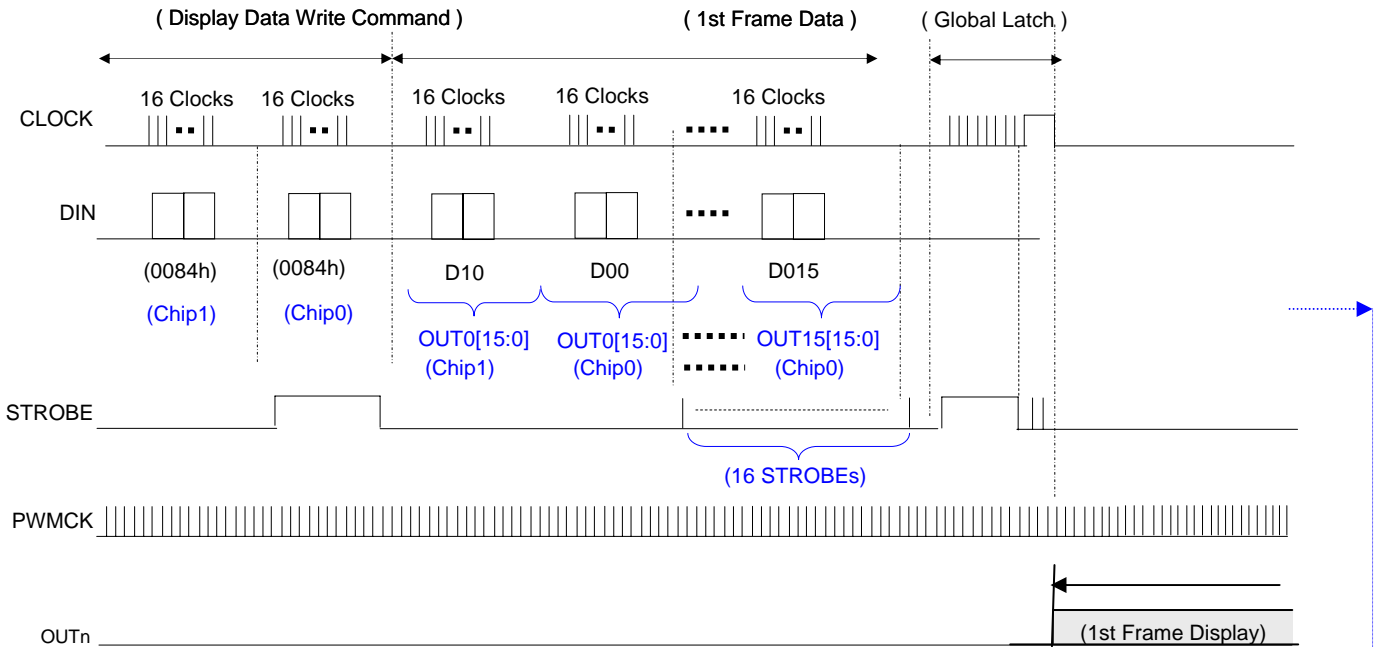


APPLICATION CIRCUIT 1 (16x2 Static Type)

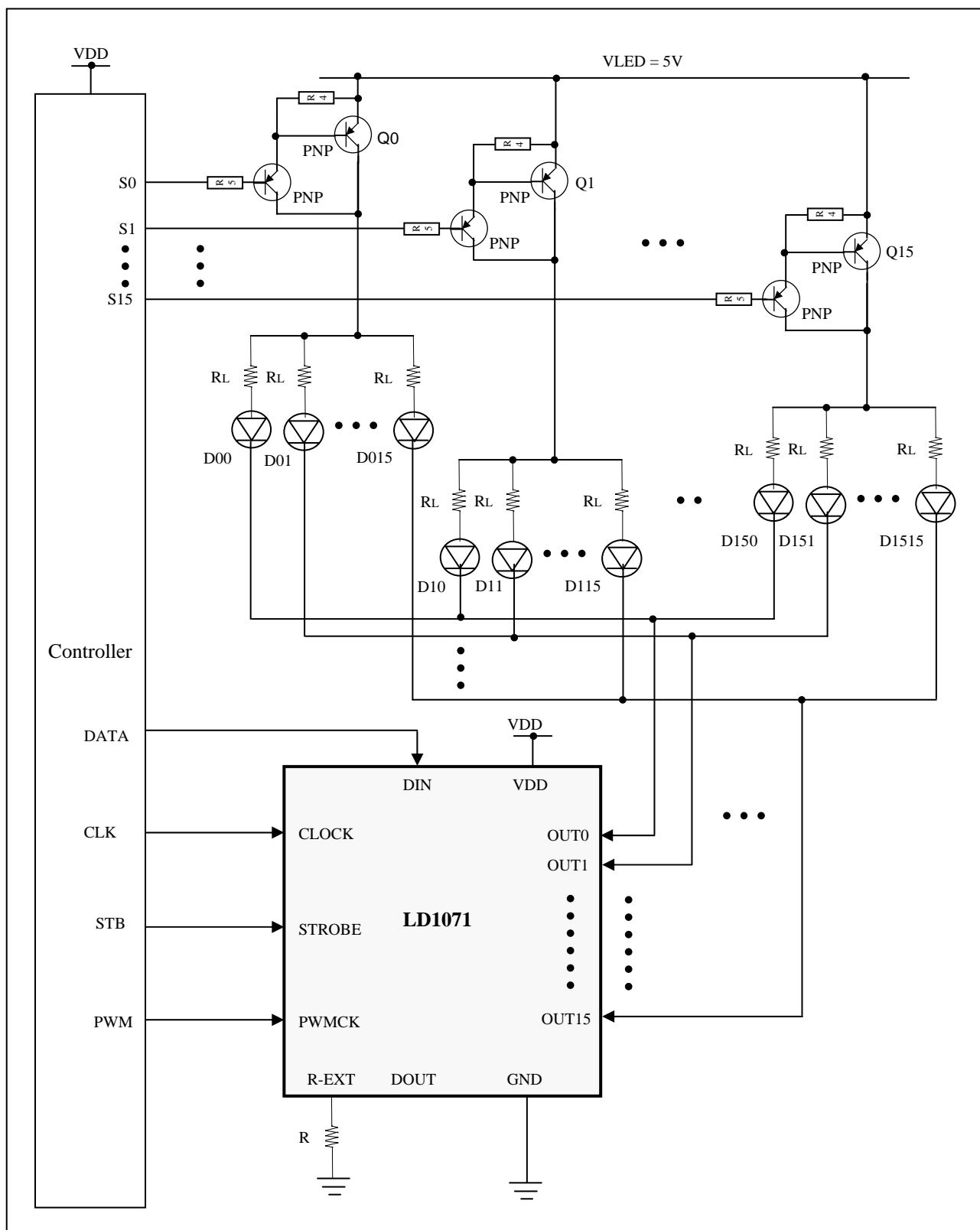


Data & Control Signal Connection for 16x2 Static Type Application

TIMING DIAGRAM FOR APPLICATION CIRCUIT 1 (Default One Shot Mode)

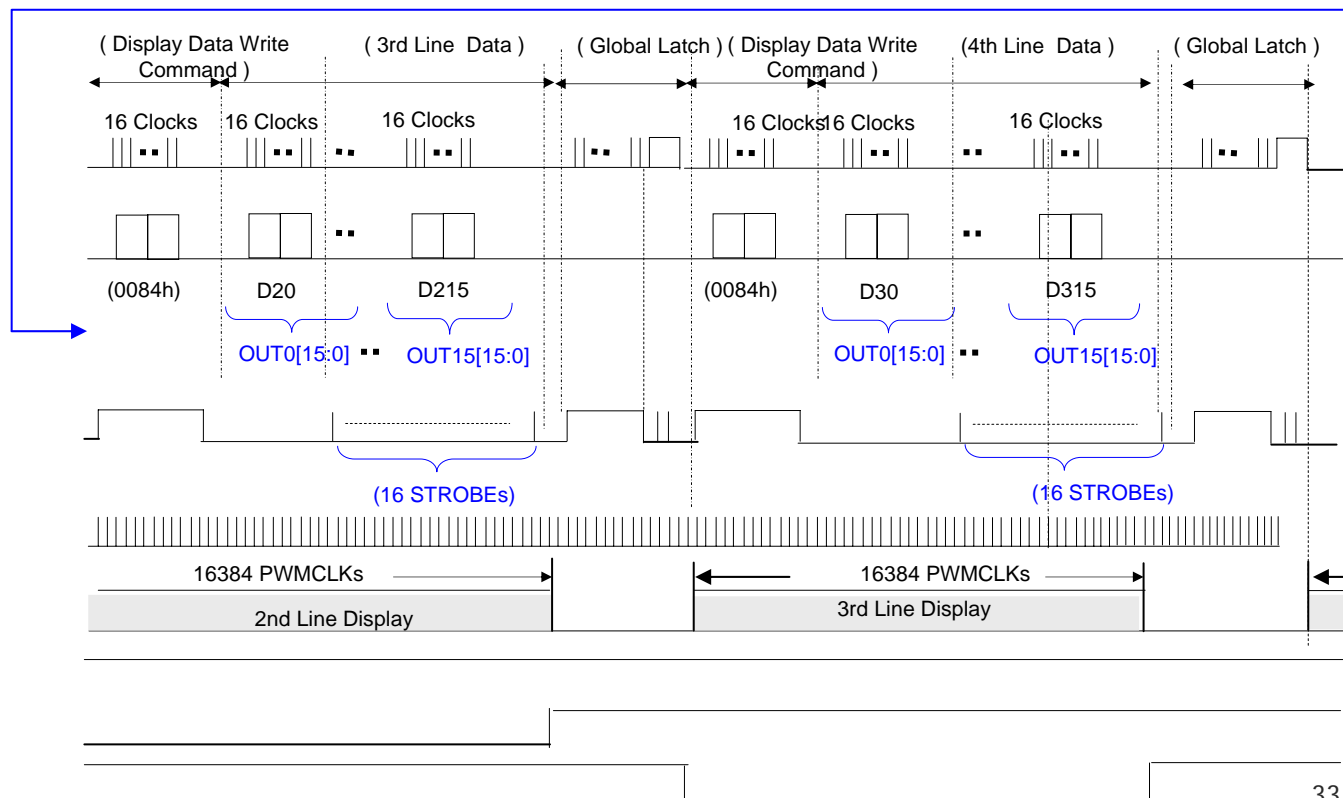
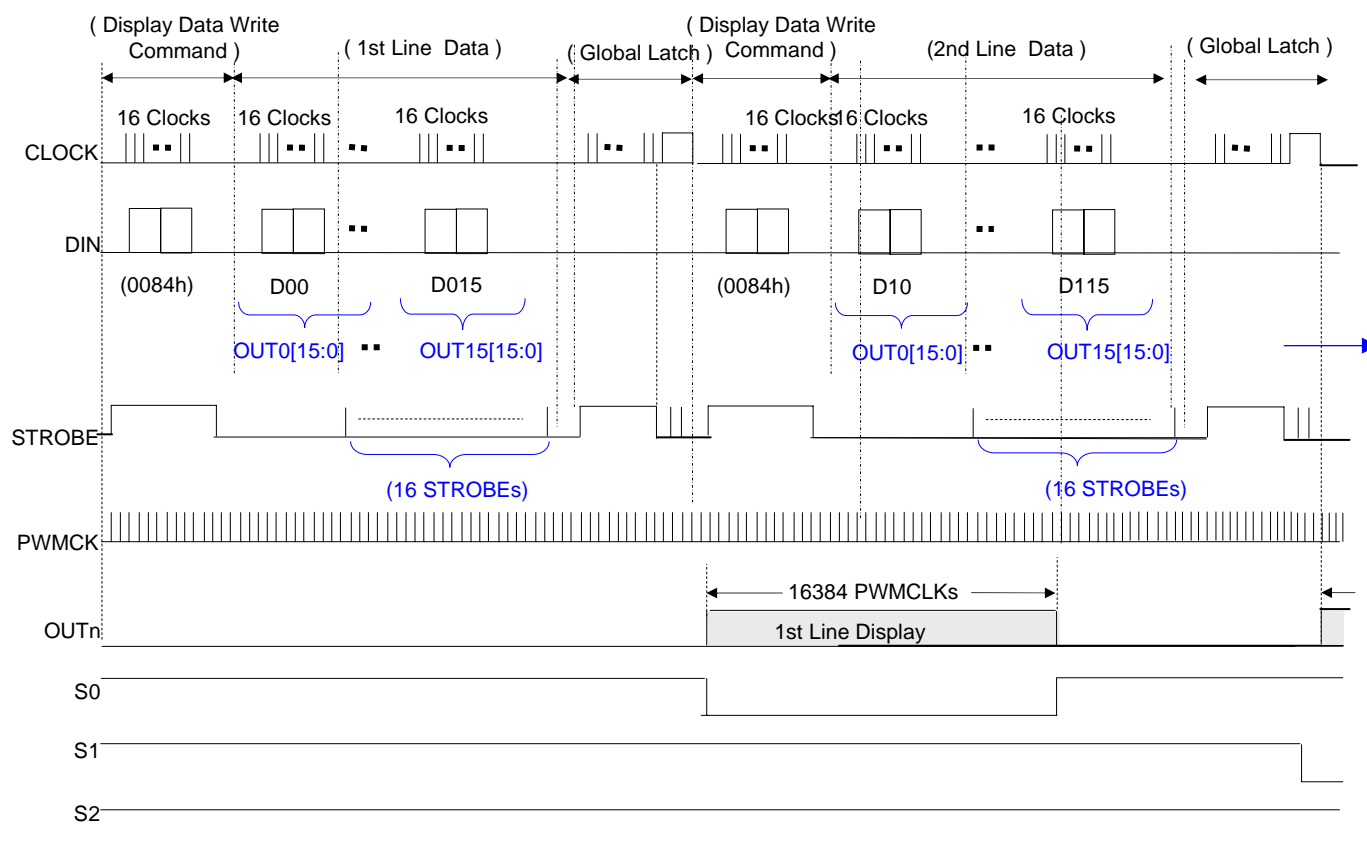


APPLICATION CIRCUIT 2 (16x16 Dynamic Type)



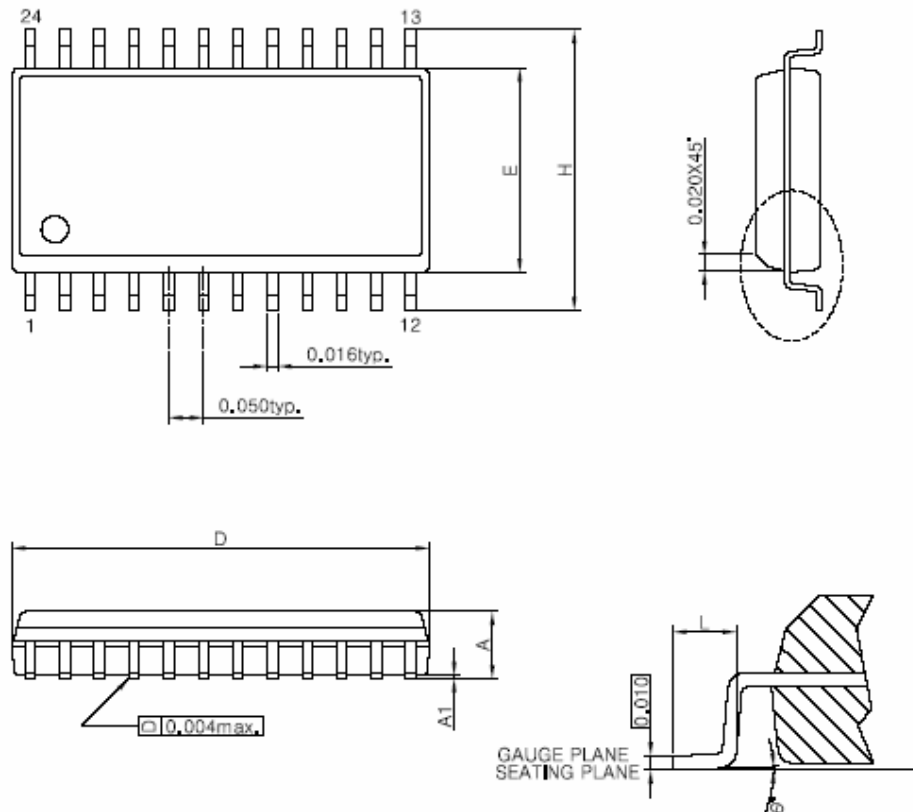
Data & Control Signal Connection for 16x16 Dynamic Type Application

TIMING DIAGRAM FOR APPLICATION CIRCUIT 2 (Default One Shot Mode)



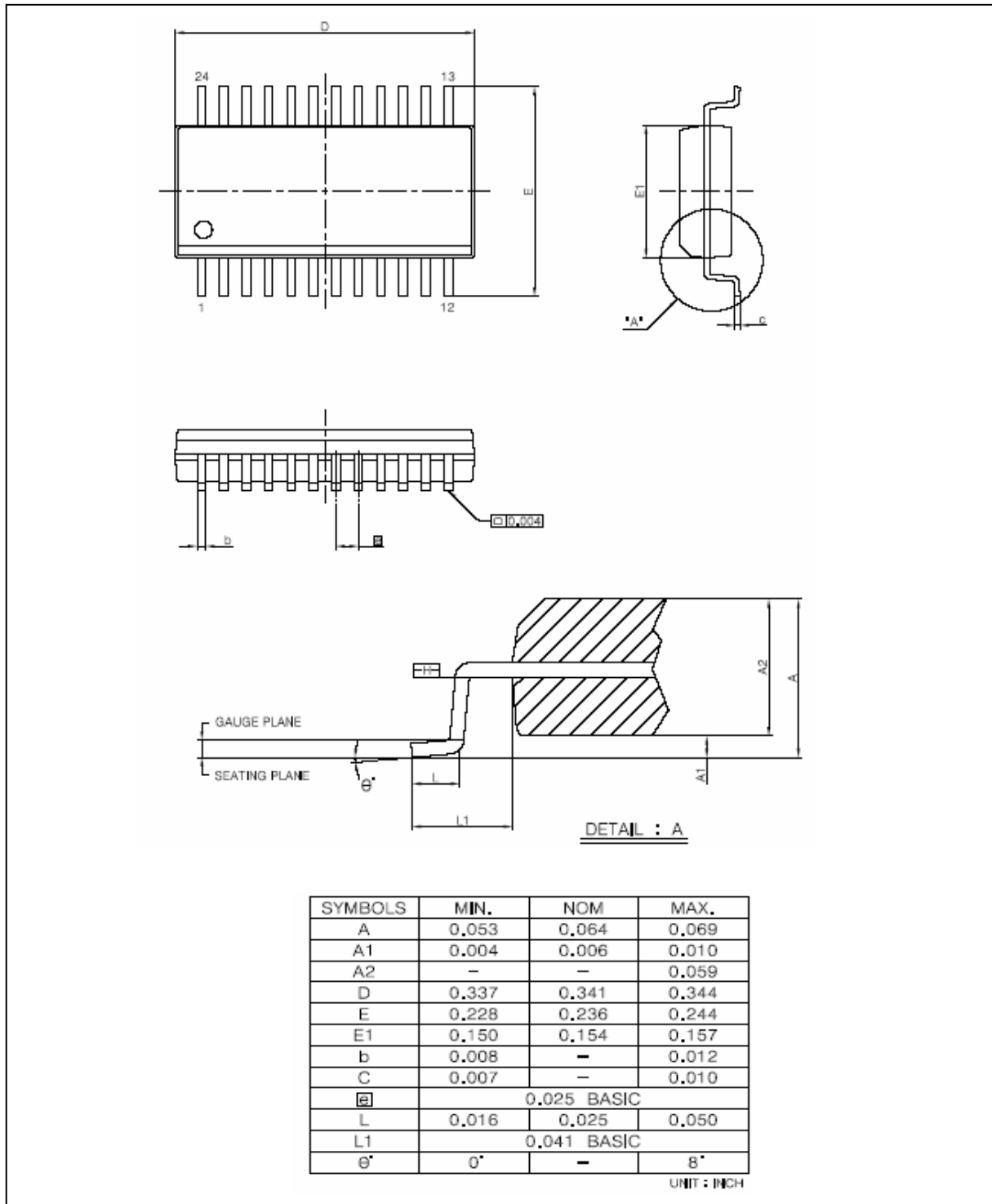
PACKAGE INFORMATION

LD1071-SP (SOP 24)



| SYMBOLS | MIN. | NOM | MAX. |
|---------|-------|-------|-------|
| A | — | — | 0.104 |
| A1 | 0.004 | — | — |
| D | 0.612 | 0.618 | 0.624 |
| E | 0.292 | 0.296 | 0.299 |
| H | 0.405 | 0.412 | 0.419 |
| L | 0.021 | 0.031 | 0.041 |
| θ | 0 | 4 | 8 |

UNIT : INCH

LD1071-SS (SSOP 24 – 150)


The products listed herein are designed for ordinary electronic applications, such as electrical applications, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instrument, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.

LDT will not take any responsibilities regarding the misuse of the products mentioned above. Anyone who purchases any products described herein with the above-mentioned intention or with such misused application should accept full responsibility and indemnify. LDT and its distributors and all their officers and employees shall defend jointly and severally against any and all claims and litigation and all damages, cost and associated with such intention and manipulation.