VGA Port Companion Circuit For Monitors

Features

- Includes ESD protection, level-shifting, buffering and sync impedance matching
- VESA VSIS Version 1 Revision 2 Compatible Interface
- Supports Optional NAVI Signalling requirements
- 7 channels of ESD protection for all VGA port connector pins meeting IEC-61000-4-2 Level 4 ESD requirements (±8kV contact discharge)
- Very low loading capacitance from ESD protection diodes on VIDEO lines, 3pF maximum
- Schmitt triggered input buffers for HSYNC and VSYNC lines
- Bi-directional level shifting N-channel FETs provided for DDC_CLK & DDC_DATA channels
- Backdrive protection on all lines
- Compact 16-lead QSOP package

Applications

- VGA and DVI-I ports in:
  - Monitors
  - Set Top Boxes

Product Description

The CM2006 connects between the VGA or DVI-I port connector and the internal analog or digital flat panel controller logic. The CM2006 incorporates ESD protection for all signals, level shifting for the DDC signals and buffering for the SYNC signals. ESD protection for the video, DDC and SYNC lines is implemented with low-capacitance current steering diodes.

All connector interface pins are designed to safely handle the high current spikes specified by IEC-61000-4-2 Level 4 (±8kV contact discharge). The ESD protection for the DDC, SYNC and VIDEO signal pins is designed to prevent "back current" when the device is powered down while connected to a video source that is powered up.

Separate positive supply rails are provided for the VIDEO / SYNC signals and DDC signals to facilitate interfacing with low voltage video controller ICs and microcontrollers to provide design flexibility in multi-supply-voltage environments.

Two Schmitt-Triggered non-inverting buffers redrive and condition the HSYNC and VSYNC signals from the video Connector (SYNC1, SYNC2). These buffers accept VESA VSIS compliant TTL input signals and convert them to CMOS output levels that swing between Ground and V_{CC}.

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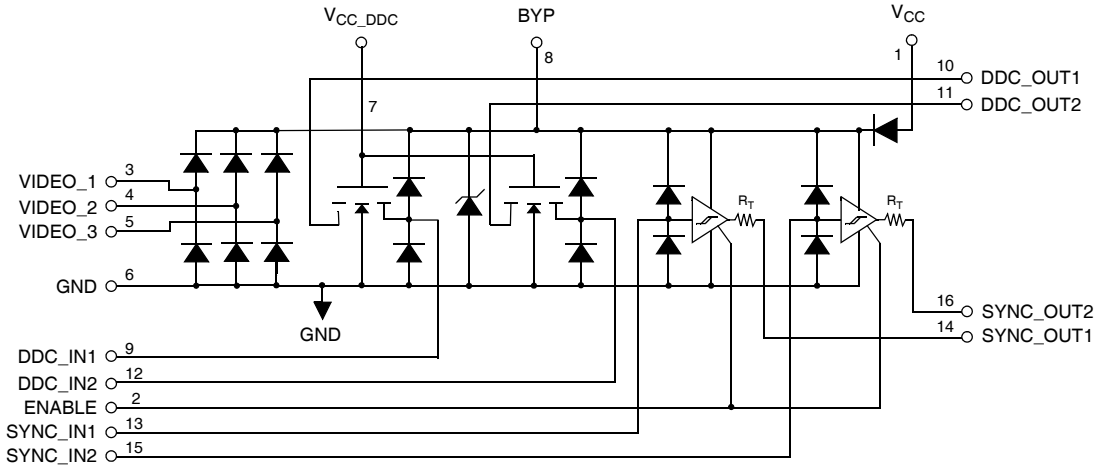
Simplified Electrical Schematic

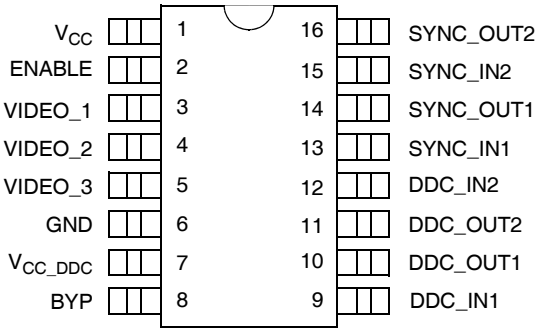


Product Description (cont'd)

Two N-channel MOSFETs provide the level shifting function required when the DDC controller or EDID EEPROM is operated at a lower supply voltage than the monitor. The gate terminals for these MOSFETS (V_{CC_DDC}) should be connected to the supply rail (typically 3.3V, 2.5V etc.) that supplies power to the transceivers of the DDC controller.

PACKAGE / PINOUT DIAGRAM

Top View



16 Pin QSOP

Note: This drawing is not to scale.

PIN DESCRIPTIONS

LEAD(s)	NAME	DESCRIPTION
1	V_{CC}	This is a supply input for the SYNC_1 and SYNC_2 level shifters, video protection and the DDC circuits.
2	ENABLE	Active high enable. Disables the Sync buffer outputs when low.
3	VIDEO_1	Video signal ESD protection channel. This pin is typically tied one of the video lines between the controller device and the video connector.
4	VIDEO_2	Video signal ESD protection channel. This pin is typically tied one of the video lines between the controller device and the video connector.
5	VIDEO_3	Video signal ESD protection channel. This pin is typically tied one of the video lines between the controller device and the video connector.
6	GND	Ground reference supply pin.
7	V_{CC_DDC}	This is an isolated supply input for the DDC_1 and DDC_2 level-shifting N-FET gates.
8	BYP	An external 0.22uF bypass capacitor is required on this pin.
9	DDC_IN1	DDC signal input. Connects to the video connector side of one of the DDC lines.signal output.
10	DDC_OUT1	DDC signal output. Connects to the monitor DDC logic.
11	DDC_OUT	DDC signal output. Connects to the monitor DDC logic.
12	DDC_IN2	DDC signal input. Connects to the video connector side of one of the DDC lines
13	SYNC_IN1	Sync signal buffer input. Connects to the video connector side of one of the sync lines.
14	SYNC_OUT1	Sync signal buffer output. Connects to the monitor SYNC logic.
15	SYNC_IN2	Sync signal buffer input. Connects to the video connector side of one of the sync lines.
16	SYNC_OUT2	Sync signal buffer output. Connects to the monitor SYNC logic.

Ordering Information

PART NUMBERING INFORMATION					
		Standard Finish		Lead-free Finish	
Pins	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
16	QSOP	CM2006-02QS	CM2006-02QS	CM2006-02QR	CM2006-02QR

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
V_{CC_DDC} and V_{CC} Supply Voltage Inputs	[GND - 0.5] to +6.0	V
DC Voltage at Inputs VIDEO_1, VIDEO_2, VIDEO_3 DDC_IN1, DDC_IN2 DDC_OUT1, DDC_OUT2 SYNC_IN1, SYNC_IN2, ENABLE	 [GND - 0.5] to [V_{CC} + 0.5] [GND - 0.5] to 6.0 [GND - 0.5] to 6.0 [GND - 0.5] to [V_{CC} + 0.5]	 V V V V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-40 to +150	°C
Package Power Rating (T_A=25°C)	500	mW

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Operating Temperature Range	-40 to +85	°C
V_{CC}	5	V

Specifications

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{CC_DDC}	V_{CC_DDC} Supply Current	V_{CC_DDC} = 5.0V			10	µA
I_{CC}	V_{CC} Supply Current	V_{CC} = 5V; SYNC inputs at GND or V_{CC}; SYNC outputs unloaded			1	mA
		V_{CC} = 5V; SYNC inputs at 3.0V; SYNC outputs unloaded			2.0	mA
V_F	ESD Diode Forward Voltage	I_F = 10mA			1.0	V
V_{IH}	Logic High Input Voltage	V_{CC} = 5.0V; Note 2	2.0			V
V_{IL}	Logic Low Input Voltage	V_{CC} = 5.0V; Note 2			0.5	V
V_{HYS}	Hysteresis Voltage	V_{CC} = 5.0V; Note 2		400		mV
V_{OH}	Logic High Output Voltage	I_{OH} = 0mA, V_{CC} = 5.0V; Note 2	4.0			V
V_{OL}	Logic Low Output Voltage	I_{OL} = 0mA, V_{CC} = 5.0V; Note 2			0.15	V
R_{OUT}	SYNC Driver Output Resistance	V_{CC} = 5.0V; SYNC Inputs at GND or 3.0V	7	15	24	Ω
I_{IN}	Input Current VIDEO Inputs	V_{CC} = 5.0V; V_{IN} = V_{CC} or GND			±10	µA
	SYNC_IN1, SYNC_IN2 Inputs	V_{CC} = 5.0V; V_{IN} = V_{CC} or GND			±10	µA
I_{OFF}	Level Shifting N-MOSFET "OFF" State Leakage Current	(V_{CC_DDC} - V_{DDC_IN}) < 0.4V; V_{DDC_OUT} = V_{CC_DDC}			10	µA
		(V_{CC_DDC} - V_{DDC_OUT}) < 0.4V; V_{DDC_IN} = V_{CC_DDC}			10	µA
$I_{BACKDRIVE}$	Current conducted from input pins when Vcc is powered down.	V_{CC} < V_{INPUT_PIN} ; Note 6		10		µA
V_{ON}	Voltage Drop Across Level-shifting N-MOSFET when "ON"	V_{CC_DDC} = 2.5V; V_S = GND; I_{DS} = 3mA;			0.18	V
C_{IN_VID}	VIDEO Input Capacitance	V_{CC} = 5.0V; V_{IN} = 2.5V; f = 1MHz; Note 4			3	pF
		V_{CC} = 2.5V; V_{IN} = 1.25V; f = 1MHz; Note 4			3.5	pF
t_{PLH}	SYNC Driver L => H Propagation Delay	C_L = 50pF; V_{CC} = 5.0V; Input t_R and t_F < 5ns			12	ns
t_{PHL}	SYNC Driver H => L Propagation Delay	C_L = 50pF; V_{CC} = 5.0V; Input t_R and t_F < 5ns			12	ns
t_R, t_F	SYNC Driver Output Rise & Fall Times	C_L = 50pF; V_{CC} = 5.0V; Input t_R and t_F < 5ns		3		ns
V_{ESD1}	ESD Withstand Voltage, Sync_out pins only	V_{CC} = 5V; Notes 3, 4, & 5	± 2			kV
V_{ESD}	ESD Withstand Voltage	V_{CC} = 5V; Notes 3, 4, & 6	± 8			kV

Note 1: All parameters specified over standard operating conditions unless otherwise noted

Note 2: These parameters apply only to the SYNC drivers. Note that $R_{OUT} = R_T + R_{BUFFER}$.

Note 3: Per the IEC-61000-4-2 International ESD Standard, Level 4 contact discharge method. BYP and V_{CC} must be bypassed to GND via a low impedance ground plane with a 0.22µF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulses can be positive or negative with respect to GND. Applicable pins are: VIDEO_1, VIDEO_2, VIDEO_3, SYNC_IN1, SYNC_IN2, DDC_IN1 and DDC_IN2. All pins are ESD protected to the industry standard ±2kV Human Body Model (MIL-STD-883, Method 3015).

Note 4: This parameter is guaranteed by design and characterization.

Note 5: This specification applies to the SYNC_OUT pins only.

Note 6: Applicable pins are: VIDEO_1, VIDEO_2, VIDEO_3, SYNC_IN1, SYNC_IN2, DDC_IN1 and DDC_IN2.

Application Information

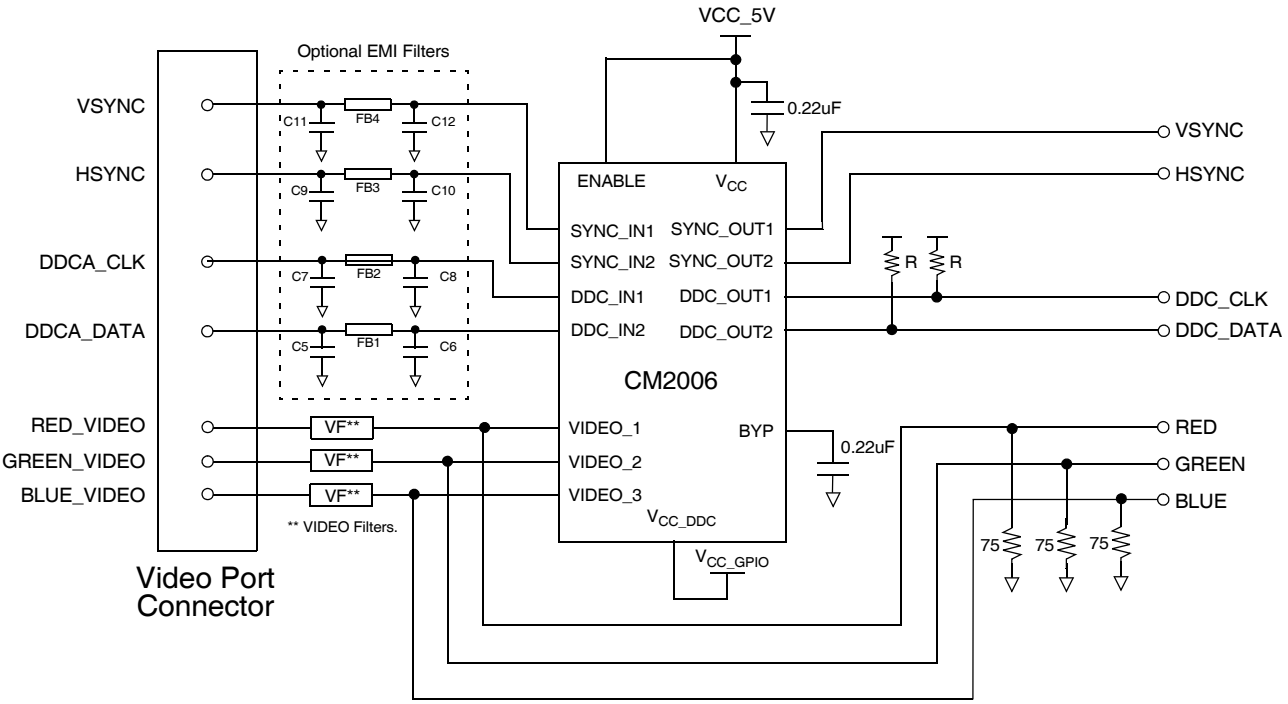


Figure 1. Typical Application Connection Diagram

NOTES

1 The CM2006 should be placed as close to the VGA or DVI-I connector as possible.

2 The ESD protection channels VIDEO_1, VIDEO_2, VIDEO_3 may be used interchangeably between the R, G, B signals.

3 If differential video signal routing is used, the $\overline{\text{RED}}$, $\overline{\text{BLUE}}$, and $\overline{\text{GREEN}}$ signal lines should be terminated with external 37.5 ohm resistors.

4 "VF" are external video filters for the RGB signals.

5 Supply bypass capacitors C1 and C2 must be placed immediately adjacent to the corresponding Vcc pins. Connections to the Vcc pins and ground plane must be made with minimal length copper traces (preferably less than 5mm) for best ESD protection.

6 The bypass capacitor for the BYP pin has been omitted in this diagram. This results in a reduction in the maximum ESD withstand voltage at the DDC_OUT pins from ±8kV to ±2kV. If 8kV ESD protection is required, a 0.22µF ceramic bypass capacitor should be connected between BYP and ground.

7 The SYNC buffers may be used interchangeably between HSYNC and VSYNC.

8 The EMI filters at the SYNC_OUT and DDC_OUT pins (C5 to C12, and Ferrite Beads FB1 to FB4) are for reference only. The component values and filter configuration may be changed to suit the application.

9 The DDC level shifters DDC_IN, DDC_OUT, may be used interchangeably between DDCA_CLK and DDCA_DATA.

10 R1, R2 are optional. They may be used, if required, to pull the DDC_CLK and DDC_DATA lines to VCC_5V when no monitor is connected to the VGA connector. If used, it should be noted that "back current" may flow between the DDC pins and VCC_5V via these resistors when VCC_5V is powered down.

Mechanical Details

QSOP Mechanical Specifications

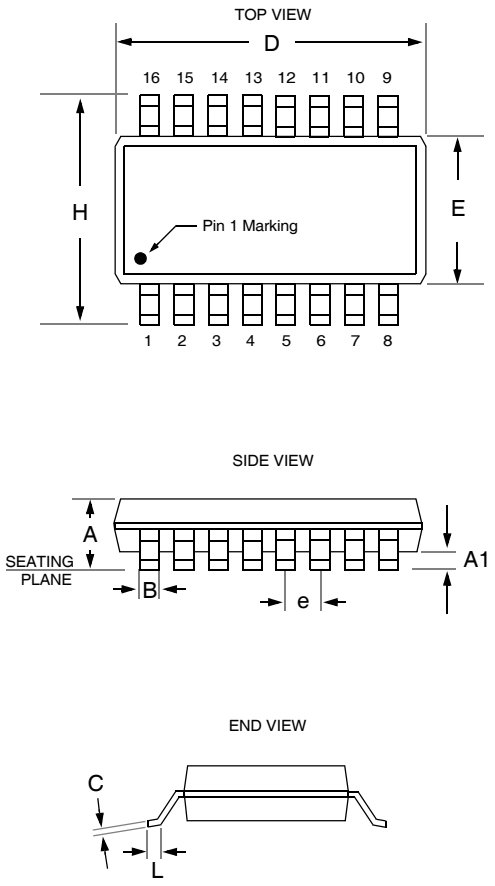
CM2006 devices are packaged in 16-pin QSOP packages. Dimensions are presented below.

For complete information on the QSOP-16 package, see the California Micro Devices QSOP Package Information document.

PACKAGE DIMENSIONS				
Package	QSOP (JEDEC name is SSOP)			
Pins	16			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.20	0.30	0.008	0.012
C	0.18	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.81	3.98	0.150	0.157
e	0.64 BSC		0.025 BSC	
H	5.79	6.19	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	100 pcs*			
# per tape and reel	2500 pcs			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for QSOP-16