**Booth Kittson**

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**SUMMARY**

I am the owner of Red Beauty Textiles, an online only shop for yarn and fabric.

I am currently a student at The Coding Boot Camp at University of Texas in Austin with graduation date in October 2016.

After 30 years in a successful career as an Analog Layout Designer, I needed a change. I had stagnated and become complacent in my job. I had a part time business selling yarn and fabric online and decided to try my hand as a full time business owner. During the setup of several successive websites on various ecommerce platforms, I've become aware of two things. The first is that I have more interest in the technical details of my sites than actually selling the products. The second is that there seems to be a dearth of good web developers focussing on user (customer) experience and design.

I have always been interested in programming. My job as a Layout Designer required mastering complicated 2D CAD and verification software; part of that mastery included some programming in the associated application specific languages. With this and a bit of Perl under my belt I decided to explore web development as a third career. Coincident with this choice, the Coding Boot Camp was opened for enrollment.

**EXPERIENCE**

**Red Beauty Textiles (redbeautytextiles.com)** 2011 - present

***Owner***

Red Beauty Textiles is an online only fabric and yarn store. I have been running RBT part time since 2011 and full time since 2014. My duties are inclusive of running an online retail website.

* Evaluate online ecommerce selling platforms, if necessary interview and hire advanced technical help for customization
* Migration from Zencart php opensource platform to ecommerce package hosted by Shopify
* Shopify minor theme customization using css/javascript/jquery in a liquid framework
* Responsible for online graphics, including “look” of shop, logos, and new graphics necessary for online advertising or social media using Photoshop, Inkscape, Adobe Illustrator
* Product presentation including extensive photography and photo editing (Photoshop)
* Product description writing, including SEO descriptions, titles, keywords, etc.
* Assessment of sales trends to evaluate future product lines to carry
* Google Analytics, Google Adwords, Facebook advertising
* Social media posting including Facebook and Wordpress, and periodic newsletter
* Additionally maintain second website, Purple Sage Yarns, and five Etsy marketplace shops
* Customer service

**Broadcom (division of Broadcom Ltd.)** 2010 – 2014

***Sr. Layout Engineer***

* Analog layout design in 28nm, 20nm TSMC processes for SOC Tuners and Satelllite products
* Layout design of RF circuits including LNAs, TX and RX s, padrings, I/O cells, and custom devices
* Top level floorplanning, routing, and assembly. Common centroid-ing, device matching
* LVS/DRC verification using Assura and Calibre, VXL, Cadence Virtuoso, Composer

**Contract, Layout Designer** 2005 – 2010

***Qualcomm, Inc., Austin, TX***

* Layout design of 28nm TSMC RF test chips using Cadence 6.1 release
* Planning and layout of synthesizer and LDO blocks, including loop filters, regulators, VCO’s, opamps in 65nm TSMC process. Calibre DRC/LVS
* Complex matching/balancing of devices including dummy device placement, common centroid-ing, minimization of resistance for routing
* Directing layout designers on sub-blocks; layout techniques for DFM considerations, IR drop, electromigration

***Sequoia Communications, Inc.***

* Layout design of RF circuits in IBM cmos7wl .13 process, TSMC 65nm
* Responsible for revision of top level blocks consisting of mixers, tx and rx basebands, and VCOs
* Device matching and dummy device placement
* Conduit wiring of sensitive signals
* Assisted with top level routing and physical verification
* Assura and Calibre DRC/LVS, Cadence toolset
* SKILL applications programming

***Anokiwave, Inc.***

* Layout design of RF circuits in Jazz process
* Cadence toolset, Assura

***Newport Media, Inc.***

* Lead layout design of multiple RF circuits for SOC applications in TSMC 65nm process
* Top level planning
* Layout of LNAs, VCOs, opamps, filters, SDAs
* Device matching and mimicing of parasitics
* Shielded wiring/twisted pairs/conduiting
* Directing junior designers
* Top level routing and physical verification using Calibre and Assura
* Tape out duties
* SKILL applications programming

***RF Magic, Inc.***

* Layout design
* Jazz and ST processes

***Qualcomm, Inc., San Diego, CA***

* Layout design .65nm process

**RF Magic, Inc. (now MaxLinear)** 2004 – 2005

***IC Layout Manager***

* Managed back-end layout design of RFIC products
* Managed staff of direct and contract layout
* Led layout design of RF circuits including filters, LNAs, VCOs, padrings, I/O cells, and custom devices
* Top level floorplanning, routing, and assembly. Common centroid-ing, device matching
* Minimization of parasitics
* LVS/DRC verification using Assura and Calibre, VXL, Virtuoso, Composer

**Vativ Technologies, Inc.**  2002 – 2004

***Senior Layout Designer***

* Layout design of analog and digital circuits
* Top level floorplanning, assembly
* LVS/DRC verification using Assura and Calibre, VXL, Virtuoso, Composer
* SKILL and Perl programming for layout and netlisting applications

**Peregrine Semiconductor, Inc.** 2001 – 2002

***Senior CAD Engineer***

* Responsible for creation and maintenance of Diva/Assura DRC, ERC, EXTRACT, and LVS rules files
* SKILL programming for layout applications and utilities
* Pcell coding and maintenance
* Layout design of analog and photonic circuits
* LVS/DRC using Diva and Assura, VXL, Virtuoso, Composer

**Centaur Technology, Inc. (aq. by Via Technologies)** 1999 – 2001

***Layout Designer***

* Layout design of complex digital microprocessors including custom blocks and datapath elements using .13 TSMC eight metal process
* Responsible for writing and maintaining Diva DRC
* LVS/DRC using Mentor Graphics Calibre, VXL, Virtuoso, Composer

**Cadence Design Systems, Inc.** 1997 – 1999

***Principal Consultant***

* Wide range of duties including new standard cell library qualification using Silicon Ensemble, construction of RCX (parasitic extraction) rules sets for Vampire, construction of Diva DRC/LVS rules sets, course development for Austin Design Center
* Supported Dracula, Diva, and Vampire (Assura)
* Wrote and edited Perl scripts

**Consultant, Layout Design** 1994 – 1997

**Philips Semiconductors** 1993 – 1994

***Sr. Mask Design Engineer, Technical Instructor***

* Project lead for high speed BiCMOS/analog designs
* Successfully directed transition from in-house CAD tools to Cadence Opus software
* Trained design staff in Unix and Cadence tools
* Dracula/Diva support

**Cadence Design Systems, Inc.** 1992 – 1993

***Sr. Technical Instructor for Dracula***

* Developed and maintained Dracula courses using Framemaker
* Taught on and off site technical classes
* Customer support for Virtuoso, DLE (VXL), Diva, and Dracula Cadence products

**Tera Microsystems, Inc.** 1990 – 1992

***Supervisor, Layout Engineer***

* Hired and supervised layout staff, project lead on all chips; Unix training and support

prior work history available upon request