<table>
<tr><td>Semester 1</td><td colspan="3"></td></tr>
<tr><td>Course Code</td><td colspan="3">CSC 541 2.0</td></tr>
<tr><td>Course Name</td><td colspan="3">Computer System Architecture</td></tr>
<tr><td>Credit Value</td><td colspan="3">2.0</td></tr>
<tr><td>Core/Optional</td><td colspan="3">Core</td></tr>
<tr><td rowspan="2">Hourly Breakdown</td><td>Theory</td><td>Practical/Tutorial</td><td>Independent Learning</td></tr>
<tr><td>28</td><td></td><td>72</td></tr>
<tr><td colspan="4">Course Aim/Intended Learning Outcomes:

At the completion of this course student will be able to

➢ Explain the architecture of a processor and a computer system.
➢ Appreciate the concept of an ISA and the nature of a machine level instruction in terms of its functionality and use of resources.
➢ Be aware of the various classes of instructions.
➢ Compile high-level instructions to assembly instructions and then to machine language instructions.
➢ Identify various types of buses in a computer system and understand how devices compete for a bus and are granted access to the bus.
➢ Describe various types of memory, their errors and techniques used for fault tolerance
➢ Justify the need of a memory hierarchy in order to reduce the memory latency.
➢ Explain the organization of cache memory.
➢ Measure the performance of a computer, and interpret results.
➢ Discuss the concept of parallel processing, and identify the relationship between parallelism and performance.</td></tr>
<tr><td colspan="4">Course Content: (Main topics, Sub topics)

Processor and System Architecture
Processor structure, Processor specification, Instruction pipeline, processor and system performance
Memory System Organization and Architecture
Types of memory, Main memory organization, Memory errors, Techniques for fault tolerance, Cache organization, Cache performance, Secondary memory
Instruction Set Architecture (ISA)
Overview of ISA, Instruction formats, Addressing, Instruction types, RISC V assembly language, RISC V machine language
Multiprocessing and Parallelism
On-chip parallelism, Coprocessors, Shared-memory multiprocessor, Message-passing multicomputer</td></tr>
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Teaching /Learning Methods:

1. Direct instruction based teaching for the lectures using visual aid via slides
2. Self-learning method for in-depth knowledge of specialized topics
3. Inquire based teaching for the practical/tutorial sessions

Assessment Strategy:

Continuous Assessment			Final Assessment		
30%			100%		
Details: quizzes %, mid-term %, Assignments %			Theory (%)	Practical (%)	Other (%)(specify)
0%	100%	0%	100%	0%	0%

References/Reading Materials:

- *Computer Organization and Design – RISC-V Edition*: *The Hardware/Software Interface*, Patterson, D., and Hennesey, J., Morgan Kaufmann, Second Edition, 2020
- *Structured Computer Organization*, Tanenbaum, A., and Austin, T., Pearson Education Inc., Sixth Edition, 2013