A processor design toolkit for an open-source FPGA toolchain

105

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1 Introductionn

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL) like VHDL (Very High Speed Integrated Circuit) Hardware Description Language Verilog Verilog HDL System-Verilog An extension to Verilog to bring Verilog up to VHDL and introduce Object Oriented Programming concepts , similar to that used for an application-specific integrated circuit (ASIC). (Circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare.) They can be used to explore real hardware implementations of processor desighns from simple accumulator machines,

1.1 Background to the problem.

Their use outside industry has previously been limited due to the high cost and complexity of their associated development software. However this is changing, with an open-source toolchain for popular FPGA devises becoming available in the last year (the equivalent of Lineux in the OS world).

1.2 Problem Statement

1.3 Aim and Objectives

1.3.1 Aim or general objective

This project will build on this toolchain to develop the additional software necessary to allow students to design and explore simple processor designs on a custom FPGA development board.

1.3.2 Project Scope

The current toolchain requires the use of the Verilog hardware description language. Verilog is very powerful but also very general. This project will develop a higher level language (possibly a graphical language) focused on the development of simple processor designs from a small number of standard components (such as RAM, multiplexers and registers).

1.3.3 Research Significance

2 Methodology

3 References