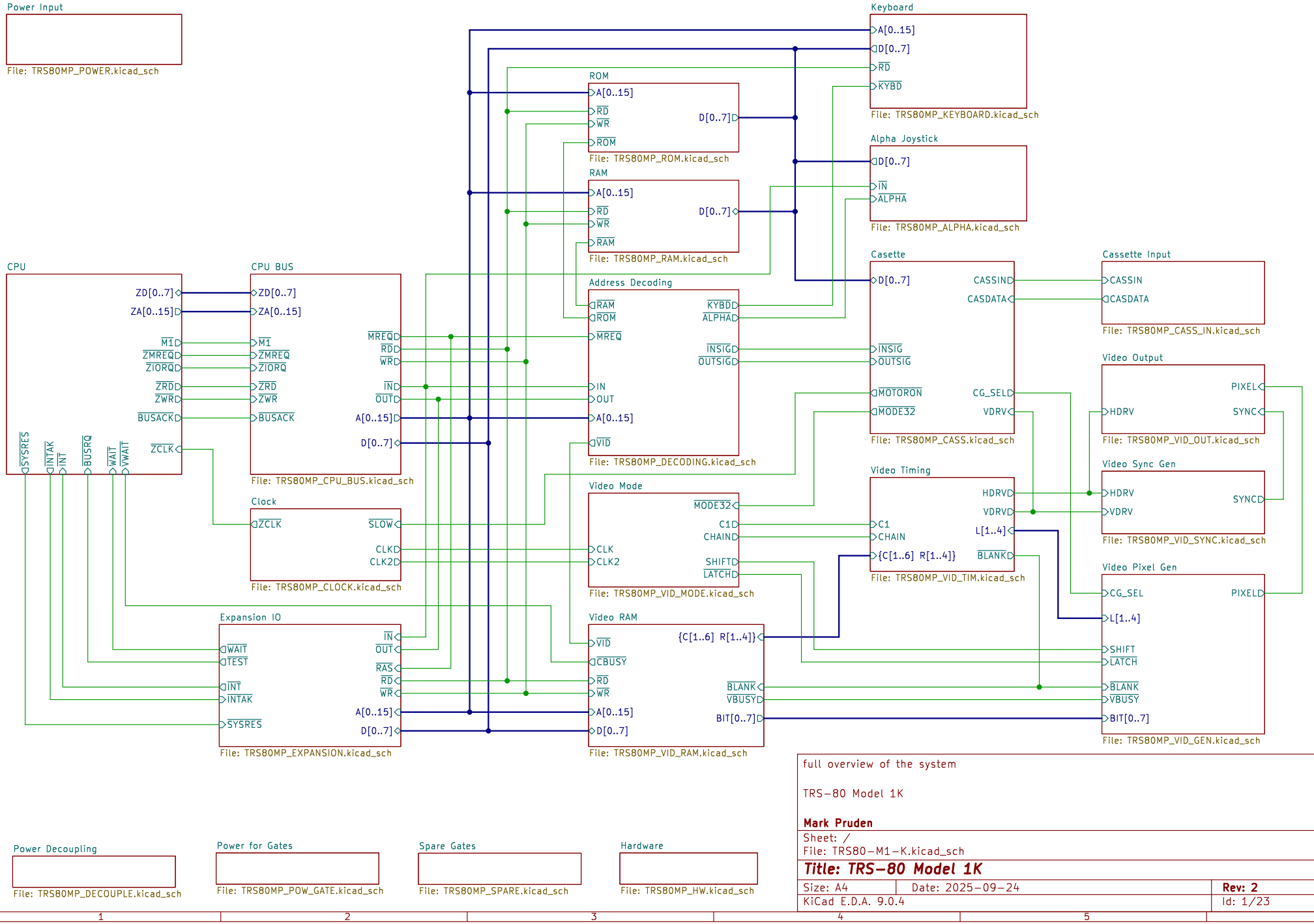
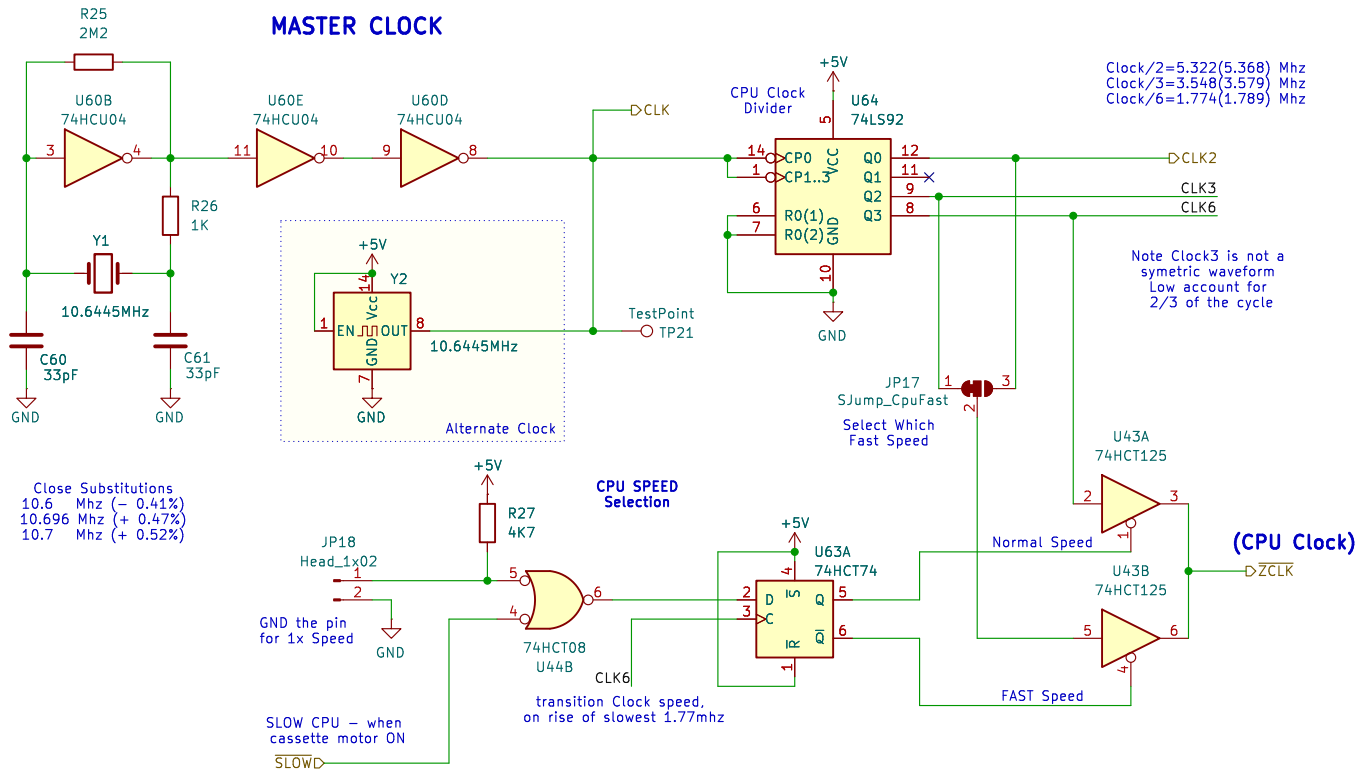

Power Input
File: TRS80MP_POWER.kicad_sch
Keyboard
A[0..15]
D[0..7]
RD
KYBD
File: TRS80MP_KEYBOARD.kicad_sch
ROM
A[0..15]
RD
WR
ROM
D[0..7]
File: TRS80MP_ROM.kicad_sch
Alpha Joystick
D[0..7]
IN
ALPHA
File: TRS80MP_ALPHA.kicad_sch
RAM
A[0..15]
RD
WR
RAM
D[0..7]
File: TRS80MP_RAM.kicad_sch
CPU
ZD[0..7]
ZA[0..15]
M1
ZMREQ
ZIORQ
ZRD
ZWR
BUSACK
ZCLK
SYSRES
INTAK
INT
BUSRQ
WAIT
VWAIT
CPU BUS
ZD[0..7]
ZA[0..15]
M1
ZMREQ
ZIORQ
ZRD
ZWR
BUSACK
MREQ
RD
WR
IN
OUT
A[0..15]
D[0..7]
File: TRS80MP_CPU_BUS.kicad_sch
Address Decoding
RAM
ROM
MREQ
IN
OUT
A[0..15]
VID
KYBD
ALPHA
INSIG
OUTSIG
File: TRS80MP_DECODING.kicad_sch
Casette
D[0..7]
CASSIN
CASDATA
INSIG
OUTSIG
MOTORON
MODE32
CG_SELD
VDRV
File: TRS80MP_CASS.kicad_sch
Cassette Input
CASSIN
CASDATA
File: TRS80MP_CASS_IN.kicad_sch
Video Output
PIXEL
HDRV
SYNC
File: TRS80MP_VID_OUT.kicad_sch
Clock
ZCLK
SLOW
CLKD
CLK2
File: TRS80MP_CLOCK.kicad_sch
Video Mode
MODE32
C1D
CHAIND
CLK
CLK2
SHIFTD
LATCHD
File: TRS80MP_VID_MODE.kicad_sch
Video Timing
HDRVD
VDRVD
L[1..4]
BLANKD
C1
CHAIN
{C[1..6] R[1..4]}
File: TRS80MP_VID_TIM.kicad_sch
Video Sync Gen
HDRV
VDRV
SYNCD
File: TRS80MP_VID_SYNC.kicad_sch
Video Pixel Gen
CG_SEL
L[1..4]
SHIFT
LATCH
BLANK
VBUSY
BIT[0..7]
PIXELD
File: TRS80MP_VID_GEN.kicad_sch
Expansion IO
WAIT
TEST
INT
INTAK
SYSRES
IN
OUT
RAS
RD
WR
A[0..15]
D[0..7]
File: TRS80MP_EXPANSION.kicad_sch
Video RAM
VID
CBUSY
RD
WR
A[0..15]
D[0..7]
{C[1..6] R[1..4]}
BLANK
VBUSY
BIT[0..7]
File: TRS80MP_VID_RAM.kicad_sch
full overview of the system
TRS-80 Model 1K
Mark Pruden
Sheet: /
File: TRS80-M1-K.kicad_sch
Title: TRS-80 Model 1K
Size: A4
Date: 2025-09-24
Rev: 2
KiCad E.D.A. 9.0.4
Id: 1/23
Power Decoupling
File: TRS80MP_DECOUPLE.kicad_sch
Power for Gates
File: TRS80MP_POW_GATE.kicad_sch
Spare Gates
File: TRS80MP_SPARE.kicad_sch
Hardware
File: TRS80MP_HW.kicad_sch



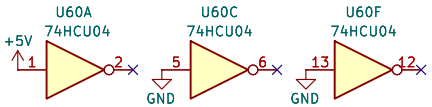
Idea 85Mhz crystal Divide by 8 = 10.6250Mhz
variance = 0.18% use a SN74F161A to divide

ALTERNATE CLOCK – DIP–14 CAN Oscillator

(U50) – 74HCU04 can be replaced with a DIP 14 CAN Oscillator. Noting:
* Pin 1 = Output Enable (High)
* Pin 7 = GND
* Pin 8 = Clock Outuput
* Pin 16 = VCC
(Then discrete components Y1, R56, R57, C60, C61 can be excluded.)

Consider Programmed 10.645 Mhz oscillator
https://www.digikey.com.au/en/products/detail/ecs-inc/ECS-P145-AN/502317

DONT RE–USE. This forms the main Oscillator



Main clock generation for CPU and video

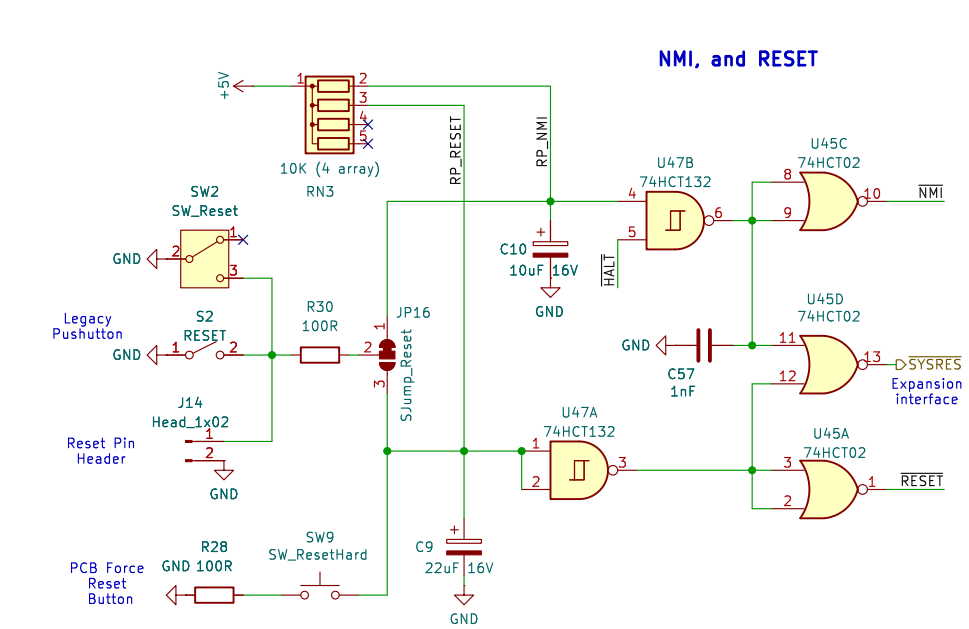
CLOCK

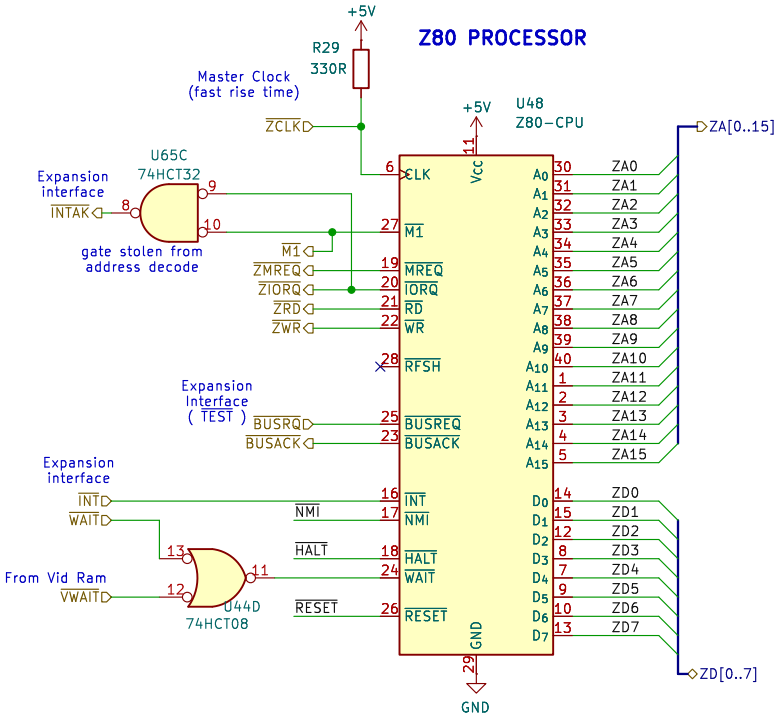
Mark Pruden

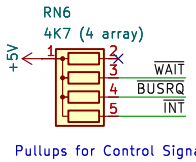
Sheet: /Clock/
File: TRS80MP_CLOCK.kicad_sch

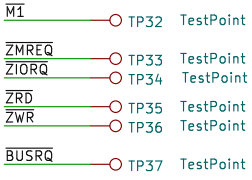
Title: TRS–80 Model 1K

Size: A4	Date: 2025–09–24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 2/23









Z80 CPU and specific support circuitry

Z80 CPU

Mark Pruden

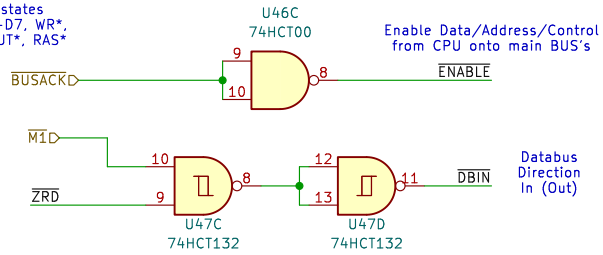
Sheet: /CPU/
File: TRS80MP_CPU.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 3/23

BUS CONTROL LOGIC

A logic 0 on BUSACK
input tri-states
A0-A15, D0-D7, WR*,
RD*, IN*, OUT*, RAS*

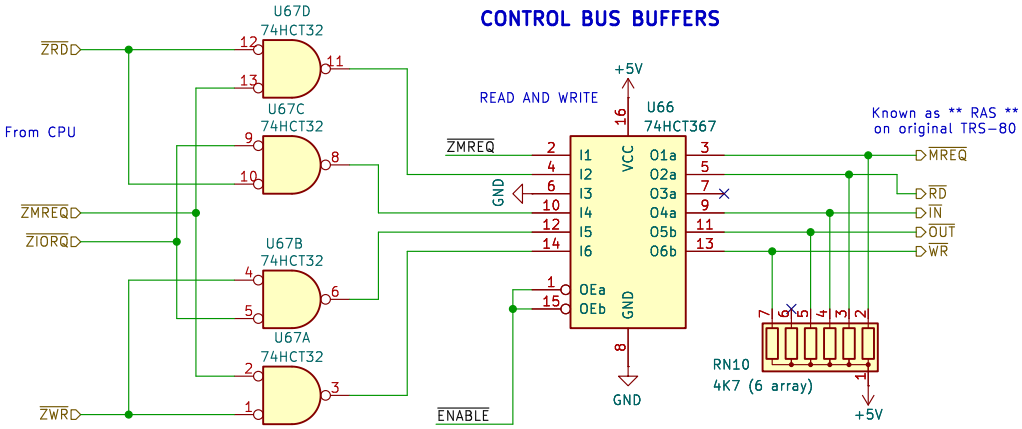


Input BUSACK was originally sourced from TEST <Credit Marcel Erz>
https://github.com/RetroStack/TRS-80-Model-I-Arduino-Library/blob/main/docs/TESTMod.md

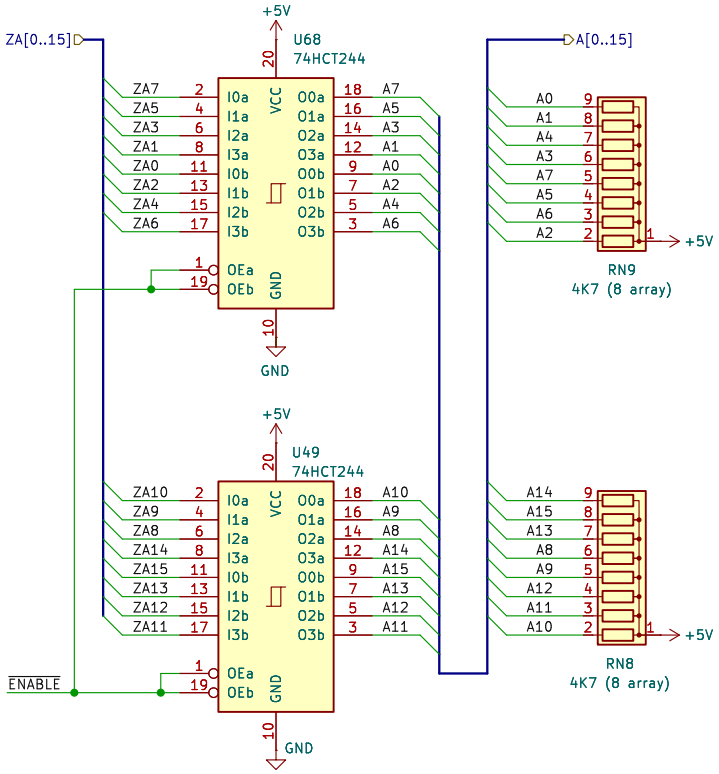
Input M1 was added to account for Interrupt handling. Without M1 interrup modes IM0 and IM2 (which require periphial to place byte on DataBus) will not be buffered back to CPU data bus

**The Model 1 hardware design issue prevents correct Interrupt handling of IM0 and IM2.
This is where the interrupting device places data on the main data bus (instruction or vector) for the CPU to process. For this reason only IM1 could realistically be used on the M1**

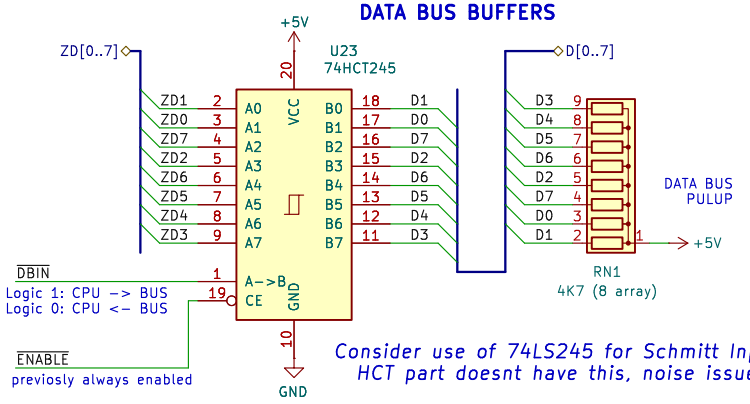
CONTROL BUS BUFFERS



ADDRESS BUS BUFFERS



DATA BUS BUFFERS



*Consider use of 74LS245 for Schmitt Inputs.
HCT part doesnt have this, noise issues.*

MREQ — TP42TestPoint
IN — TP43TestPoint
OUT — TP44TestPoint
RD — TP45TestPoint
WR — TP46TestPoint

Links Z80 to main system bus

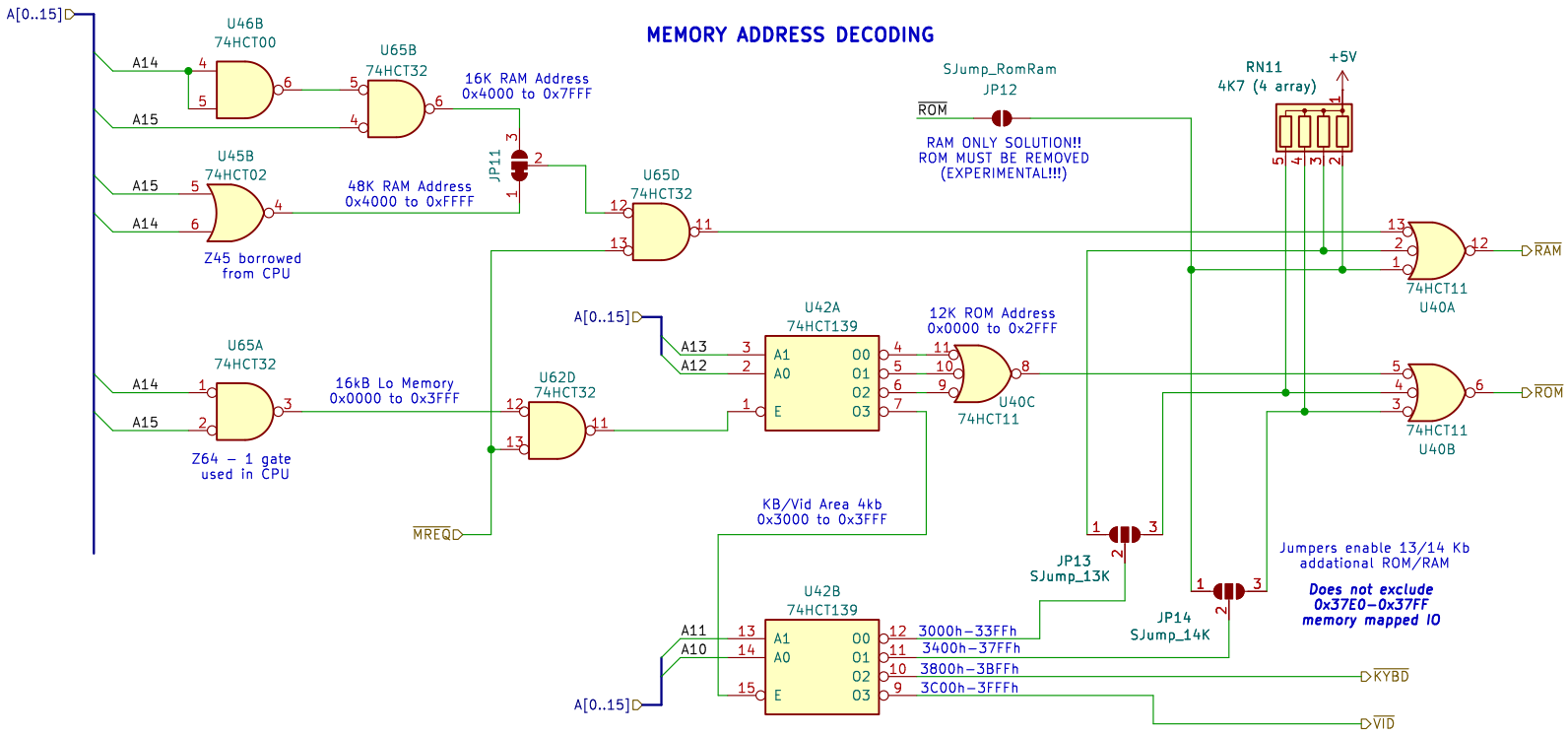
CPU BUS

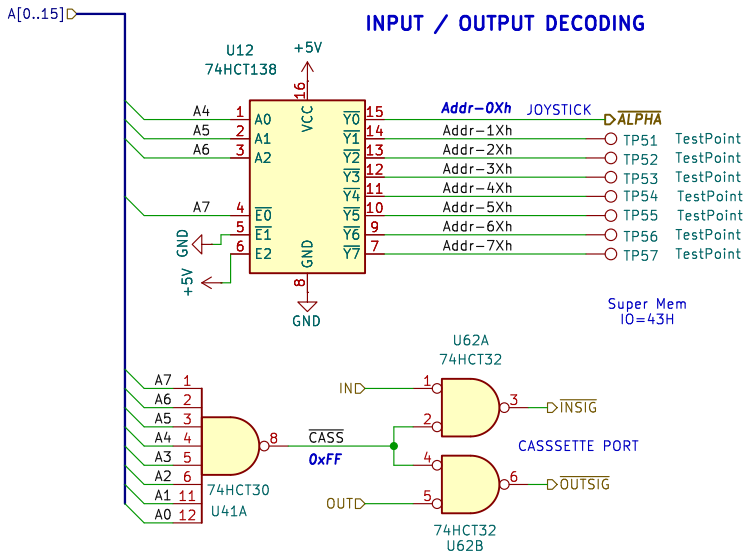
Mark Pruden

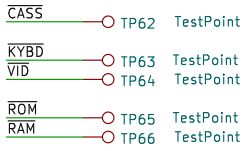
Sheet: /CPU BUS/
File: TRS80MP_CPU_BUS.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 4/23







JUMPER SETTINGS

JP12	JP13	JP14	Memory
–	–	–	12K ROM
–	12	–	12K ROM +1K RAM
–	12	23	12K ROM +1K RAM, ROM
–	12	12	12K ROM +2K RAM
–	23	–	13K ROM
–	23	12	13K ROM +1K RAM
–	23	23	14K ROM
X	–	–	12K RAM
X	23	–	13K RAM
X	23	23	14K RAM

Notes:
- Bridging JP12 requires ROM removal!
- Using 14Kb (JP14) conflicts with memory mapped IO

decoding of memory and IO addresses

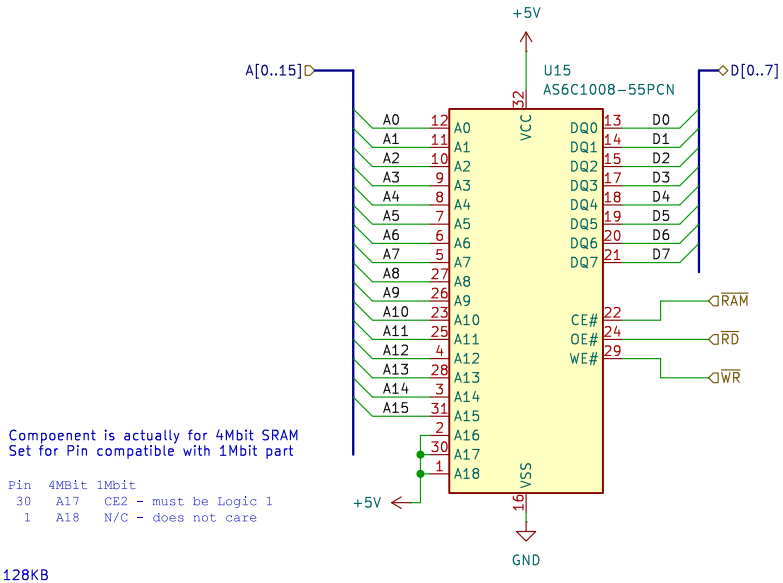
ADDRESS DECODING

Mark Pruden

Sheet: /Address Decoding/
File: TRS80MP_DECODING.kicad_sch

Title: TRS–80 Model 1K

Size: A4	Date: 2025–09–24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 5/23



Compoenent is actually for 4Mbit SRAM
Set for Pin compatible with 1Mbit part

Pin	4MBit	1Mbit
30	A17	CE2 - must be Logic 1
1	A18	N/C - does not care

128KB
Manufacturer : Alliance Memory, Inc.
Part Number : AS6C1008-55PCN
Description : SRAM - Asynchronous Memory IC 1Mbit Parallel 55 ns 32-SOP

or

512KB
Manufacturer : Alliance Memory, Inc.
Part Number : AS6C4008-55PCN
Description : SRAM - Asynchronous Memory IC 4Mbit Parallel 55 ns 32-PDIP

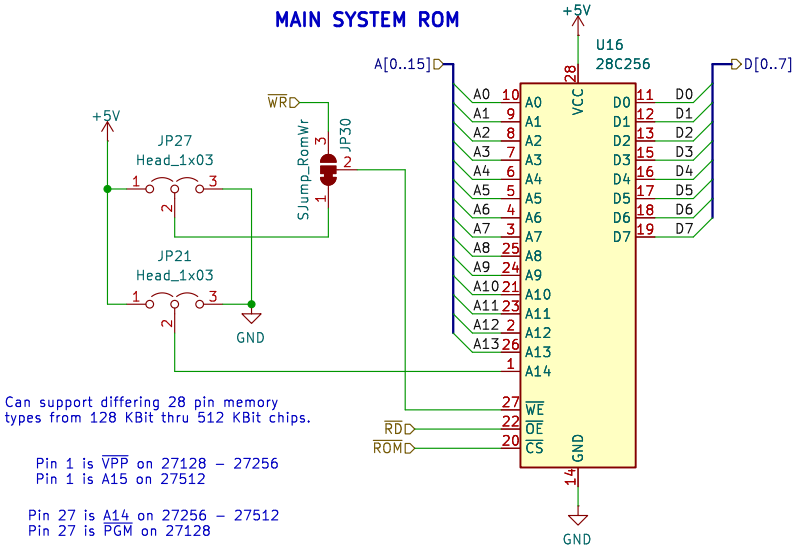
SYSTEM RAM

Mark Pruden

Sheet: /RAM/
File: TRS80MP_RAM.kicad_sch

Title: TRS-80 Model 1K

Size: A4 | Date: 2025-09-24 | **Rev: 2**
KiCad E.D.A. 9.0.4 | Id: 6/23



JUMPER SETTINGS

PROM TYPE	JP21	JP27
28256	A14	12
27512	A15	A14
27256	12	A14
27128	12	12

JP30 - EEPROM Write Mode
12 Normal Read Only
23 Enable Write (28256)

Notes:
- JP21 controls Pin 1, and JP27 Pin 27
- Bridging 1&2 Provides Logic Level 1
- Bridging 2&3 Provides Logic Level 0

Recommend EEPROM:

Manufacturer : Microchip Technology
Part Number : AT28C256-15PU
Description : EEPROM Memory IC 256Kbit Parallel 150 ns 28-PDIP

SYSTEM ROM

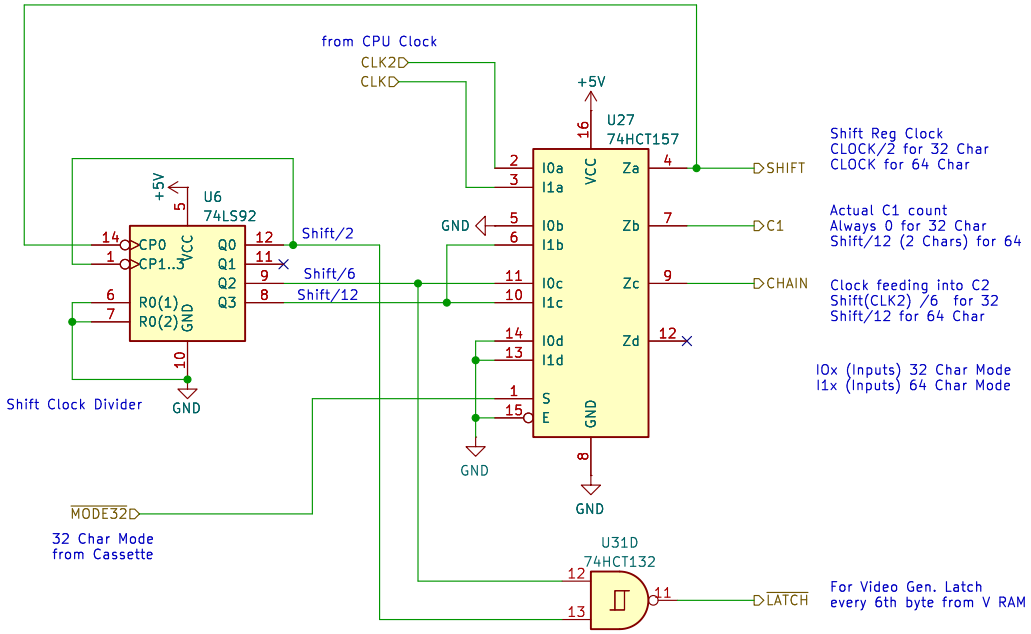
Mark Pruden

Sheet: /ROM/
File: TRS80MP_ROM.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 7/23

32 CHAR MODE CONTROL



SHIFT — TP105 TestPoint
LATCH — TP106 TestPoint

handles 32 character / 64 character mode timing

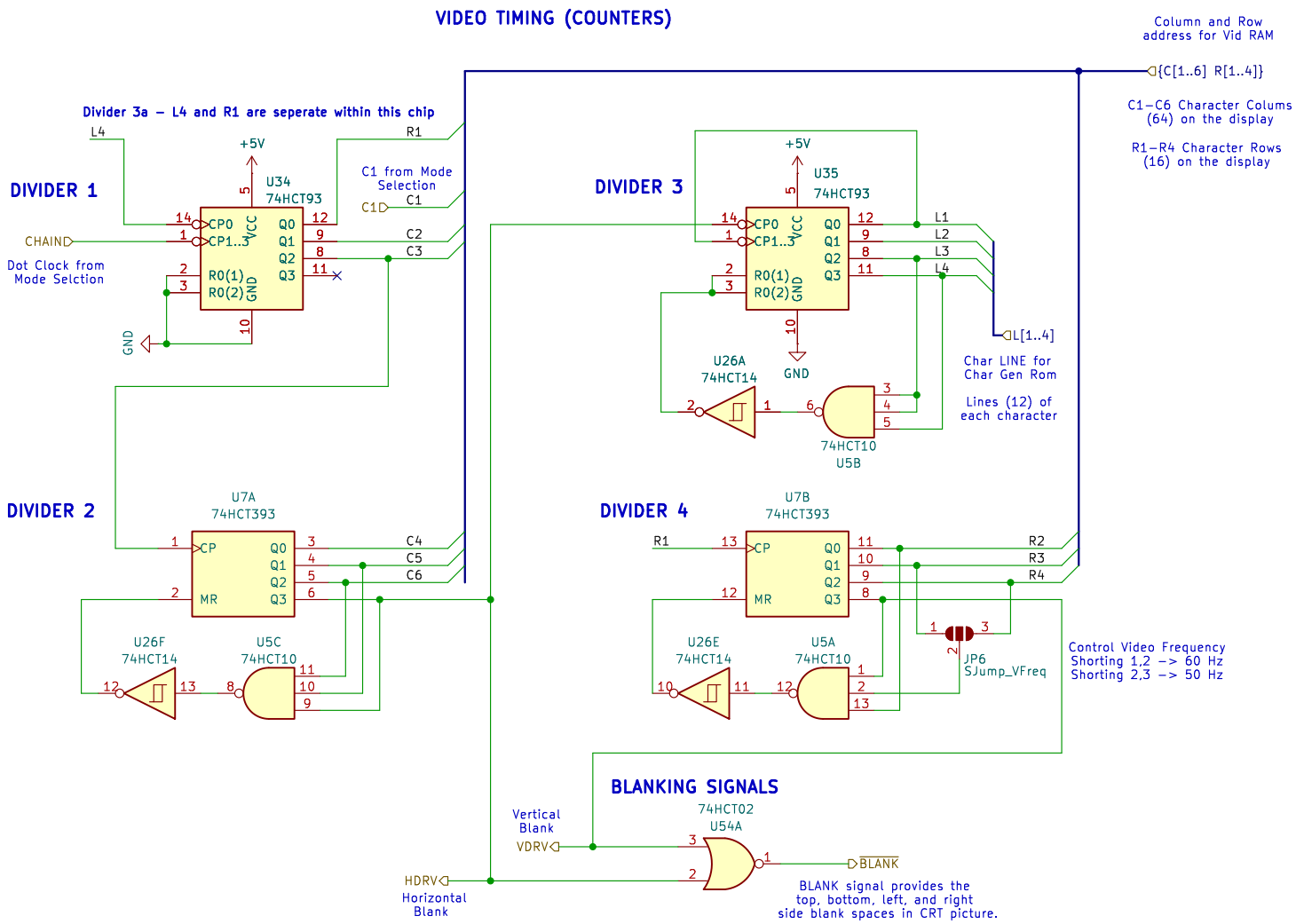
VIDEO MODEL CONTROL

Mark Pruden

Sheet: /Video Mode/
File: TRS80MP_VID_MODE.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 10/23



divides and count system clock to produce video structure

VIDEO TIMING

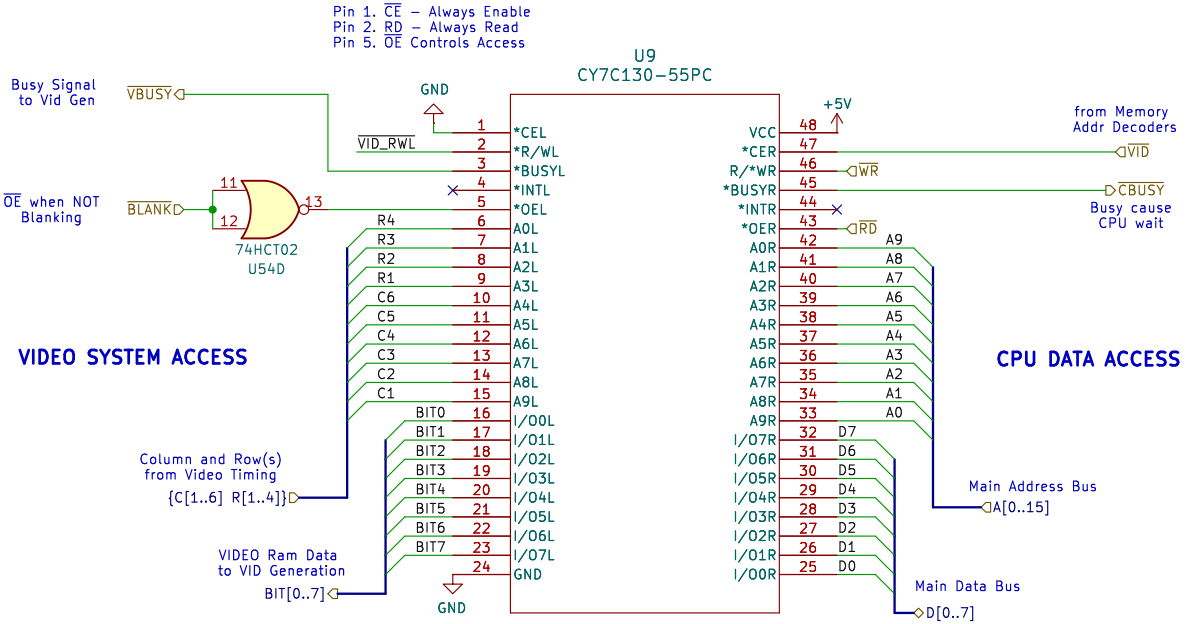
Mark Pruden

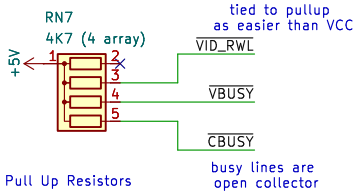
Sheet: /Video Timing/
File: TRS80MP_VID_TIM.kicad_sch

Title: TRS–80 Model 1K

Size: A4	Date: 2025–09–24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 11/23

VIDEO RAM





dual port video ram used by CPU and video subsystem

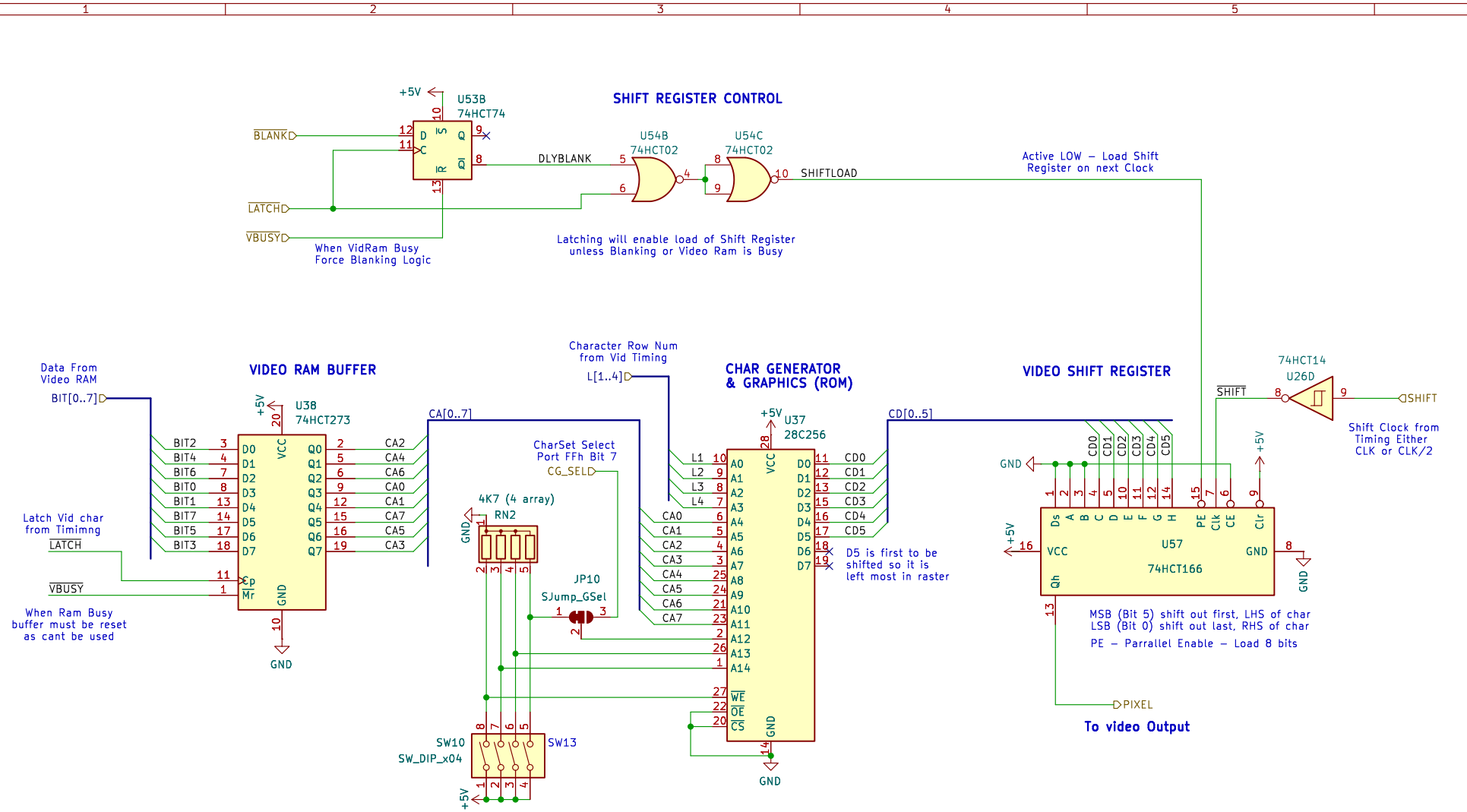
VIDEO RAM

Mark Pruden

Sheet: /Video RAM/
File: TRS80MP_VID_RAM.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 12/23



CHARACTER SET SETTINGS

PROM TYPE	SW10	SW11	SW12	SW13
28256	ON	A14	A13	A12
27512	A14	A15	A13	A12
27256	A14	ON	A13	A12
27128	ON	ON	A13	A12

JP10 - A12 Address Selection
12 Normal selectable from Dip SW13
23 Software Controlled Port FFh Bit 7

Notes:
- Silkscreen identifies SW10 – SW13.
- Dip Switch ON = Logic 1, OFF = Logic 0
- Port FFh Bit 7 conforms to Japan Model 1

Can support differing 28 pin memory types from 128 KBit thru 512 KBit EPROM chips.

Pin 1 is $\overline{VPP}$ on 27128 – 27256
Pin 1 is A15 on 27512

Pin 27 is A14 on 27256 – 27512
Pin 27 is $\overline{PGM}$ on 27128

generates the Pixel data displayed on screen

VIDEO PIXEL GENERATION

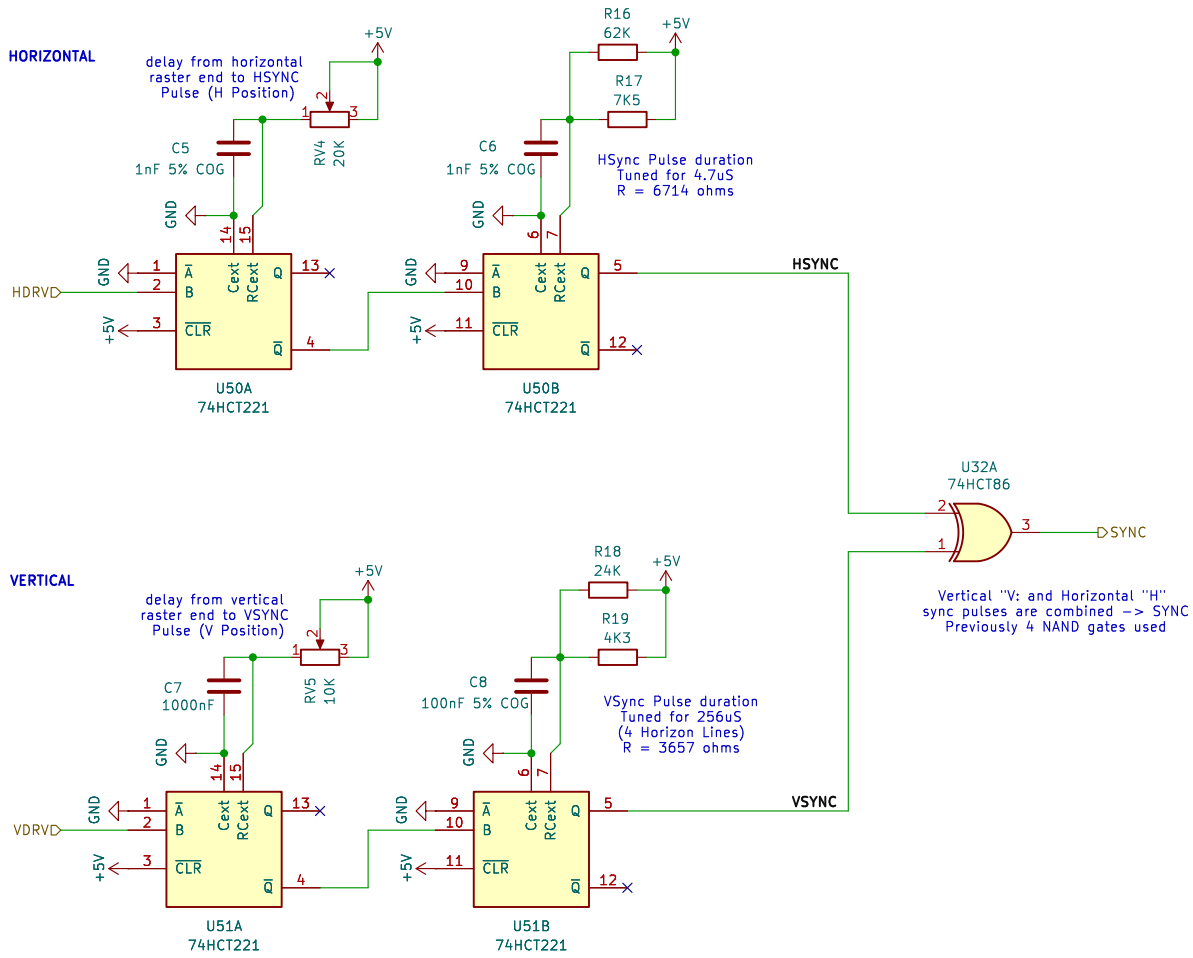
Mark Pruden

Sheet: /Video Pixel Gen/
File: TRS80MP_VID_GEN.kicad_sch

Title: TRS–80 Model 1K

Size: A4	Date: 2025–09–24	Rev: 2
KiCad E.D.A. 9.0.4		Id: 13/23

SYNC PULSE GENAERATION



R17 & R19 are primary timing resistors, and have been chosen to ensure that by themselves the pulse duraton is slightly long. Pulse duration can be adjusted via trimming resistor.

R16 & R18 are trimming resistors and should be matched based on the the other components. The values given are calaulated and are based on 100% accuracy of other components. e.g Capacitor

Exact values can only be determined via measurement. I suggest initially leaving them un-populated, then measure pulse duration (using oscilliscope) trying different values (for R16 R18) until the pulse duration is correct.

Increasing its value (or omitting it entirely) will lengthen the delay, decreasing its value will shorten the delay. Once correct values have been determined they can be soldered.

This process can be done without other major components (e.g. CPU/RAM/ROM) being inserted.

H Sync Pulse Duration should be 4.7 uS
V Sync Pulse Duration should be 256 uS

ALTERANATELY

The indicated values can be used, however C106 & C108 (specifically) should be chosen for there accuracy and resiliance to temperate differences. i.e. COG

VSYNC — TP141 TestPoint
HSYNC — TP142 TestPoint

generates the video sync signals

VIDEO SYNC GENERATION

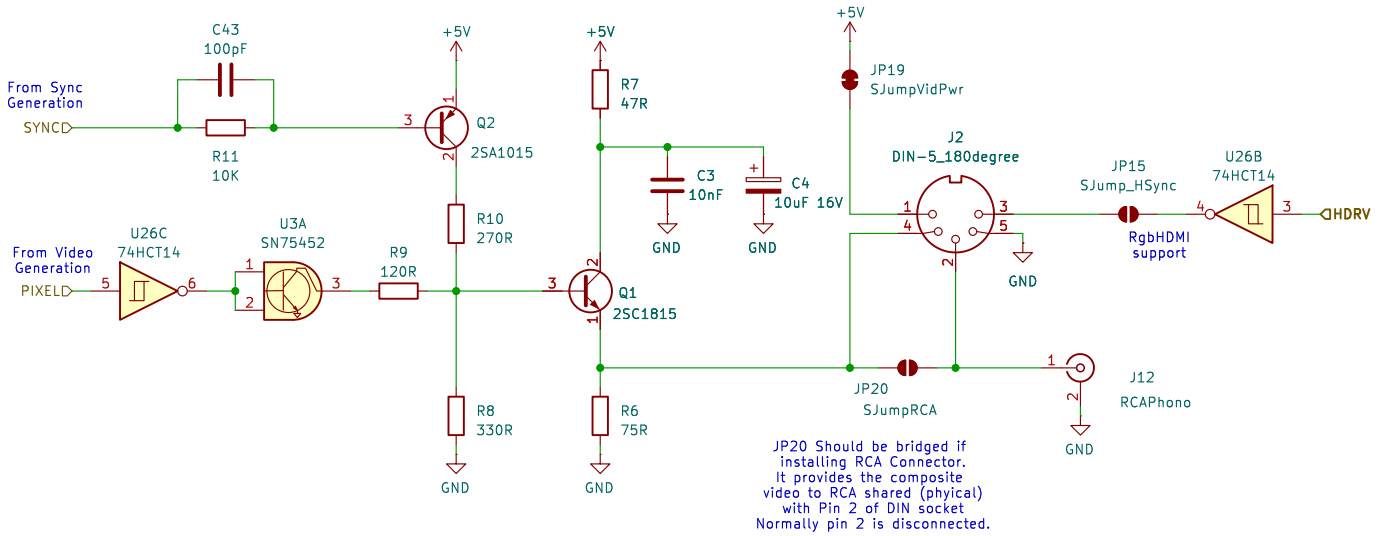
Mark Pruden

Sheet: /Video Sync Gen/
File: TRS80MP_VID_SYNC.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 14/23

VIDEO OUTPUT



combines video pixel and sync signals to produce composite video

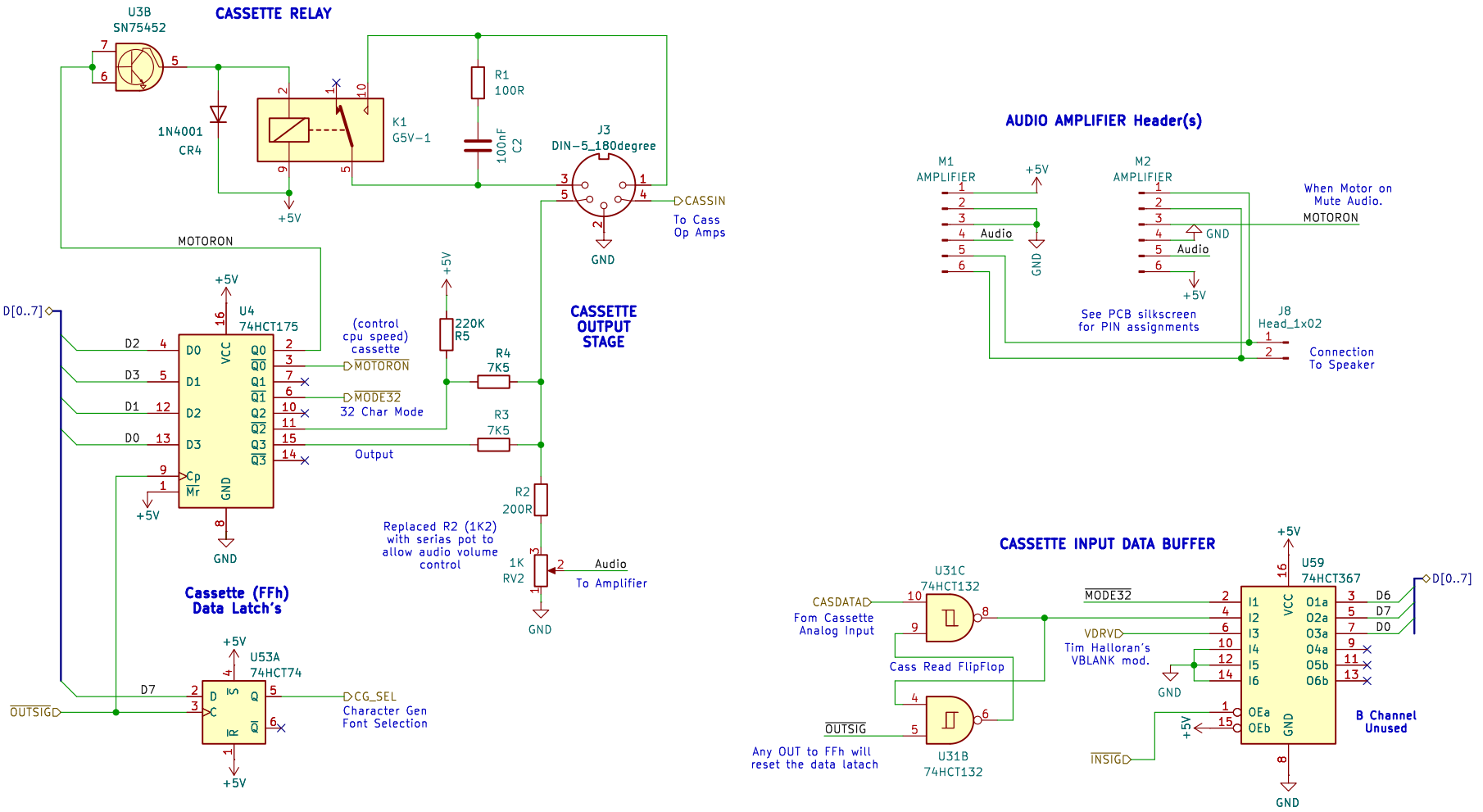
VIDEO OUTPUT

Mark Pruden

Sheet: /Video Output/
File: TRS80MP_VID_OUT.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 15/23



Tim Halloran's VBLANK mod.
https://github.com/hallorant/bigmit/tree/master/ta19demo

primary cassette (port FF) input/output, and audio amplifier

CASETTE INTERFACE

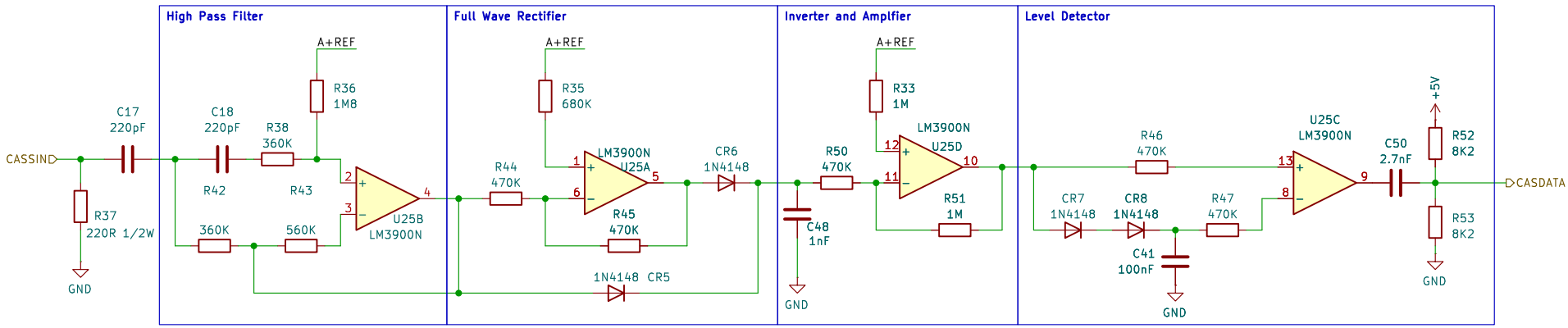
Mark Pruden

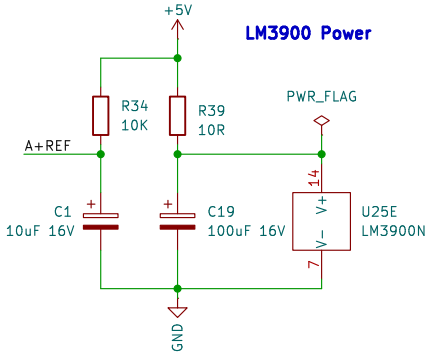
Sheet: /Casette/
File: TRS80MP_CASS.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 20/23

CASSETTE INPUT STAGE





analog cuircuitry to convert incoming cassette signal to digital

CASSETTE ANALOG INPUT

Mark Pruden

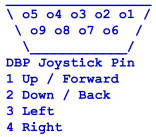
Sheet: /Cassette Input/
File: TRS80MP_CASS_IN.kicad_sch

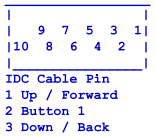
Title: TRS-80 Model 1K

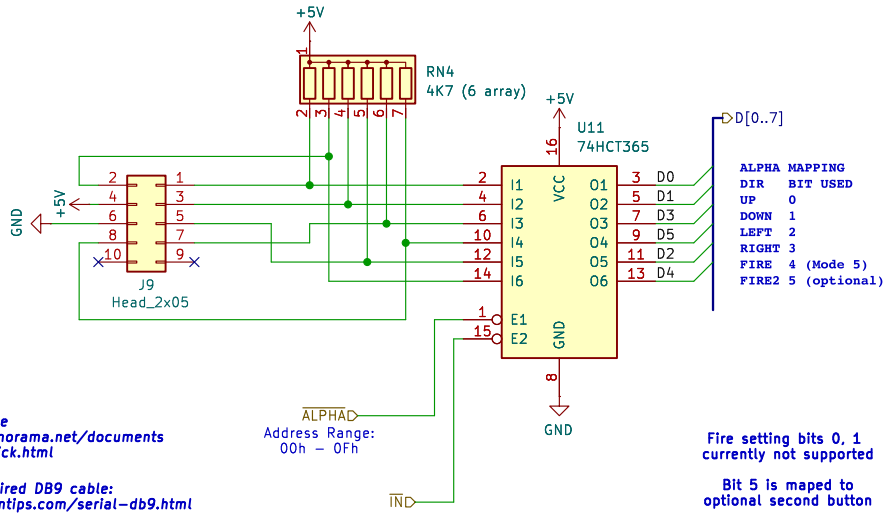
Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 21/23

ALPHA JOYSTICK PORT

(actually it is TRISSTICK)







Atari Pinout Guide
https://www.epanorama.net/documents/joystick/ataristick.html

Needs a cross wired DB9 cable:
https://www.scantips.com/serial-db9.html

Fire setting bits 0, 1 currently not supported

Bit 5 is maped to optional second button

ALPHA JOYSTICK PORT

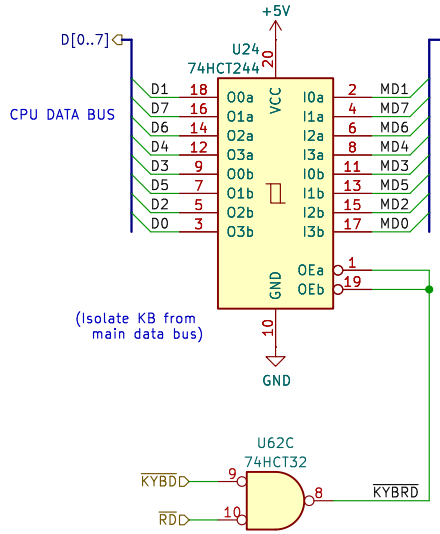
Mark Pruden

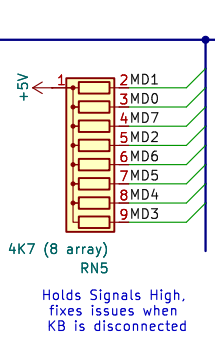
Sheet: /Alpha Joystick/
File: TRS80MP_ALPHA.kicad_sch

Title: TRS-80 Model 1K

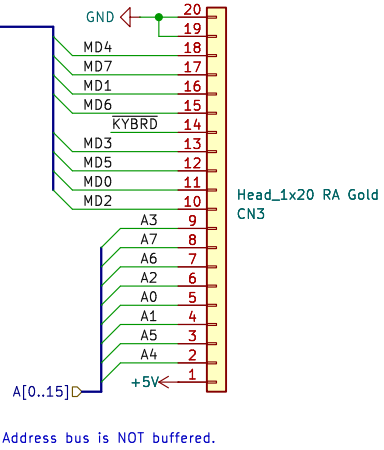
Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 24/23

KEYBOARD BUFFER





KEYBOARD CONNECTOR



keyboard input connection and buffering

KEYBOARD

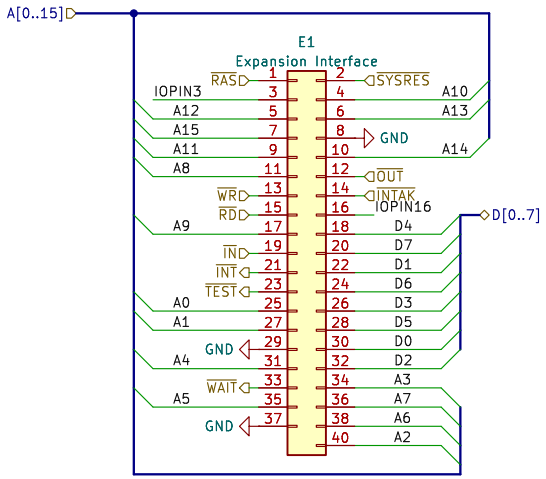
Mark Pruden

Sheet: /Keyboard/
File: TRS80MP_KEYBOARD.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 25/23

TRS-80 EXPANSION EDGE CONNECTOR



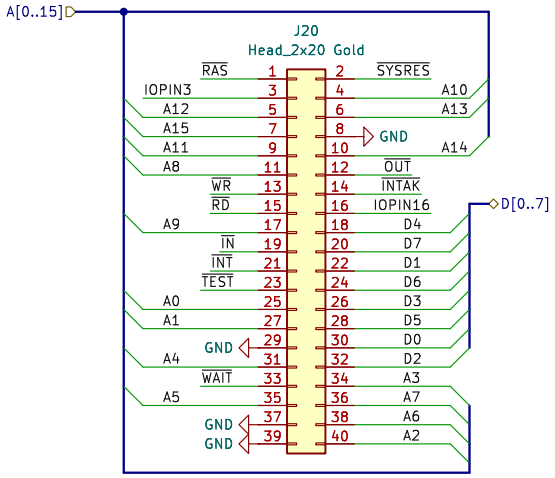
PINS 3 (RAS), 16 (MUX) for Dynamic RAM refresh ae no longer Supported

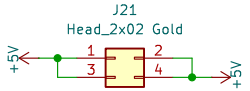
TP3 TestPoint IOPIN3

The pins are exposed and can be utilised in future via these TP's

TP16 TestPoint IOPIN16

INTERNAL EXPANSION HEADER





5 Volt Power for Internal Peripial.

main TRS-80 system expansion bus

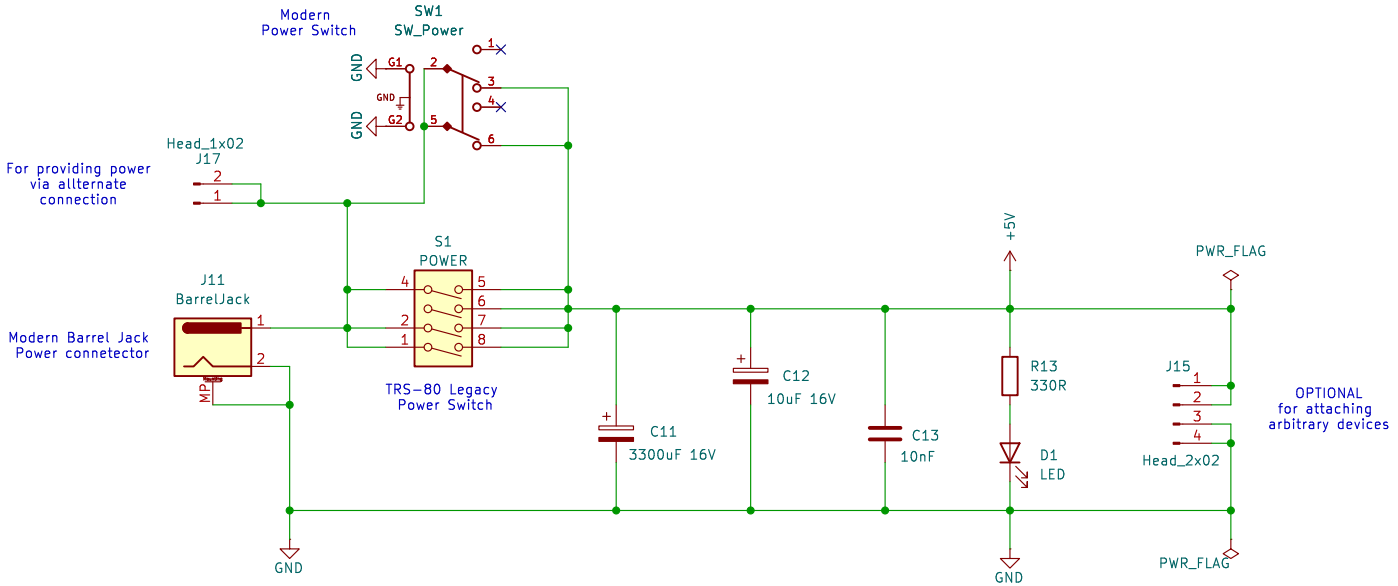
EXPANSION I/O

Mark Pruden

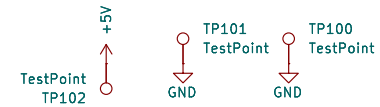
Sheet: /Expansion IO/
File: TRS80MP_EXPANSION.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 26/23



Additional through holes for capacitor C11 mounting



power input, switching, and primary input caps

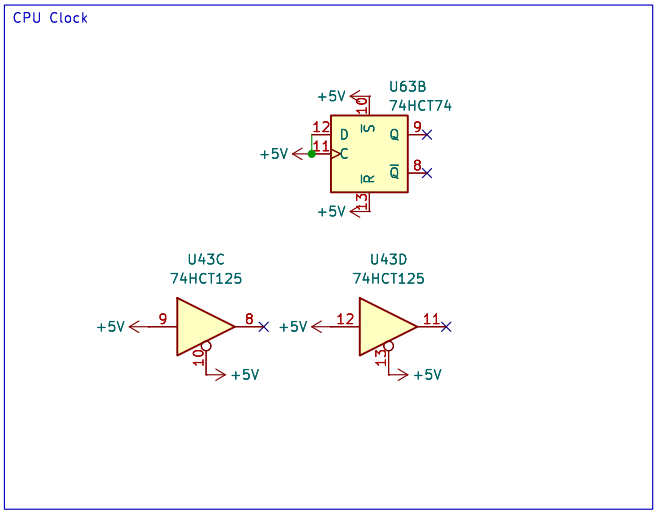
POWER INPUT

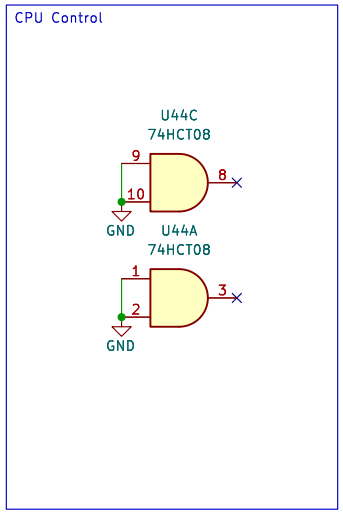
Mark Pruden

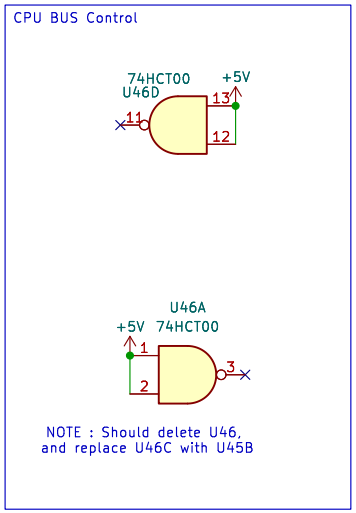
Sheet: /Power Input/
File: TRS80MP_POWER.kicad_sch

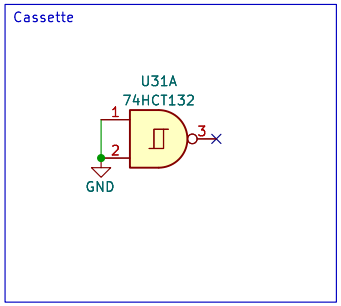
Title: TRS-80 Model 1K

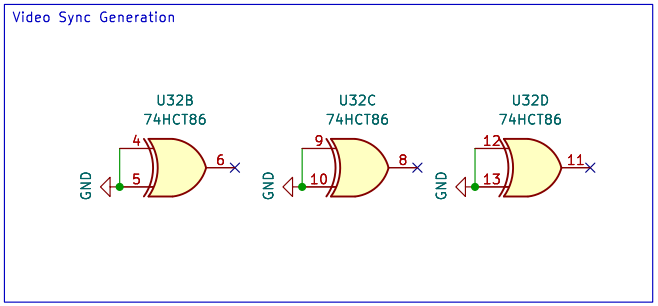
Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 27/23



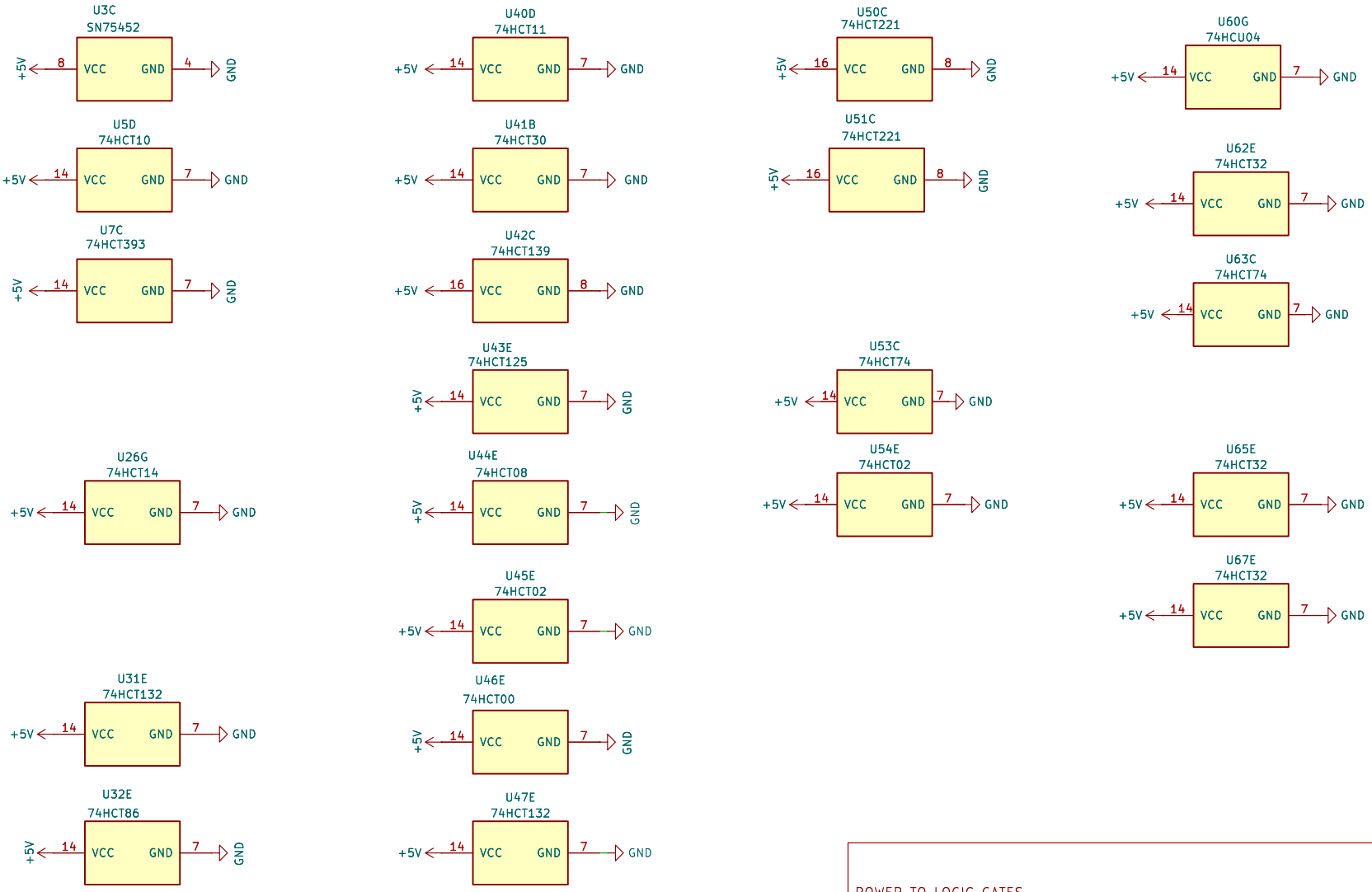








Mark Pruden		
Sheet: /Spare Gates/ File: TRS80MP_SPARE.kicad_sch		
Title: TRS-80 Model 1K		
Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 29/23



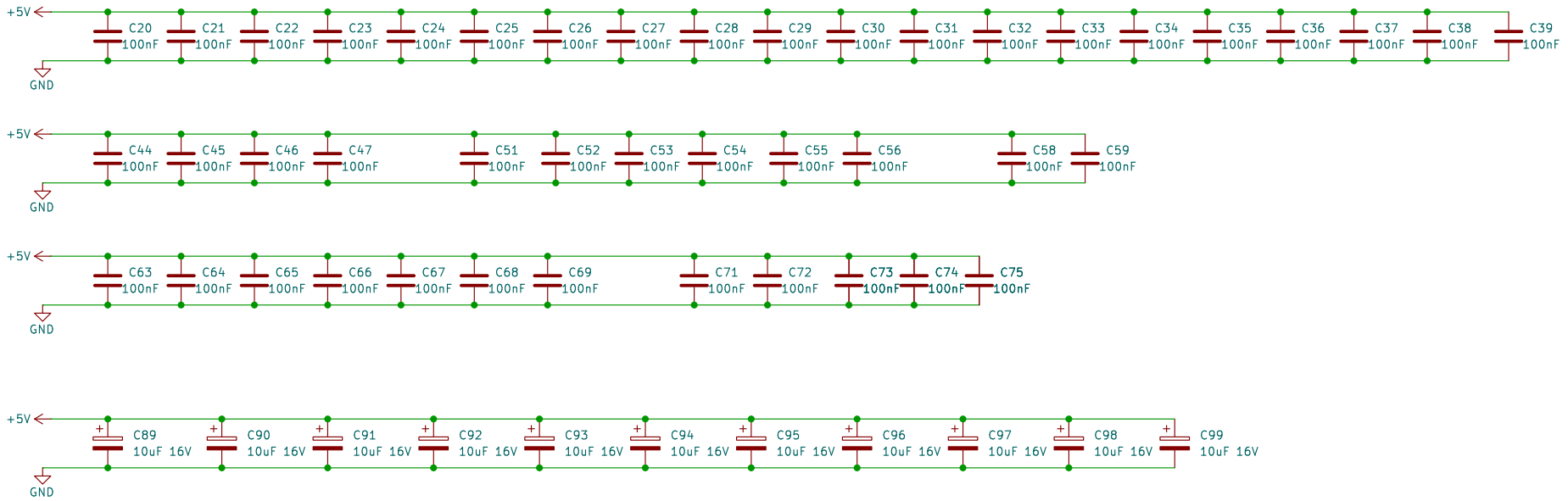
POWER TO LOGIC GATES

Mark Pruden

Sheet: /Power for Gates/
File: TRS80MP_POW_GATE.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 30/23



POWER DECOUPLING CAPACITORS

Mark Pruden

Sheet: /Power Decoupling/
File: TRS80MP_DECOUPLE.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 31/23

TRS-80 MOUNTING HOLES

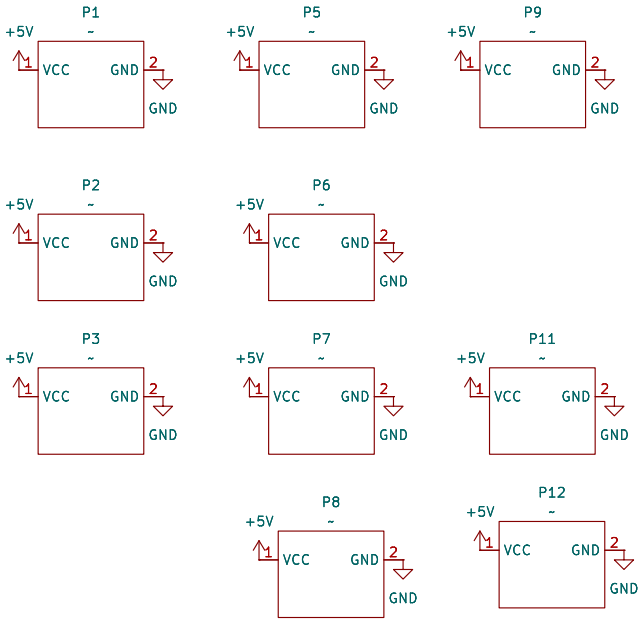
H1 MountingHole
H2 MountingHole
H3 MountingHole
H4 MountingHole
H5 MountingHole
H6 MountingHole
H7 MountingHole
H9 MountingHole
H8 MountingHole

INTERNAL EXPANSION

FREHD BOARD
H10 MountingHole
H11 MountingHole
H12 MountingHole
H13 MountingHole

designed for mounting a PCB to the Internal expansion IO

PROTOTYPE AREAS



Jumpers for BOM (only) used to bridge Config Pin Headers

MECHANICAL HARDWARE

Mark Pruden

Sheet: /Hardware/
File: TRS80MP_HW.kicad_sch

Title: TRS-80 Model 1K

Size: A4	Date: 2025-09-24	**Rev: 2**
KiCad E.D.A. 9.0.4		Id: 32/23