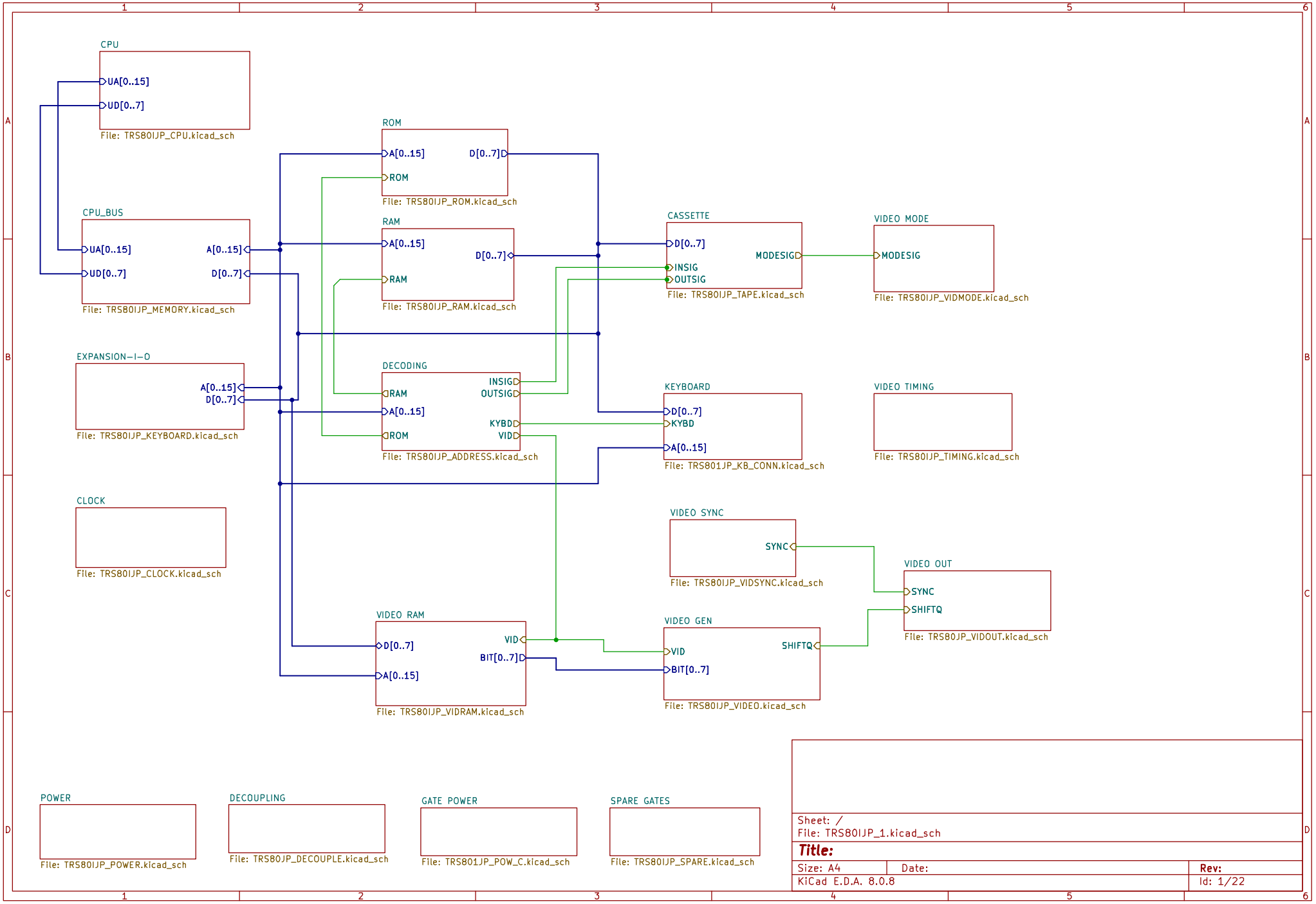
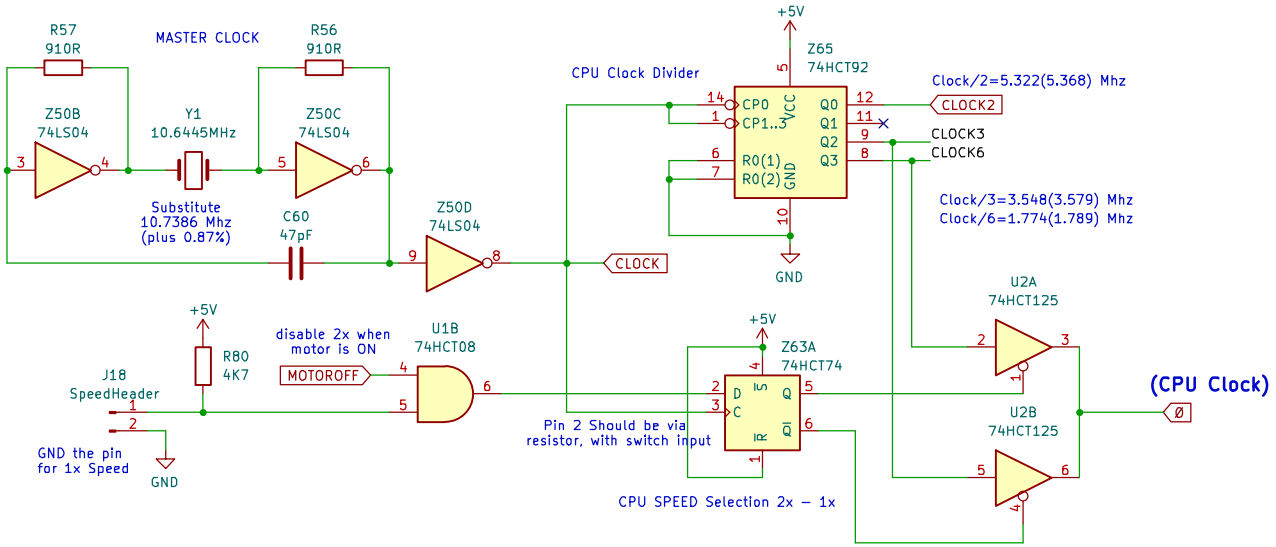
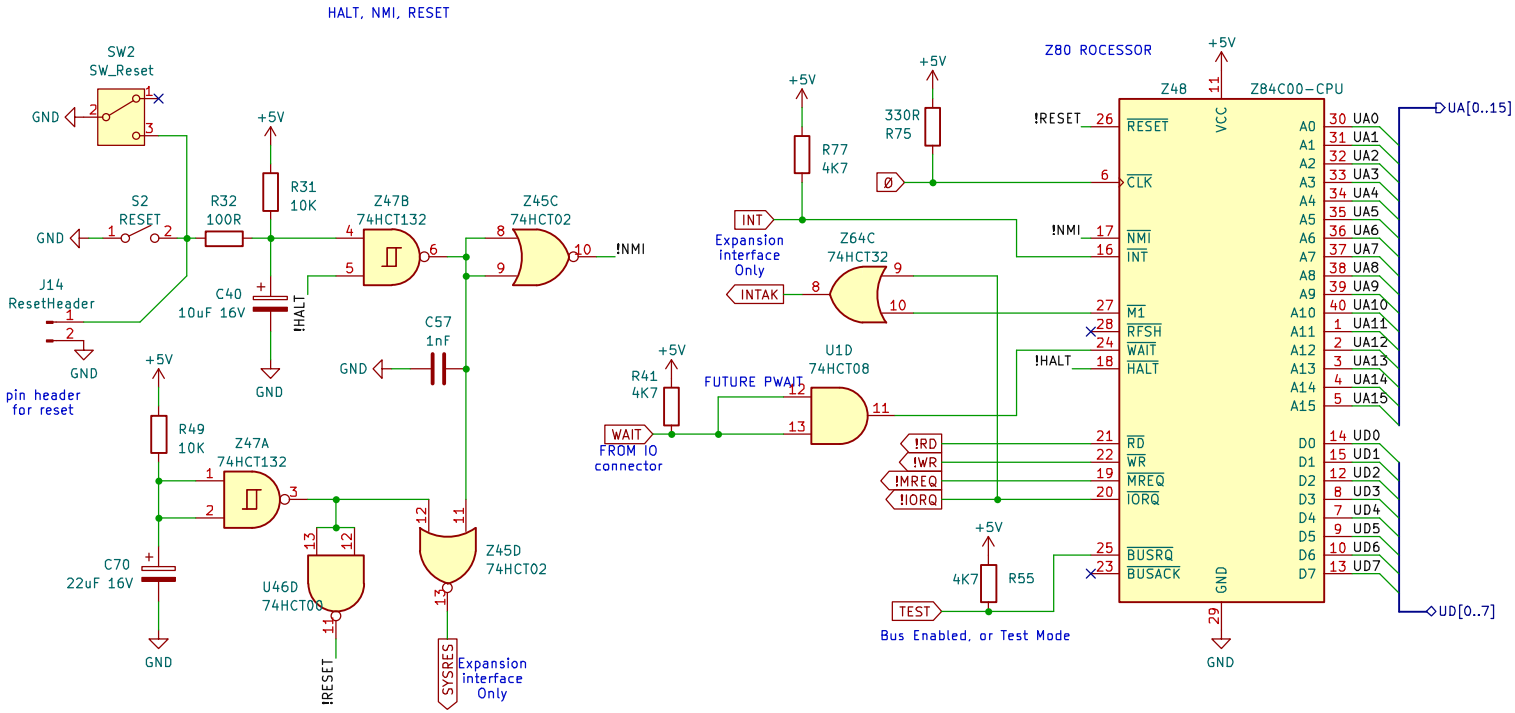
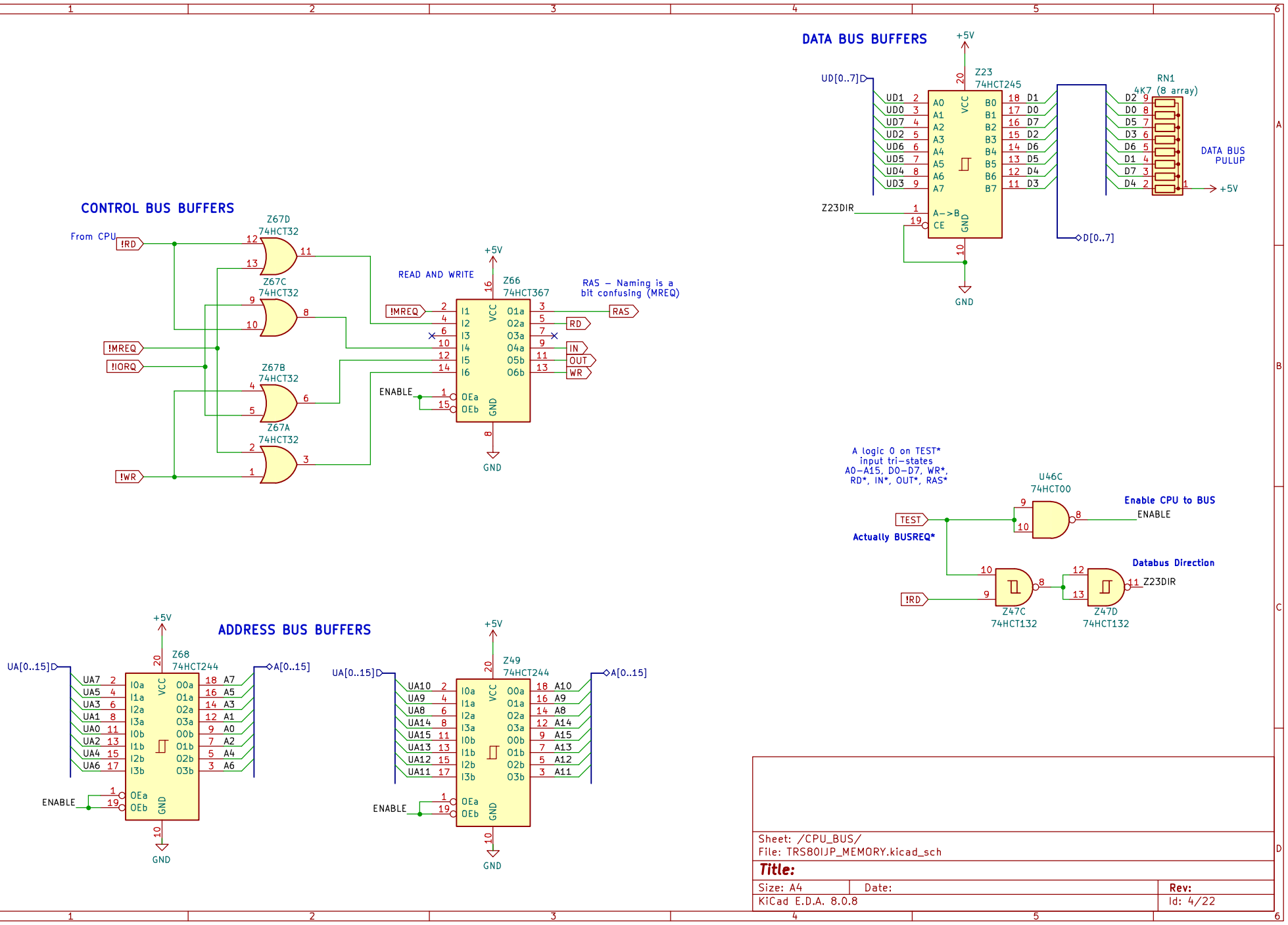

CPU
UA[0..15]
UD[0..7]
File: TRS80IJP_CPU.kicad_sch
ROM
A[0..15]
D[0..7]
ROM
File: TRS80IJP_ROM.kicad_sch
CPU_BUS
UA[0..15]
A[0..15]
UD[0..7]
D[0..7]
File: TRS80IJP_MEMORY.kicad_sch
RAM
A[0..15]
D[0..7]
RAM
File: TRS80IJP_RAM.kicad_sch
CASSETTE
D[0..7]
MODESIG
INSIG
OUTSIG
File: TRS80IJP_TAPE.kicad_sch
VIDEO MODE
MODESIG
File: TRS80IJP_VIDMODE.kicad_sch
EXPANSION—I—O
A[0..15]
D[0..7]
File: TRS80IJP_KEYBOARD.kicad_sch
DECODING
RAM
A[0..15]
ROM
INSIG
OUTSIG
KYBD
VID
File: TRS80IJP_ADDRESS.kicad_sch
KEYBOARD
D[0..7]
KYBD
A[0..15]
File: TRS801JP_KB_CONN.kicad_sch
VIDEO TIMING
File: TRS80IJP_TIMING.kicad_sch
CLOCK
File: TRS80IJP_CLOCK.kicad_sch
VIDEO SYNC
SYNC
File: TRS80IJP_VIDSYNC.kicad_sch
VIDEO OUT
SYNC
SHIFTQ
File: TRS80JP_VIDOUT.kicad_sch
VIDEO RAM
D[0..7]
A[0..15]
VID
BIT[0..7]
File: TRS80IJP_VIDRAM.kicad_sch
VIDEO GEN
VID
BIT[0..7]
SHIFTQ
File: TRS80IJP_VIDEO.kicad_sch
POWER
File: TRS80IJP_POWER.kicad_sch
DECOUPLING
File: TRS80JP_DECOUPLE.kicad_sch
GATE POWER
File: TRS801JP_POW_C.kicad_sch
SPARE GATES
File: TRS80IJP_SPARE.kicad_sch
Sheet: /
File: TRS80IJP_1.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.8
Id: 1/22



Sheet: /CLOCK/		
File: TRS80IJP_CLOCK.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 2/22



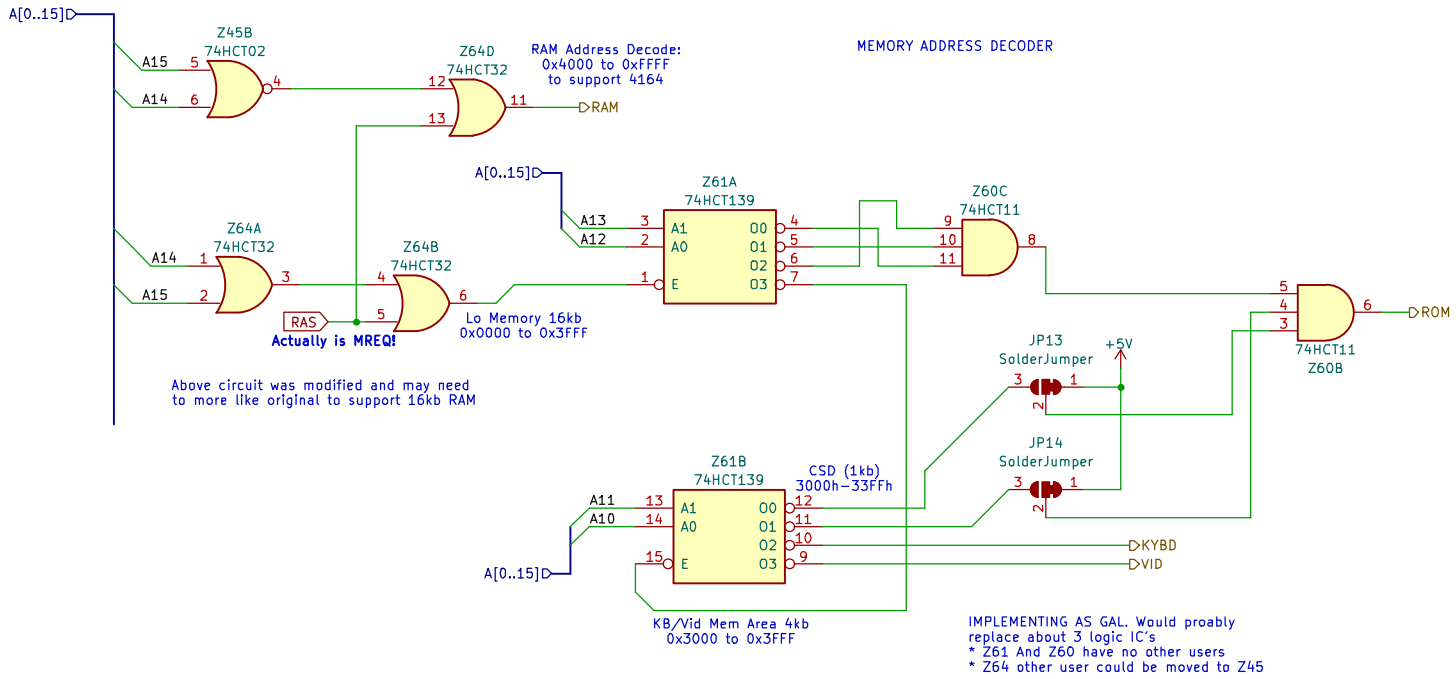
Sheet: /CPU/		
File: TRS80IJP_CPU.kicad_sch		
Title: CPU and CPU Support		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 3/22

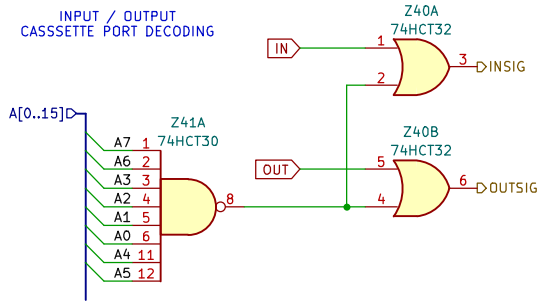


Sheet: /CPU_BUS/
File: TRS80IJP_MEMORY.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 4/22

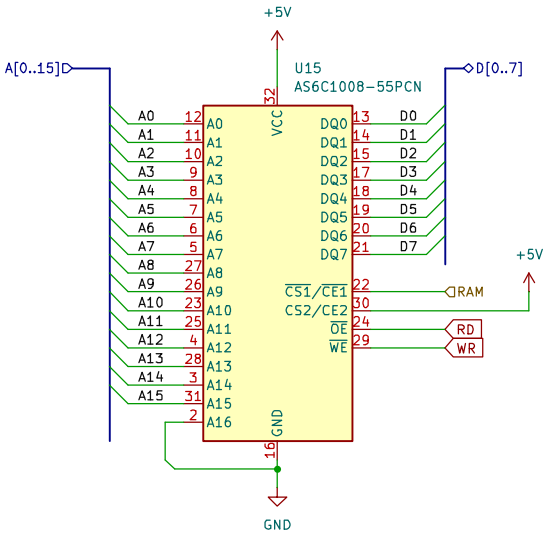




Sheet: /DECODING/
File: TRS80IJP_ADDRESS.kicad_sch

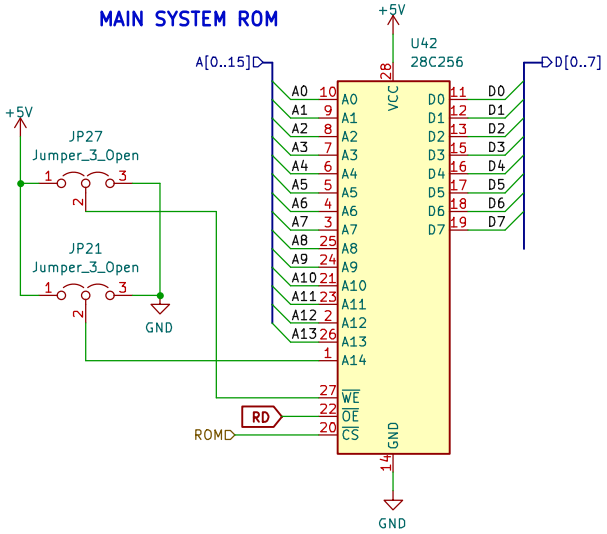
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 5/22



Manufacturer : Alliance Memory, Inc.
Part Number : AS6C1008-55PCN
Description : SRAM - Asynchronous Memory IC 1Mbit Parallel 55 ns 32-SOP

Sheet: /RAM/		
File: TRS80IJP_RAM.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 6/22



Manufacturer : Microchip Technology
Part Number : AT28C256-15PU
Description : EEPROM Memory IC 256Kbit Parallel 150 ns 28-PDIP

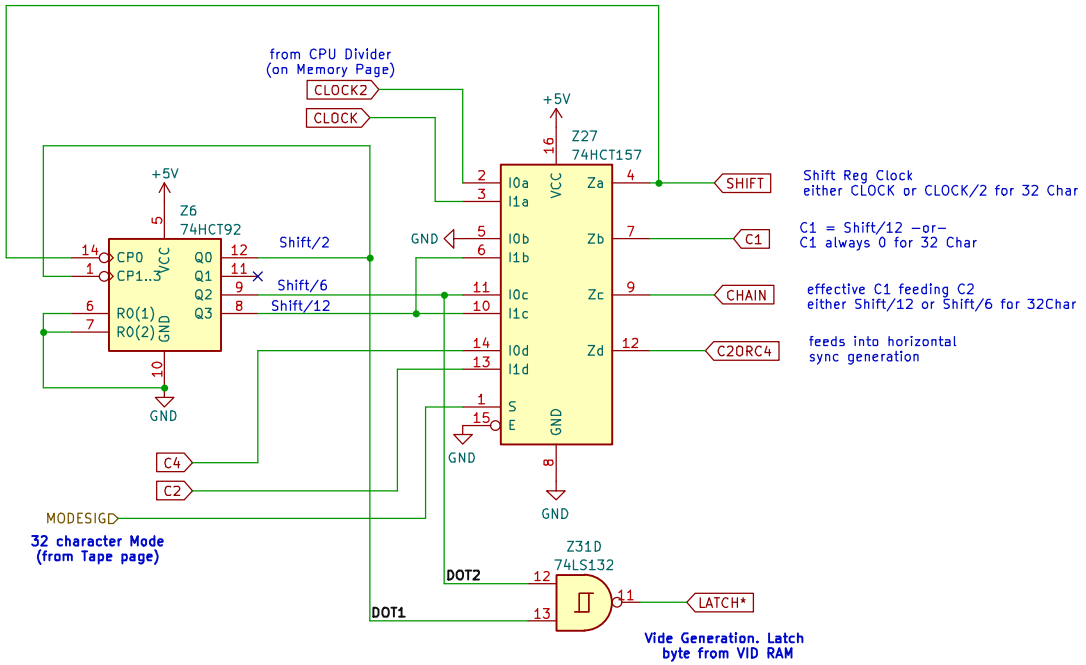
32kB - 28 pin - $28

Manufacturer : Microchip Technology
Part Number : SST39SF010A-70-4C-PHE
Description : FLASH Memory IC 1Mbit Parallel 70 ns 32-PDIP

128 KB - 32 Pin $5

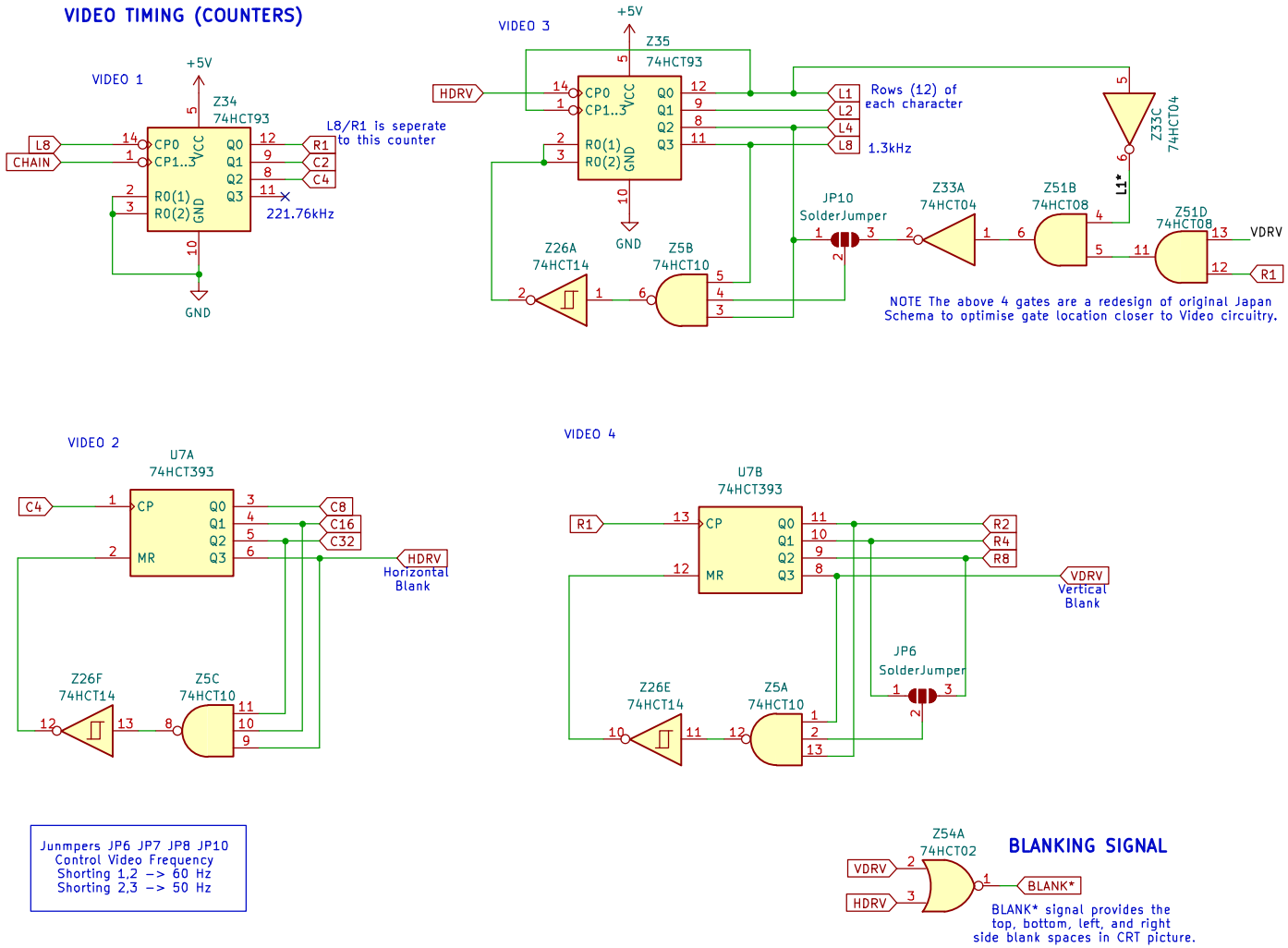
Sheet: /ROM/		
File: TRS80IJP_ROM.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 7/22

32 CHAR MODE CONTROL

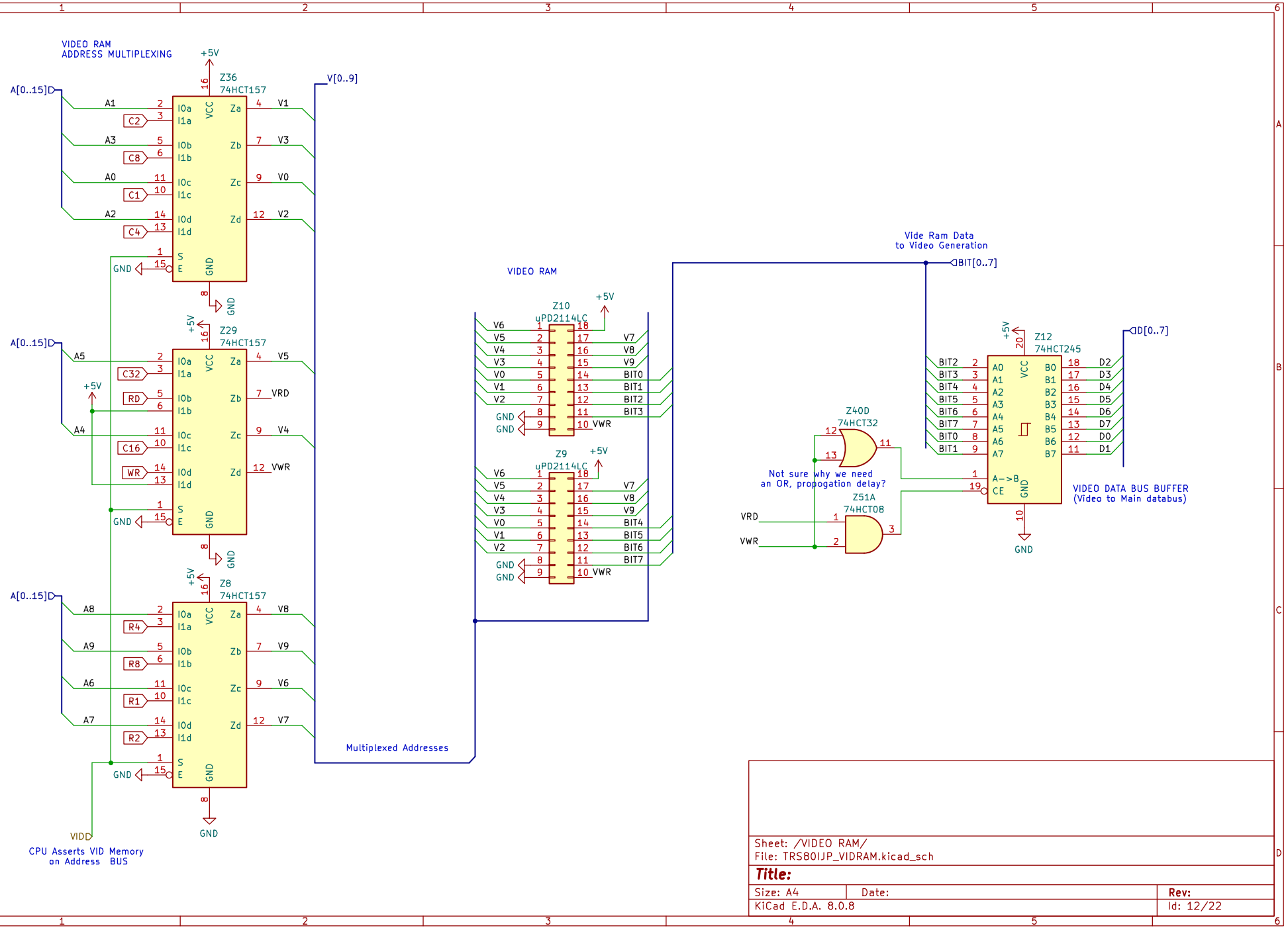


Sheet: /VIDEO MODE/		
File: TRS80IJP_VIDMODE.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 10/22

VIDEO TIMING (COUNTERS)



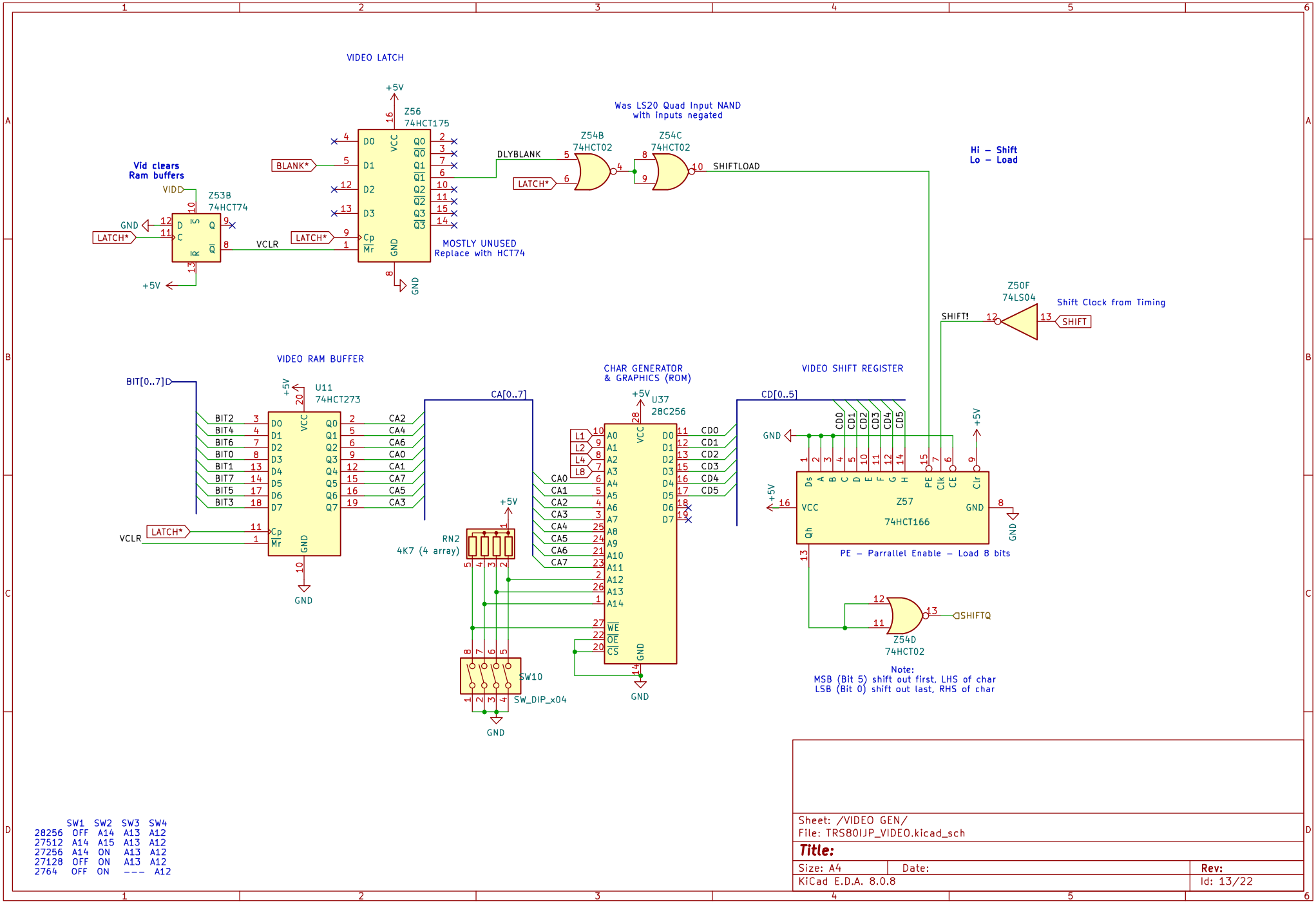
Sheet: /VIDEO TIMING/	
File: TRS80IJP_TIMING.kicad_sch	
Title:	
Size: A4	Date:
KiCad E.D.A. 8.0.8	Id: 11/22



Sheet: /VIDEO RAM/
File: TRS80IJP_VIDRAM.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 12/22

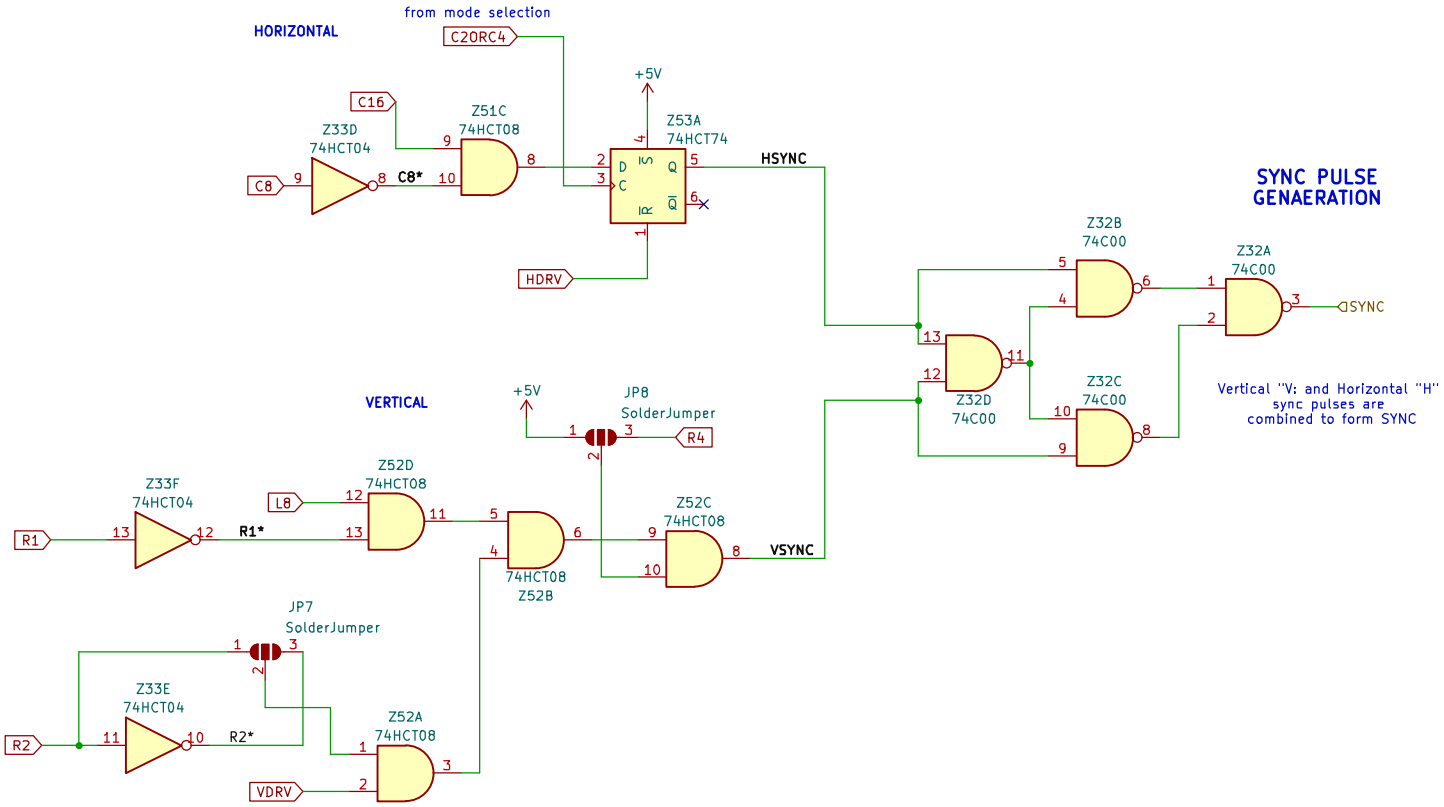


	SW1	SW2	SW3	SW4
28256	OFF	A14	A13	A12
27512	A14	A15	A13	A12
27256	A14	ON	A13	A12
27128	OFF	ON	A13	A12
2764	OFF	ON	---	A12

Sheet: /VIDEO GEN/
File: TRS80IJP_VIDEO.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 13/22

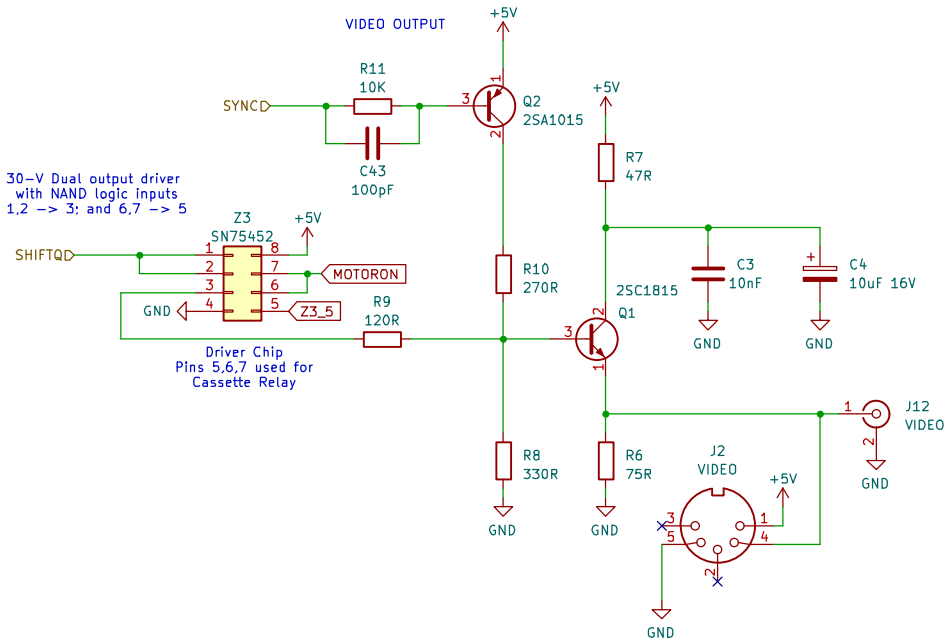


Junmpers JP6 JP7 JP8 JP10
Control Video Frequency
Shorting 1,2 -> 60 Hz
Shorting 2,3 -> 50 Hz

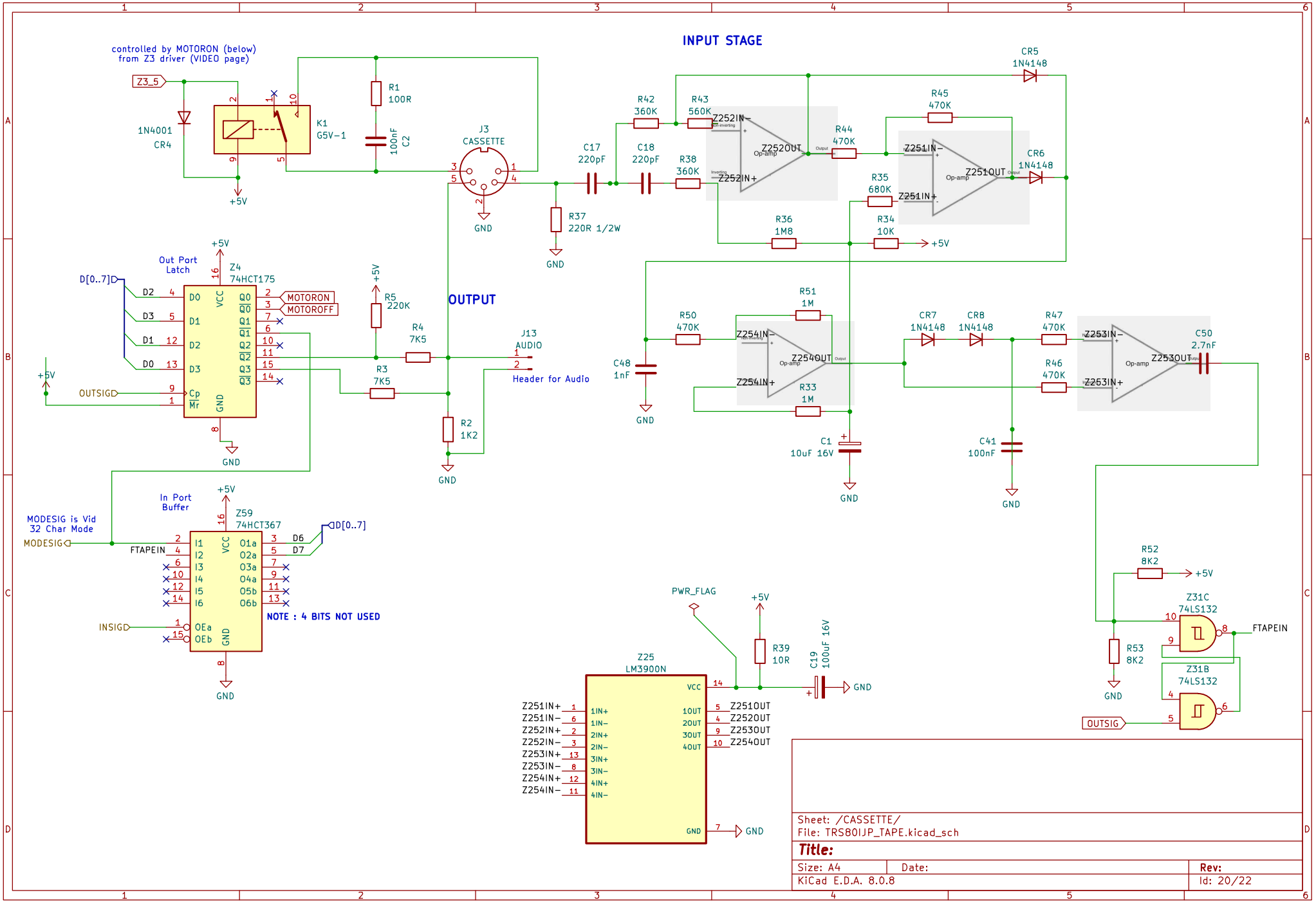
Sheet: /VIDEO SYNC/
File: TRS80IJP_VIDSYNC.kicad_sch

Title:

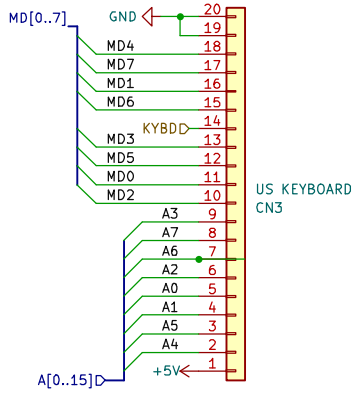
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 14/22

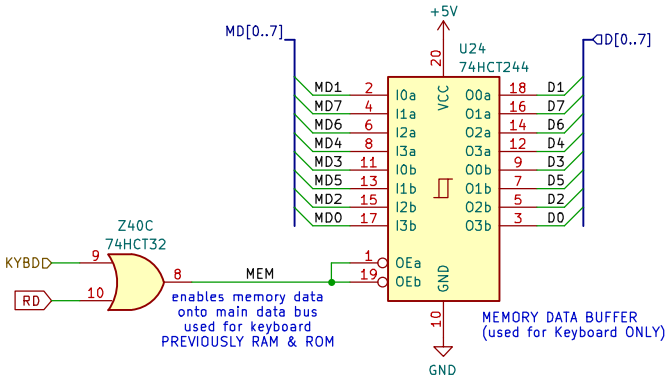


Sheet: /VIDEO OUT/		
File: TRS80JP_VIDOUT.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 15/22


INPUT STAGE
OUTPUT
controlled by MOTORON (below)
from Z3 driver (VIDEO page)
Z3_5
1N4001
CR4
K1
G5V-1
R1
100R
C2
100nF
J3
CASSETTE
+5V
GND
C17
220pF
C18
220pF
R42
360K
R43
560K
R38
360K
R37
220R 1/2W
Z252IN−
Z252IN+
Z2520UT
R44
470K
R45
470K
Z251IN−
Z251IN+
Z251OUT
CR5
1N4148
CR6
1N4148
R35
680K
R36
1M8
R34
10K
Out Port
Latch
Z4
74HCT175
D[0..7]
D2
D3
D1
D0
OUTSIGD
MOTORON
MOTOROFF
R5
220K
R4
7K5
R3
7K5
R2
1K2
J13
AUDIO
Header for Audio
R51
1M
R50
470K
C48
1nF
Z254IN−
Z254IN+
Z2540UT
R33
1M
CR7
1N4148
CR8
1N4148
R47
470K
R46
470K
Z253IN−
Z253IN+
Z2530UT
C50
2.7nF
C1
10uF 16V
C41
100nF
In Port
Buffer
Z59
74HCT367
MODESIG is Vid
32 Char Mode
MODESIG
FTAPEIN
INSIGD
D[0..7]
D6
D7
NOTE : 4 BITS NOT USED
PWR_FLAG
Z25
LM3900N
R39
10R
C19
100uF 16V
Z2510UT
Z2520UT
Z2530UT
Z2540UT
R52
8K2
R53
8K2
Z31C
74LS132
Z31B
74LS132
FTAPEIN
OUTSIG
Sheet: /CASSETTE/
File: TRS80IJP_TAPE.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.8
Id: 20/22

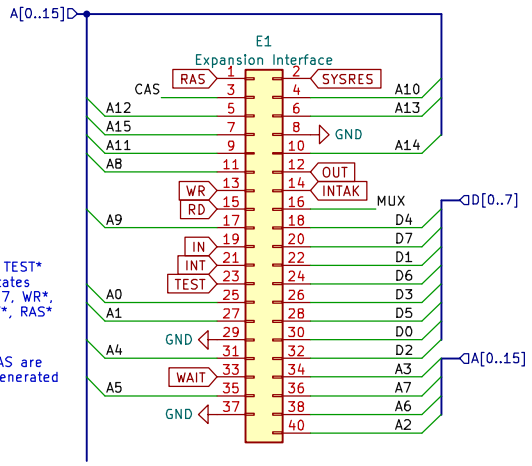
KEYBOARD CONNECTOR





Sheet: /KEYBOARD/		
File: TRS801JP_KB_CONN.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 21/22

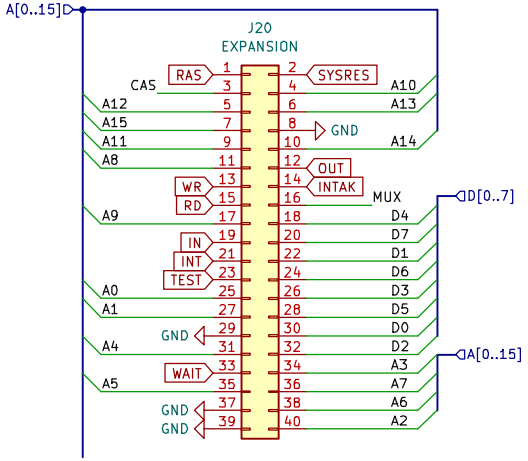
EXPANSION EDGE CONNECTOR

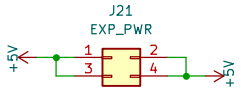


A logic 0 on TEST* input tri-states A0-A15, D0-D7, WR*, RD*, IN*, OUT*, RAS*

MUX and CAS are NO LONGER Generated

INTERNAL EXPANSION HEADER

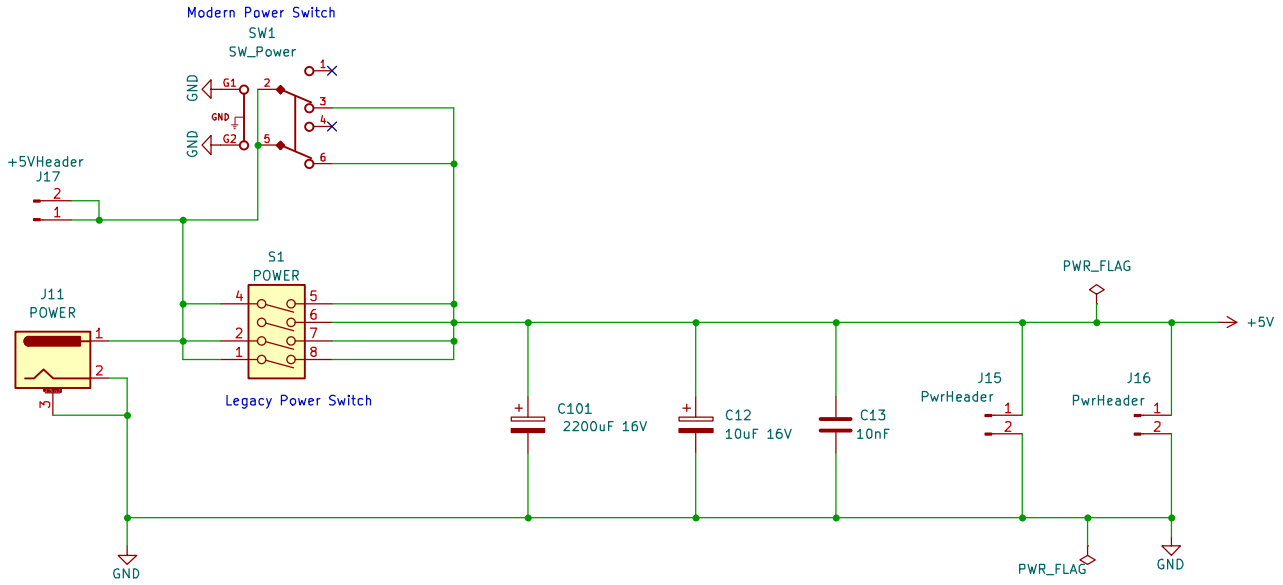




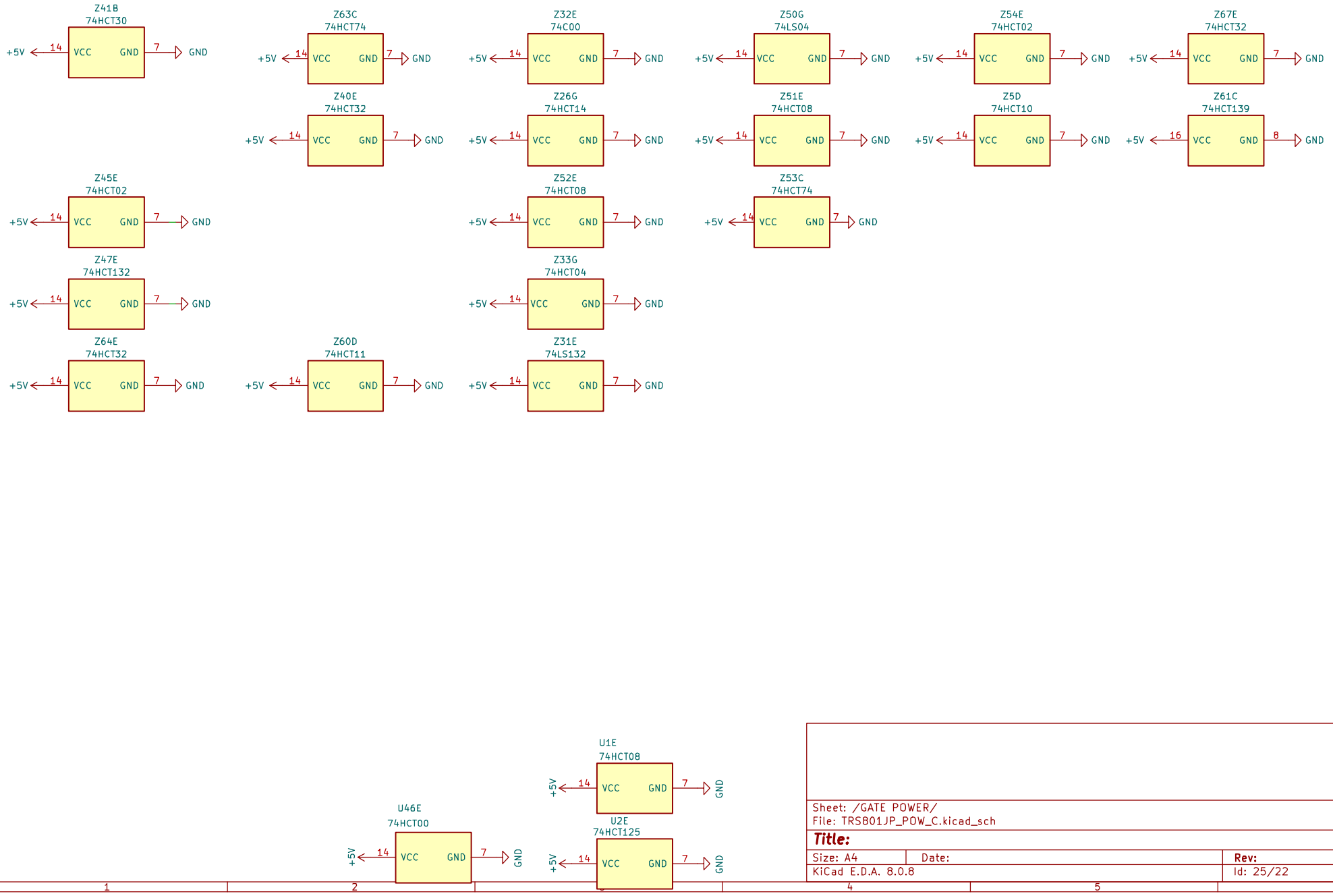
Sheet: /EXPANSION-I-O/
File: TRS80IJP_KEYBOARD.kicad_sch

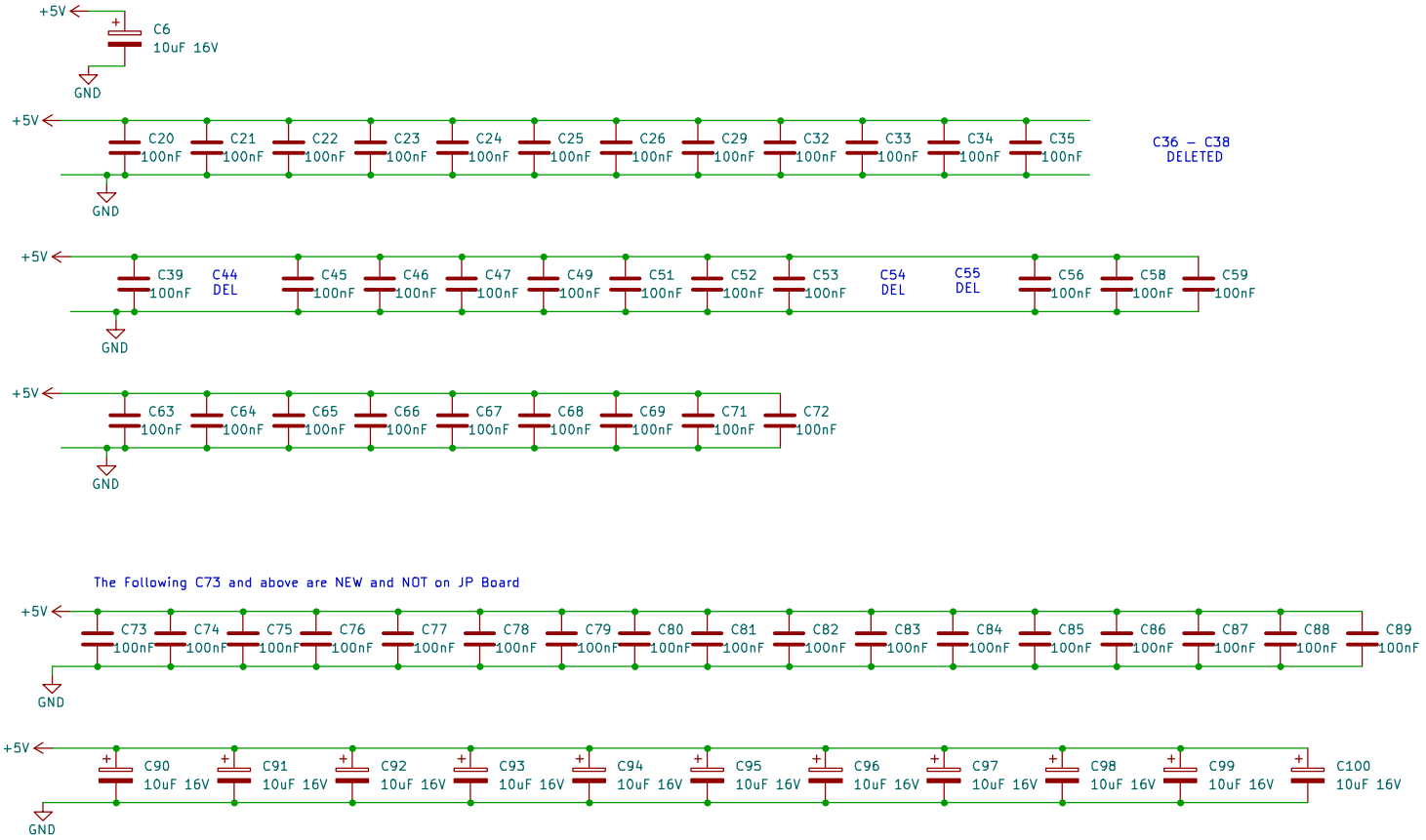
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 22/22



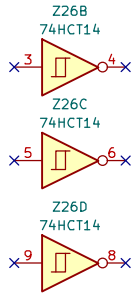
Sheet: /POWER/		
File: TRS80IJP_POWER.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 23/22


Z41B
74HCT30
Z63C
74HCT74
Z32E
74C00
Z50G
74LS04
Z54E
74HCT02
Z67E
74HCT32
Z40E
74HCT32
Z26G
74HCT14
Z51E
74HCT08
Z5D
74HCT10
Z61C
74HCT139
Z45E
74HCT02
Z52E
74HCT08
Z53C
74HCT74
Z47E
74HCT132
Z33G
74HCT04
Z64E
74HCT32
Z60D
74HCT11
Z31E
74LS132
U46E
74HCT00
U1E
74HCT08
U2E
74HCT125
+5V
GND
VCC
Sheet: /GATE POWER/
File: TRS801JP_POW_C.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.8
Id: 25/22

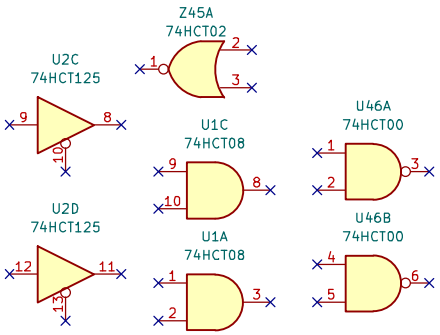


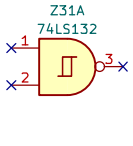
Sheet: /DECOUPLING/		
File: TRS80JP_DECOUPLE.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 26/22

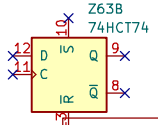
Spare Gates are SHOWN in general PHYSICAL LOCATION on the Board



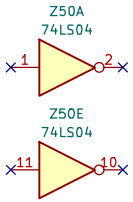
think move 2 used Inverters to NAND and Delete Inverters

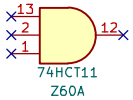






NOTE From Tech Manual –> REMOVED this and Grounded Pins Notice pins 6 and 7 of Z58. These inputs are used to clear the counter to zero. If you find CTR on sheet 1, you will see it comes from inverter Z42, pin 8, which controls the CPU CLK divider. Normally, CTR is held low. Only during automatic testing at the factory is CTR allowed to go high and clear Z58. You might find "A" and "D" Level Boards with Z58, pins 6 and 7, simply tied to ground.





Sheet: /SPARE GATES/
File: TRS80IJP_SPARE.kicad_sch

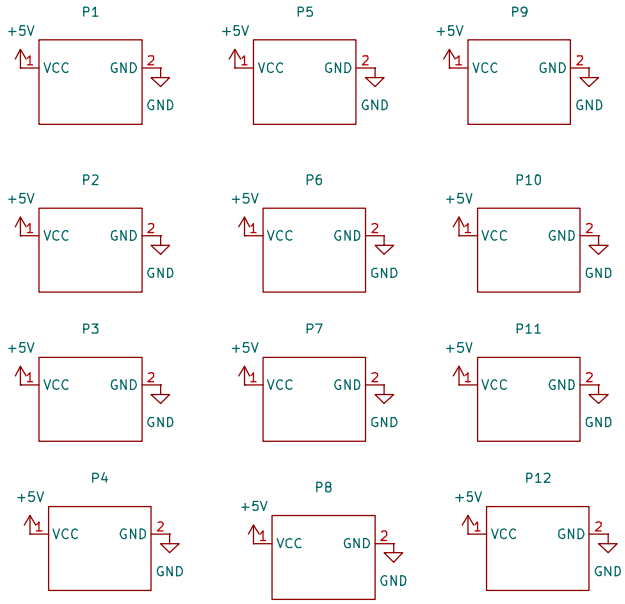
Title:

Size: A4 | Date: | **Rev:**
KiCad E.D.A. 8.0.8 | Id: 27/22

MOUNTING HOLES

H1 MountingHole
H2 MountingHole
H3 MountingHole
H4 MountingHole
H5 MountingHole
H6 MountingHole
H7 MountingHole
H9 MountingHole
H8 MountingHole

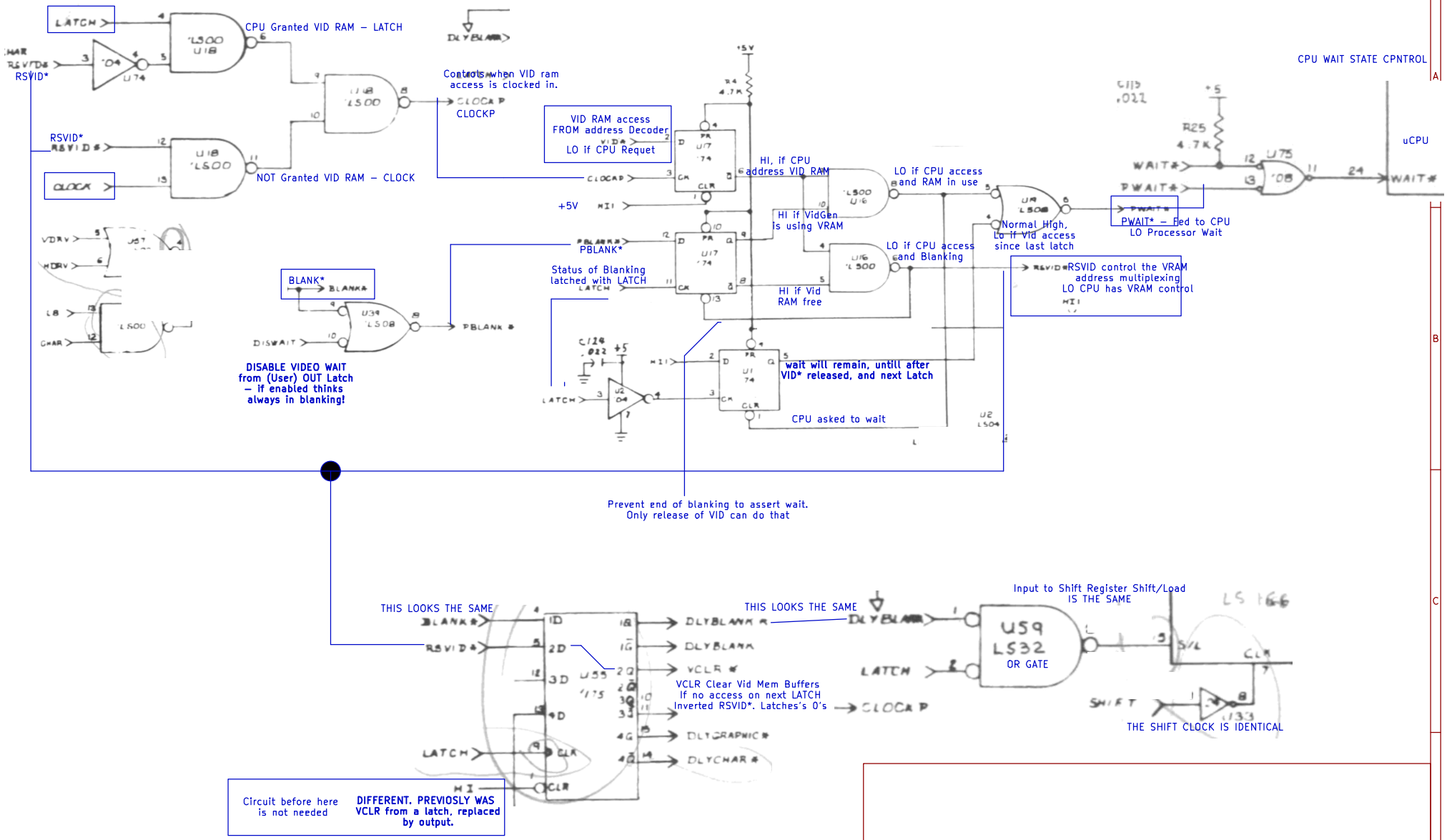
PROTOTYPE AREAS



Sheet: /HARDWARE/
File: TRS801JP_HW.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 28/22



on a Model III, a glitched line of a character doesn't exactly glitch to black. What happens is that when the redisplay hardware tries to read a character from video RAM and loses to a competing read by the CPU, the byte vale zero is returned, and then a line of character zero is drawn. Thus, if you use a chargen that doesn't have a blank in character zero, then instead of lines glitching to black, they'll glitch to lines of character zero, with some white pixels.

Sheet: /Untitled Sheet/
File: untitled.kicad_sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.8		Id: 50/22