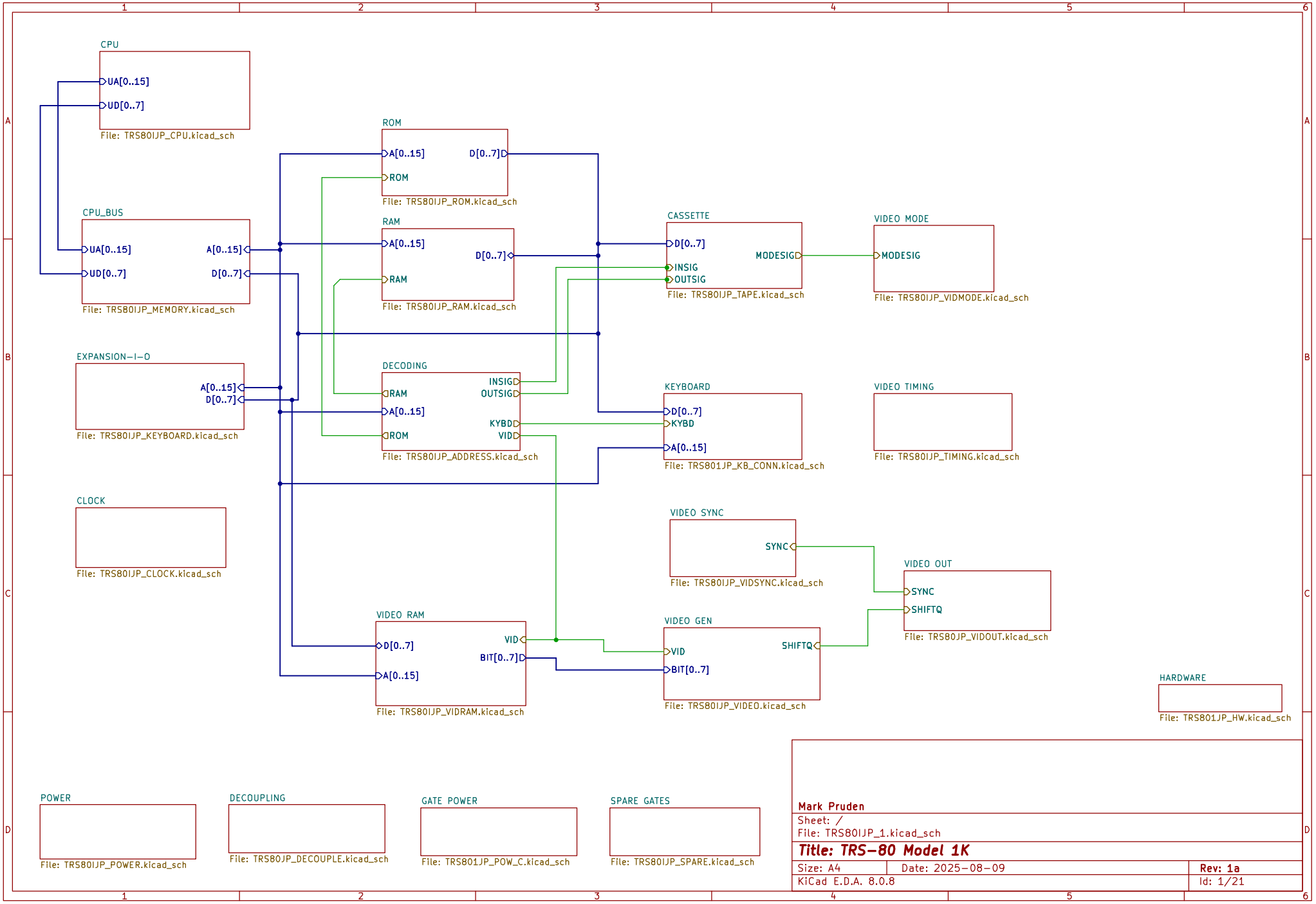


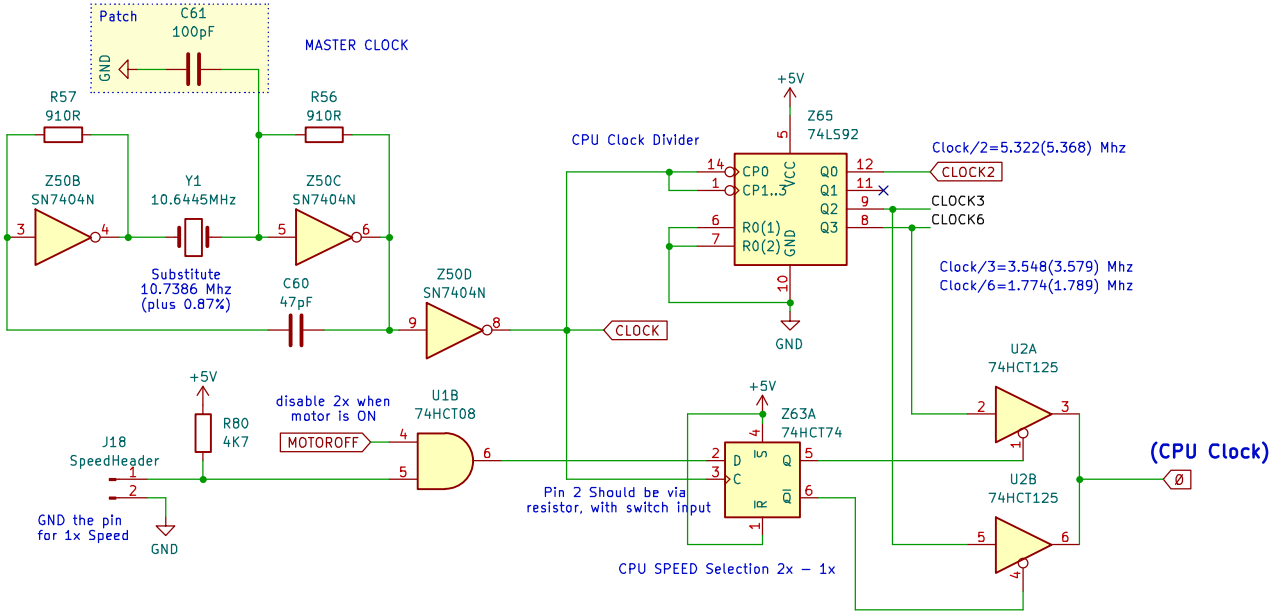

Mark Pruden

Sheet: /

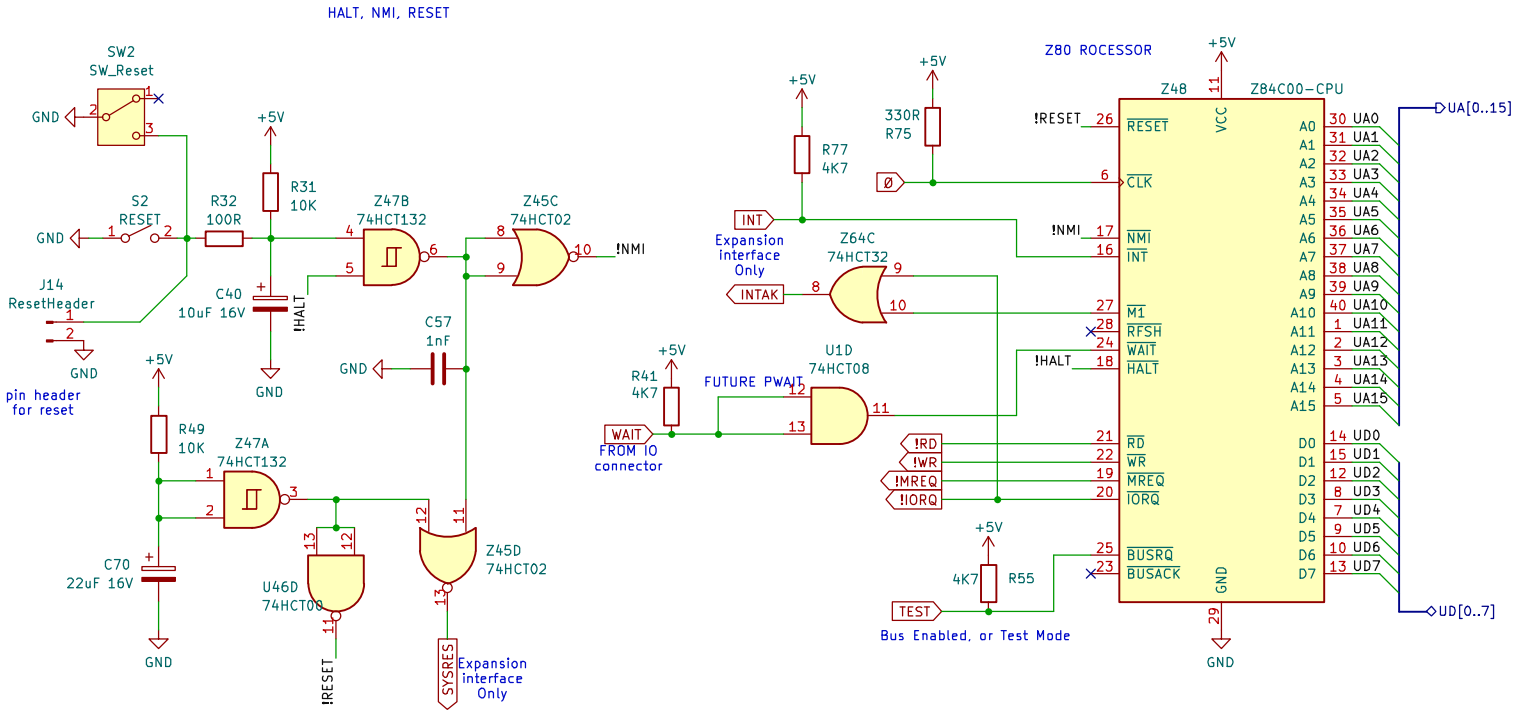
File: TRS80IJP_1.kicad_sch

**Title: TRS-80 Model 1K**

| Size: A4 | Date: 2025-08-09 | Rev: 1a |
|---|---|---|
| KiCad E.D.A. 8.0.8 | | Id: 1/21 |

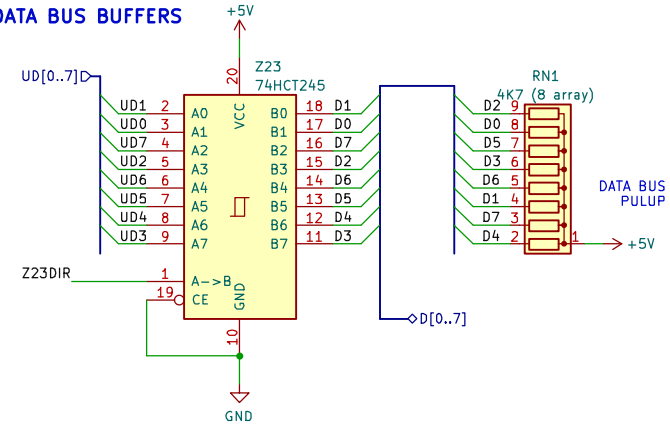



| | | |
|---|---|---|
| Mark Pruden | | |
| Sheet: /CLOCK/ | | |
| File: TRS80IJP_CLOCK.kicad_sch | | |
| **Title: TRS-80 Model 1K** | | |
| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
| KiCad E.D.A. 8.0.8 | | Id: 2/21 |

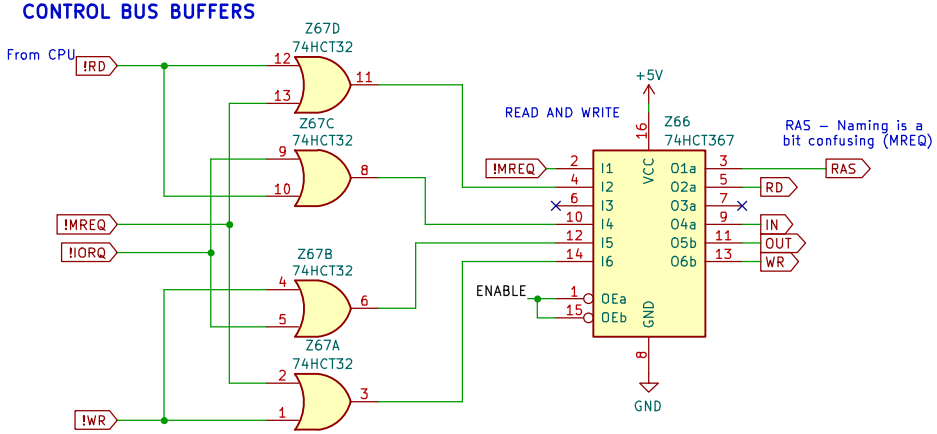



| | | |
|---|---|---|
| Mark Pruden | | |
| Sheet: /CPU/ | | |
| File: TRS80IJP_CPU.kicad_sch | | |
| **Title: TRS-80 Model 1K** | | |
| Size: A4 | Date: 2025-08-09 | Rev: 1a |
| KiCad E.D.A. 8.0.8 | | Id: 3/21 |

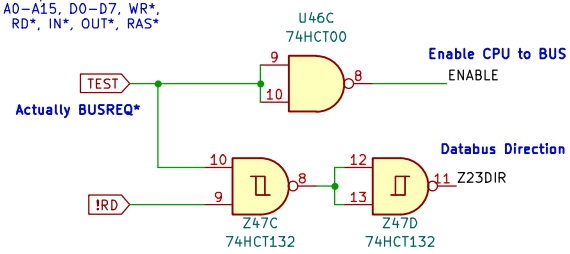
## DATA BUS BUFFERS



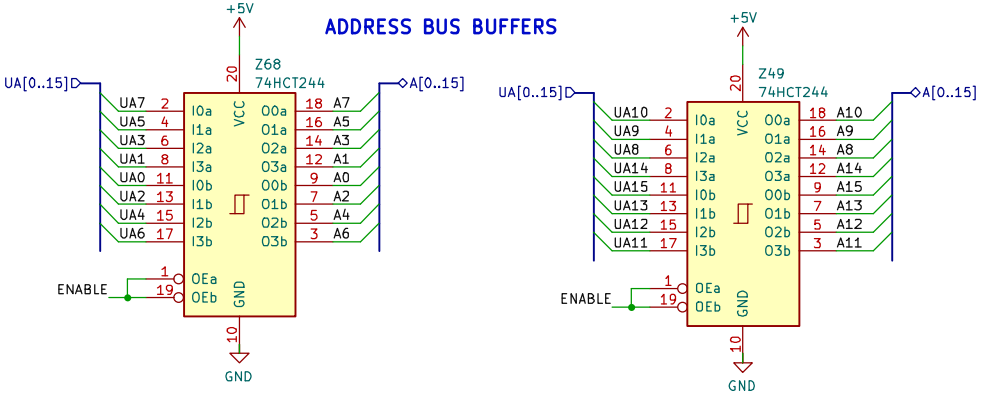

## CONTROL BUS BUFFERS




A logic 0 on TEST*
input tri-states
A0–A15, D0–D7, WR*,
RD*, IN*, OUT*, RAS*



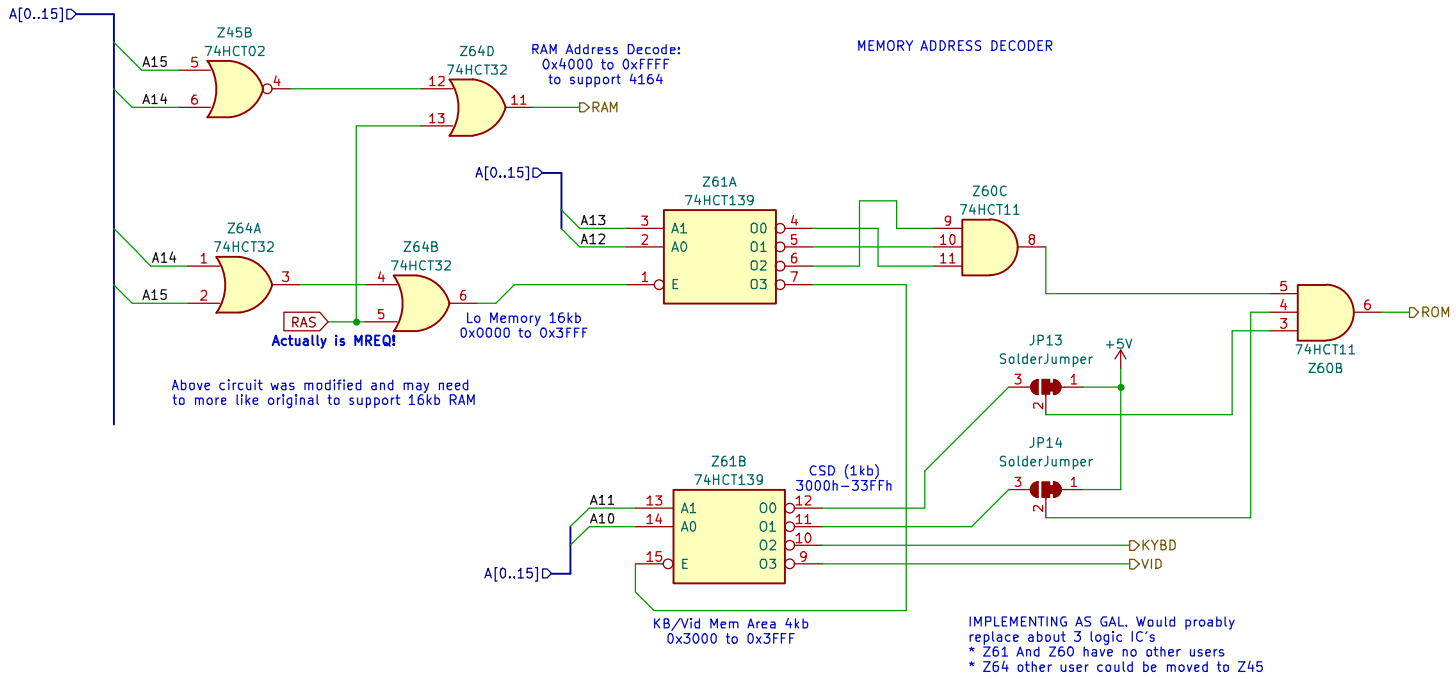

## ADDRESS BUS BUFFERS

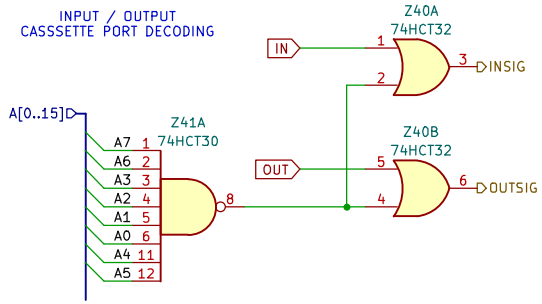



Mark Pruden
Sheet: /CPU_BUS/
File: TRS80IJP_MEMORY.kicad_sch

**Title: TRS-80 Model 1K**

| Size: A4 | Date: 2025-08-09 | Rev: 1a |
|---|---|---|
| KiCad E.D.A. 8.0.8 | | Id: 4/21 |



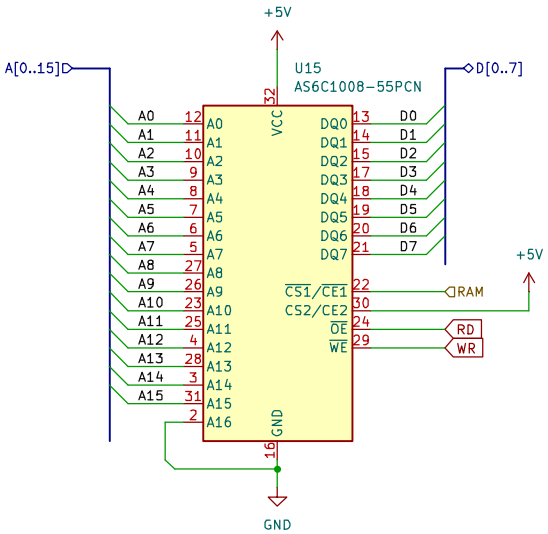

Mark Pruden

Sheet: /DECODING/

File: TRS80IJP_ADDRESS.kicad_sch

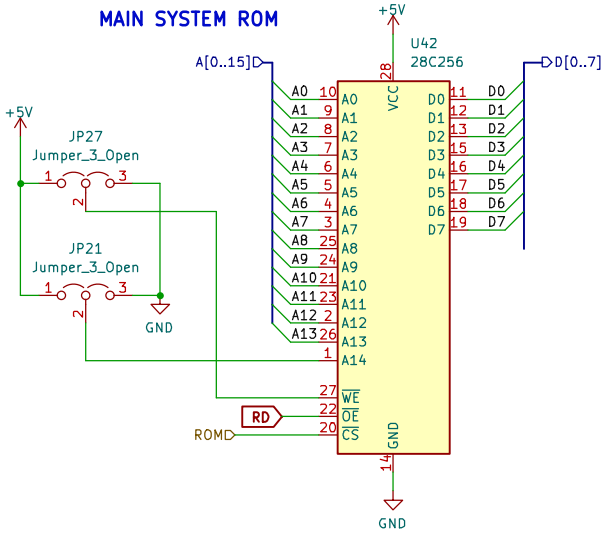
**Title: TRS-80 Model 1K**

| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
|---|---|---|
| KiCad E.D.A. 8.0.8 | | Id: 5/21 |




Manufacturer : Alliance Memory, Inc.
Part Number : AS6C1008-55PCN
Description : SRAM - Asynchronous Memory IC 1Mbit Parallel 55 ns 32-SOP

| | | |
|---|---|---|
| Mark Pruden | | |
| Sheet: /RAM/ | | |
| File: TRS80IJP_RAM.kicad_sch | | |
| **Title: TRS-80 Model 1K** | | |
| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
| KiCad E.D.A. 8.0.8 | | Id: 6/21 |




Manufacturer : Microchip Technology
Part Number : AT28C256-15PU
Description : EEPROM Memory IC 256Kbit Parallel 150 ns 28-PDIP

32kB - 28 pin - $28

Manufacturer : Microchip Technology
Part Number : SST39SF010A-70-4C-PHE
Description : FLASH Memory IC 1Mbit Parallel 70 ns 32-PDIP

128 KB - 32 Pin $5

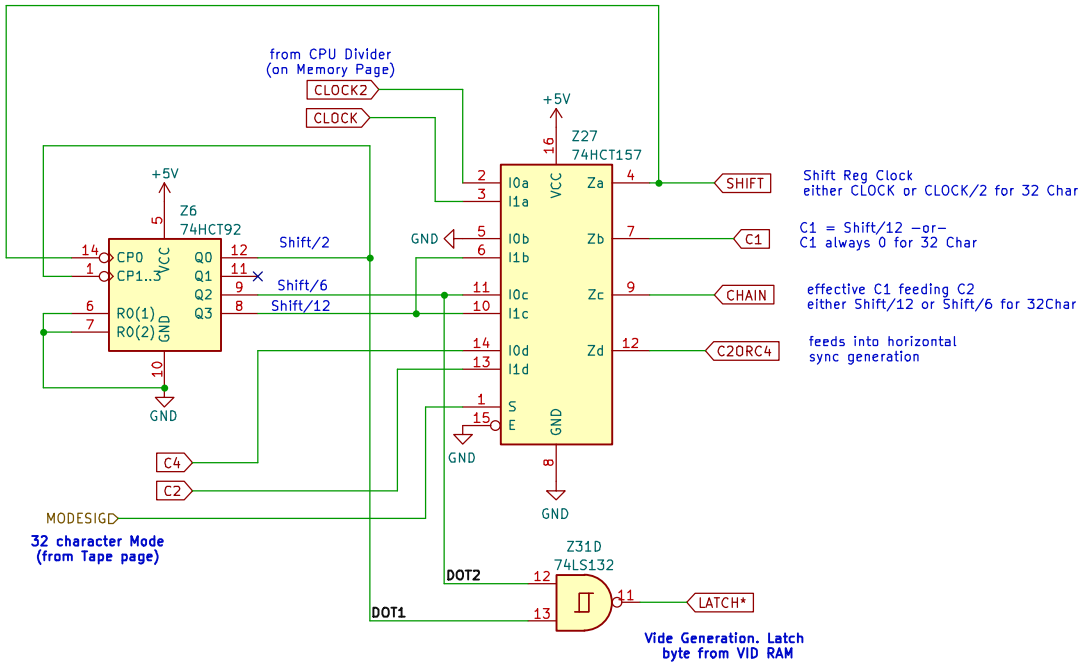
Mark Pruden

Sheet: /ROM/
File: TRS80IJP_ROM.kicad_sch

**Title: TRS-80 Model 1K**

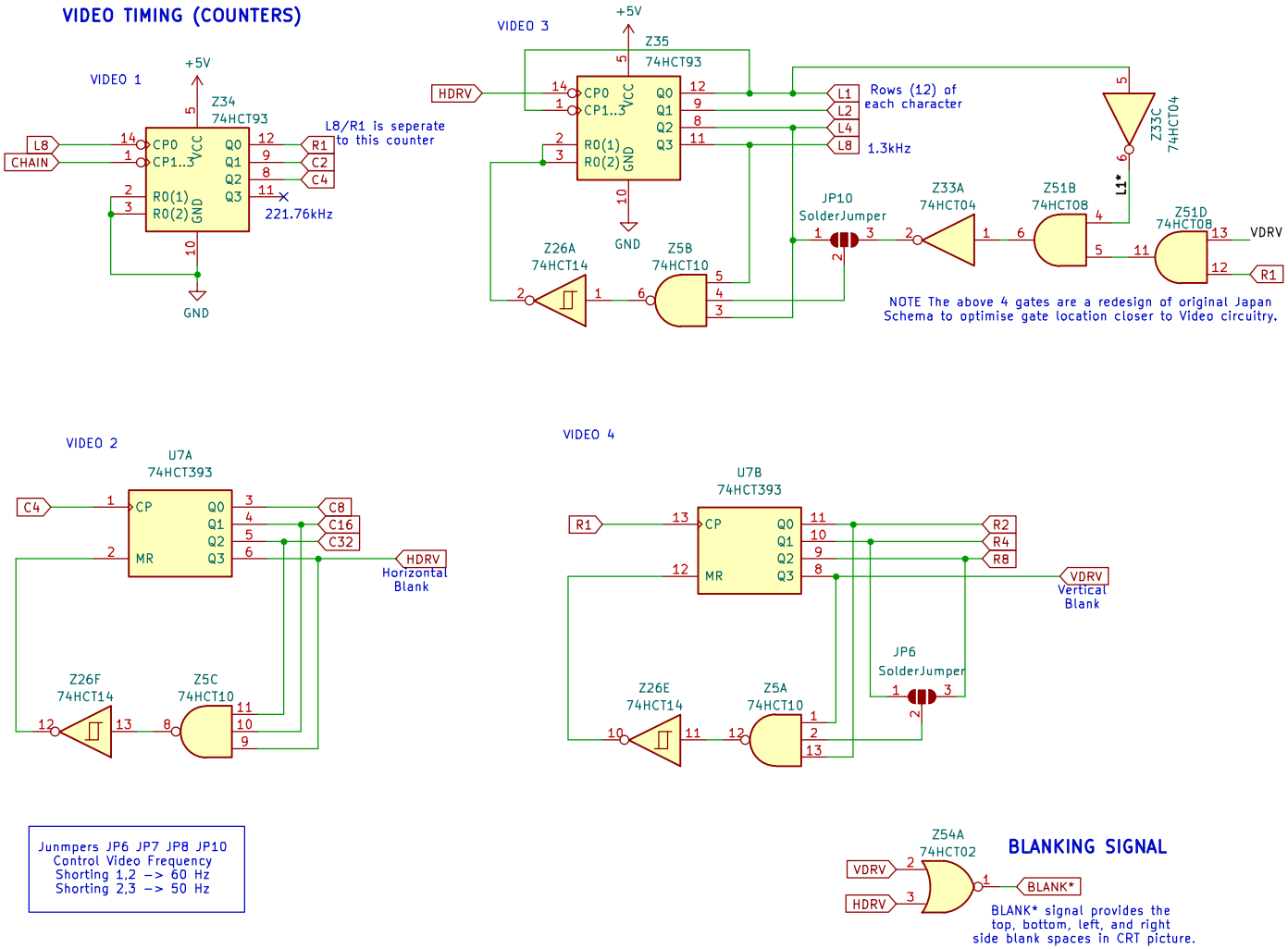
| Size: A4 | Date: 2025-08-09 | Rev: 1a |
|---|---|---|
| KiCad E.D.A. 8.0.8 | | Id: 7/21 |

# 32 CHAR MODE CONTROL

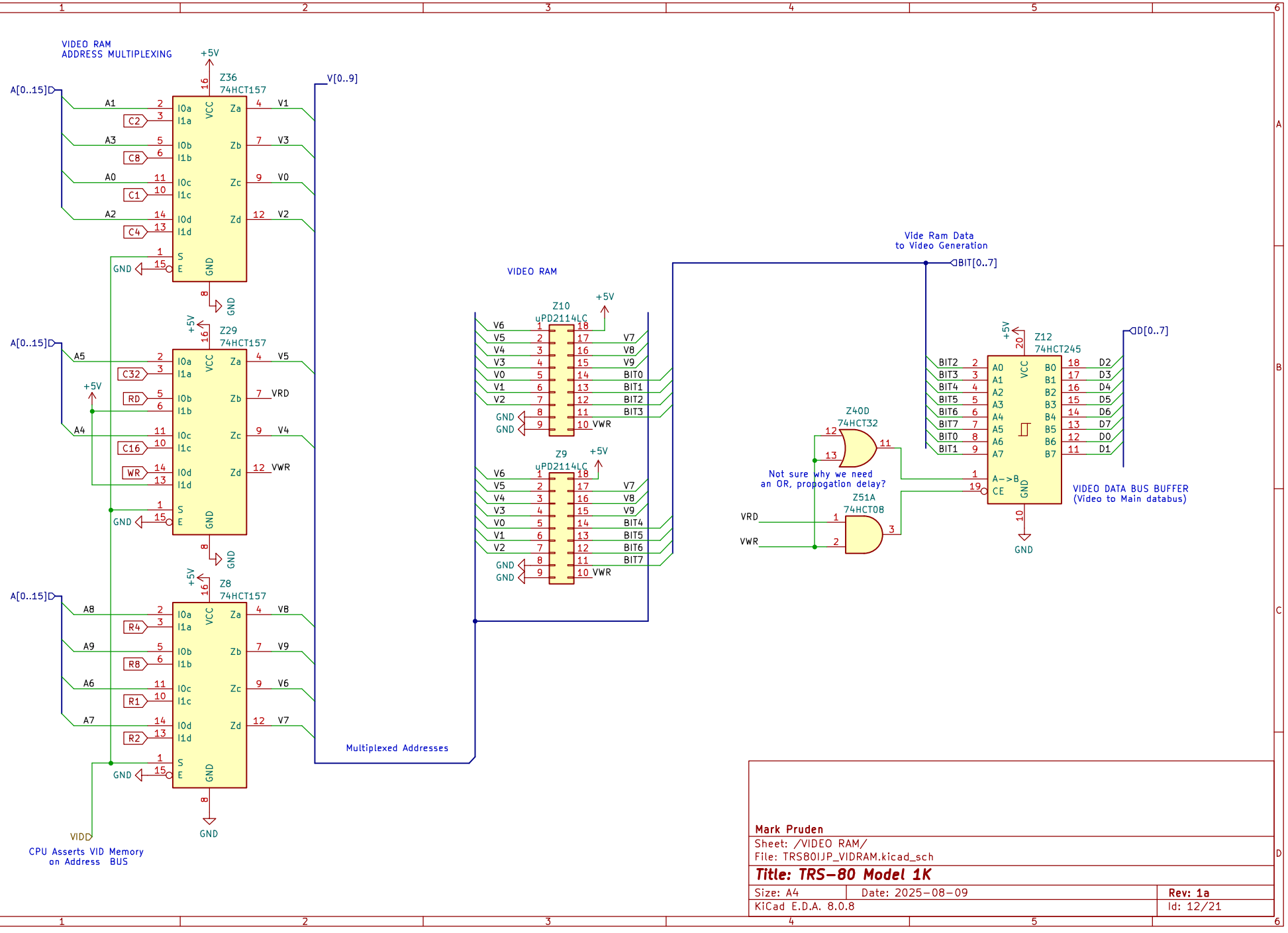


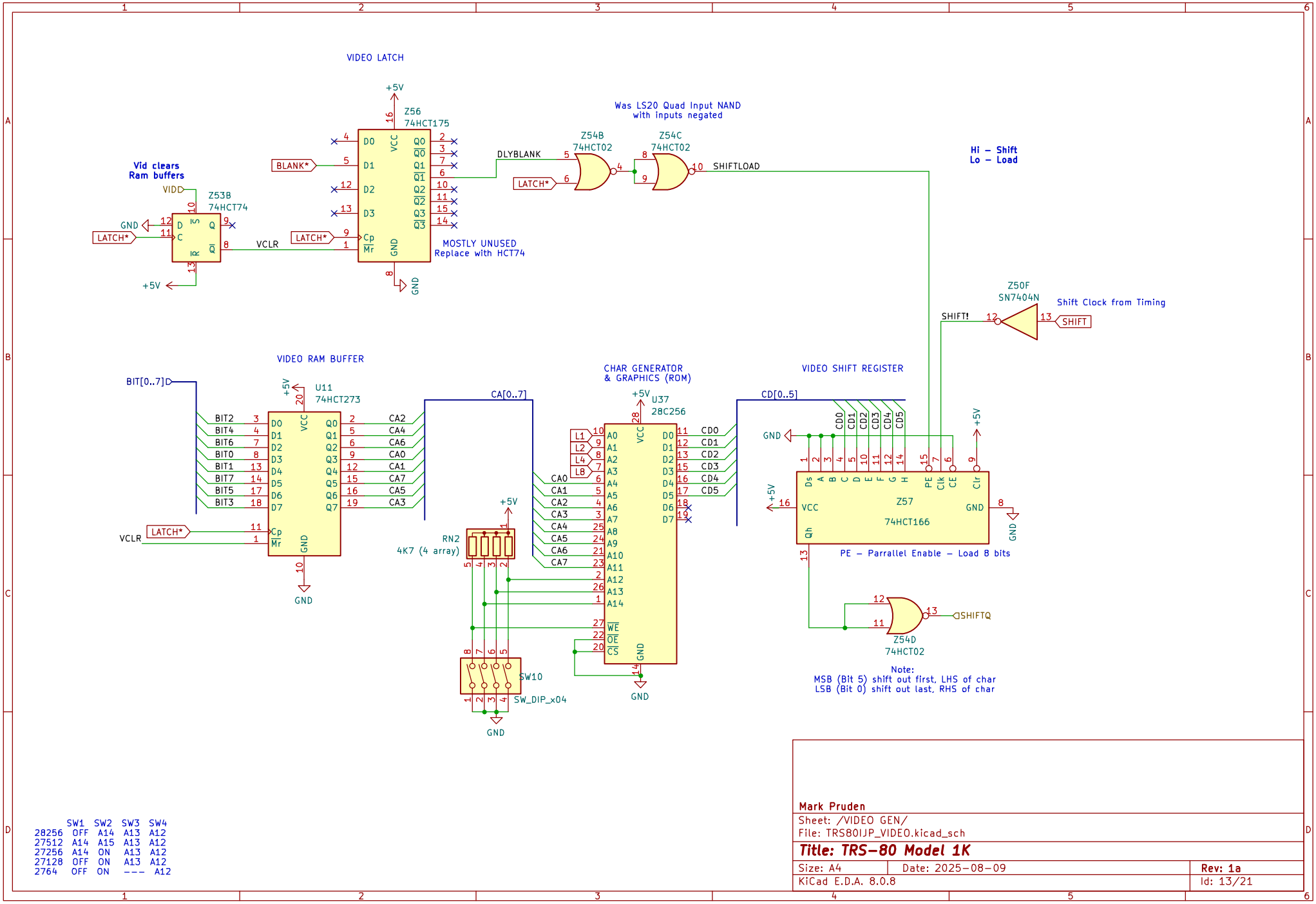

| | | |
|---|---|---|
| Mark Pruden | | |
| Sheet: /VIDEO MODE/ | | |
| File: TRS80IJP_VIDMODE.kicad_sch | | |
| **Title: TRS-80 Model 1K** | | |
| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
| KiCad E.D.A. 8.0.8 | | Id: 10/21 |

## VIDEO TIMING (COUNTERS)




| | | |
|---|---|---|
| Mark Pruden | | |
| Sheet: /VIDEO TIMING/ | | |
| File: TRS80IJP_TIMING.kicad_sch | | |
| **Title: TRS-80 Model 1K** | | |
| Size: A4 | Date: 2025-08-09 | Rev: 1a |
| KiCad E.D.A. 8.0.8 | | Id: 11/21 |


VIDEO RAM
ADDRESS MULTIPLEXING
A[0..15]
+5V
Z36
74HCT157
A1
C2
A3
C8
A0
C1
A2
C4
V1
V3
V0
V2
V[0..9]
GND
Z29
74HCT157
A5
C32
RD
A4
C16
WR
V5
VRD
V4
VWR
Z8
74HCT157
A8
R4
A9
R8
A6
R1
A7
R2
V8
V9
V6
V7
Multiplexed Addresses
VIDD
CPU Asserts VID Memory
on Address BUS
VIDEO RAM
Z10
uPD2114LC
Z9
uPD2114LC
V6
V5
V4
V3
V0
V1
V2
BIT0
BIT1
BIT2
BIT3
BIT4
BIT5
BIT6
BIT7
Vide Ram Data
to Video Generation
BIT[0..7]
Z40D
74HCT32
Not sure why we need
an OR, propogation delay?
Z51A
74HCT08
Z12
74HCT245
A->B
CE
D[0..7]
VIDEO DATA BUS BUFFER
(Video to Main databus)
Mark Pruden
Sheet: /VIDEO RAM/
File: TRS80IJP_VIDRAM.kicad_sch
Title: TRS-80 Model 1K
Size: A4
Date: 2025-08-09
Rev: 1a
KiCad E.D.A. 8.0.8
Id: 12/21




| | SW1 | SW2 | SW3 | SW4 |
|---|---|---|---|---|
| 28256 | OFF | A14 | A13 | A12 |
| 27512 | A14 | A15 | A13 | A12 |
| 27256 | A14 | ON | A13 | A12 |
| 27128 | OFF | ON | A13 | A12 |
| 2764 | OFF | ON | --- | A12 |

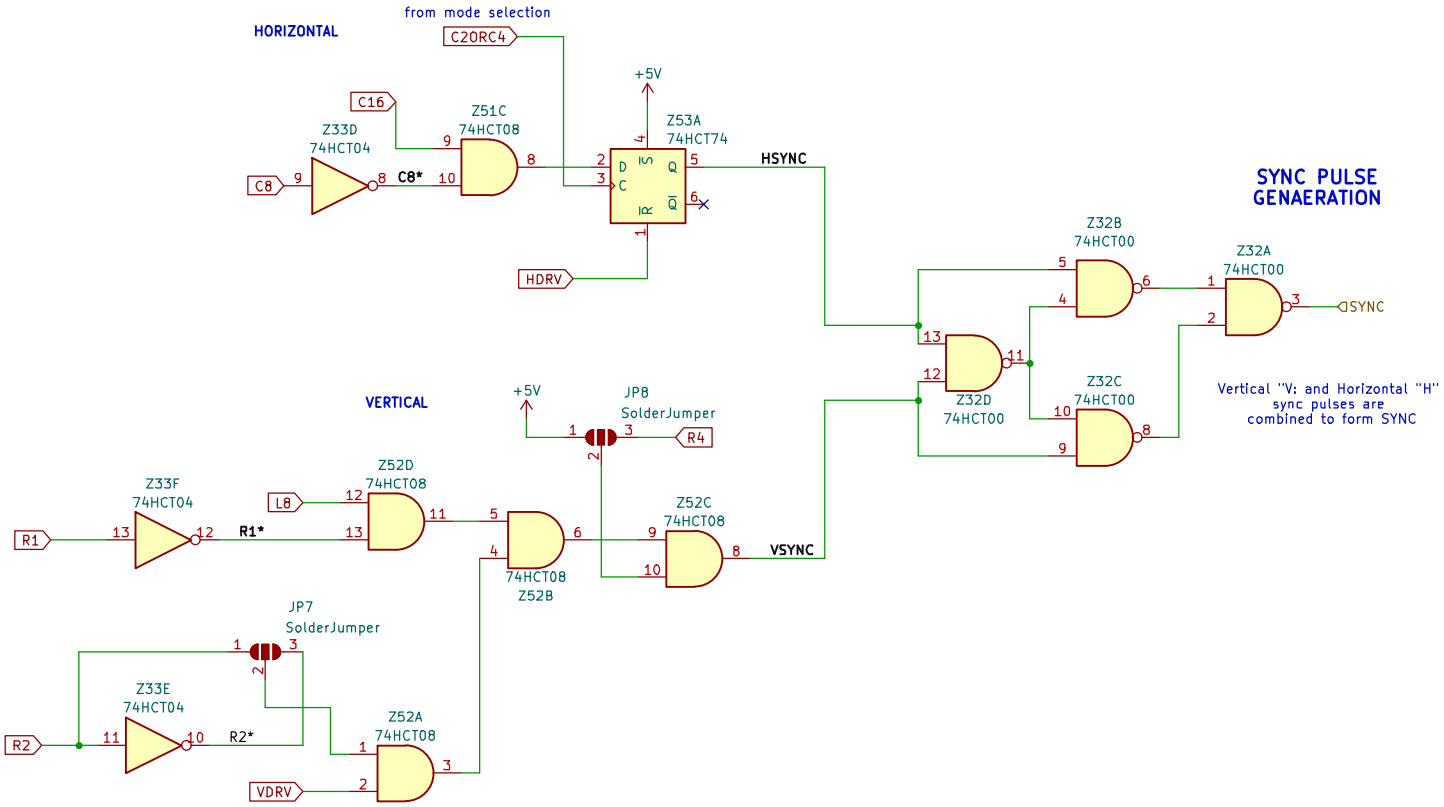
Mark Pruden

Sheet: /VIDEO GEN/

File: TRS80IJP_VIDEO.kicad_sch

**Title: TRS-80 Model 1K**

| | | |
|---|---|---|
| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
| KiCad E.D.A. 8.0.8 | | Id: 13/21 |




Junmpers JP6 JP7 JP8 JP10
Control Video Frequency
Shorting 1,2 -> 60 Hz
Shorting 2,3 -> 50 Hz

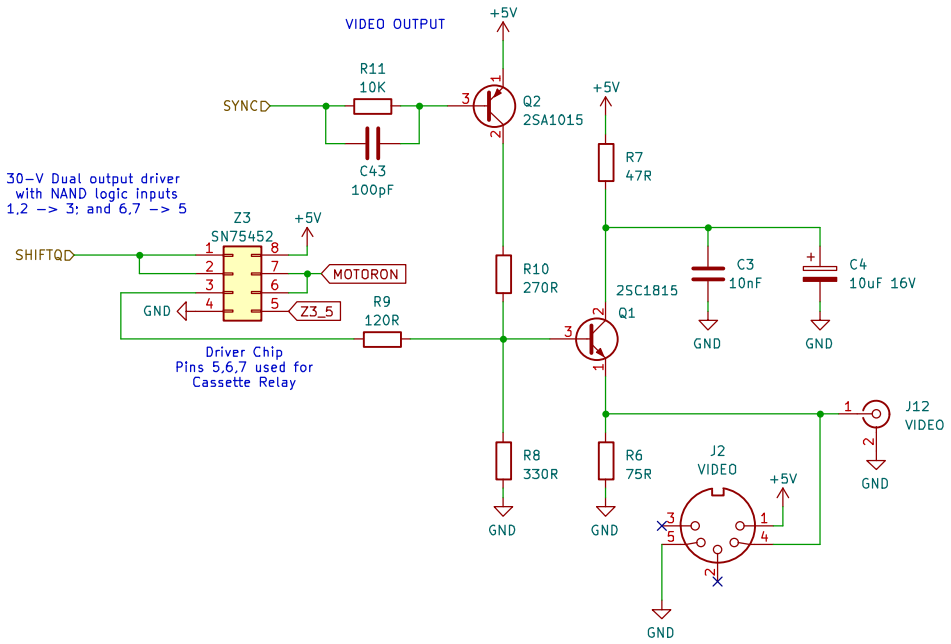
Mark Pruden

Sheet: /VIDEO SYNC/

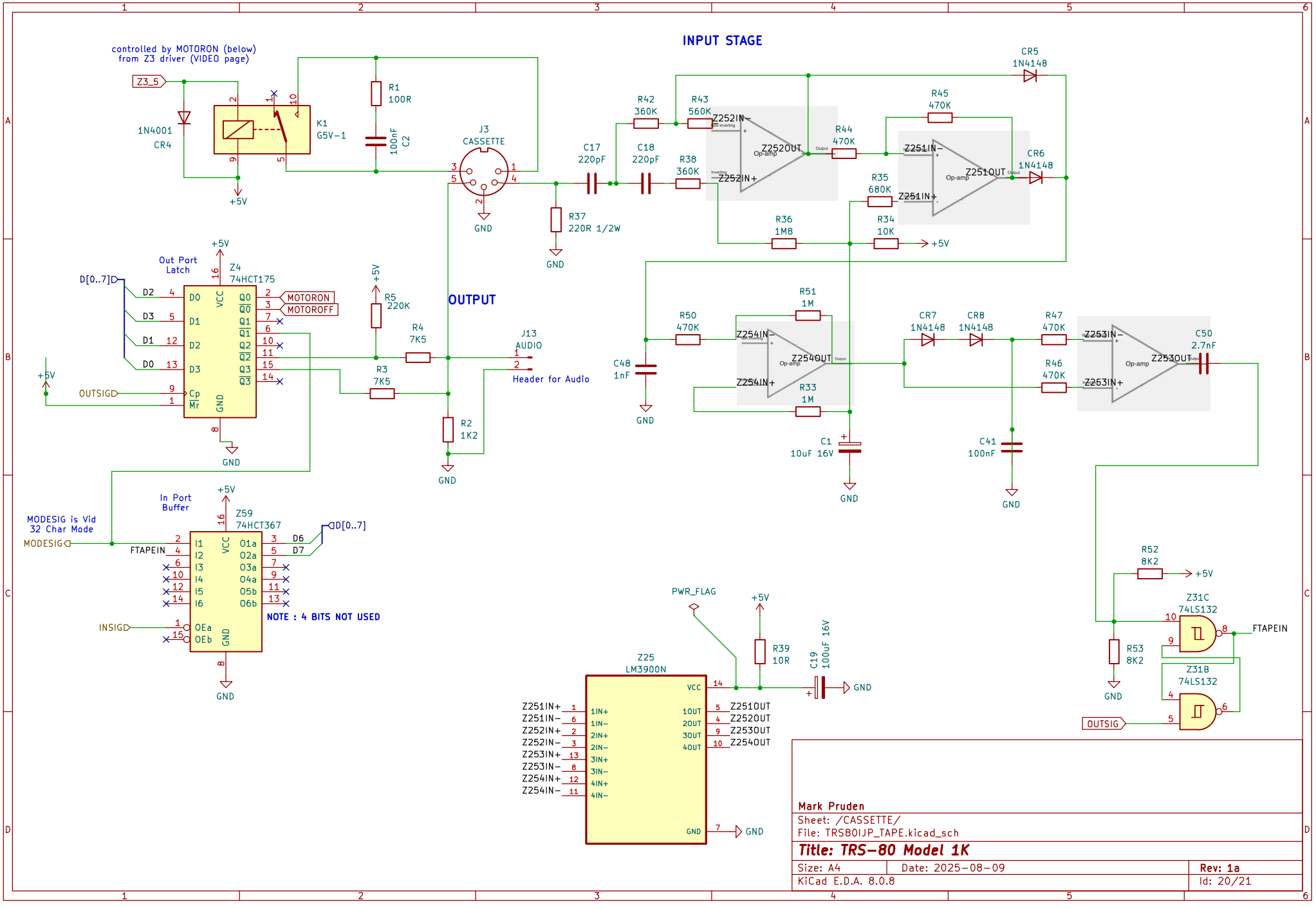
File: TRS80IJP_VIDSYNC.kicad_sch

**Title: TRS-80 Model 1K**

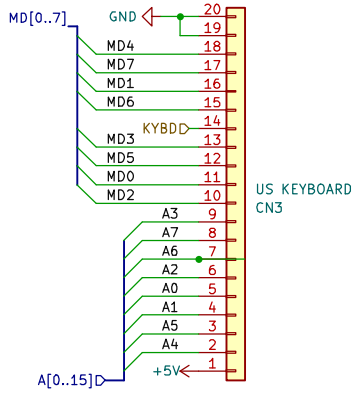
| Size: A4 | Date: 2025-08-09 | Rev: 1a |
|---|---|---|
| KiCad E.D.A. 8.0.8 | | Id: 14/21 |

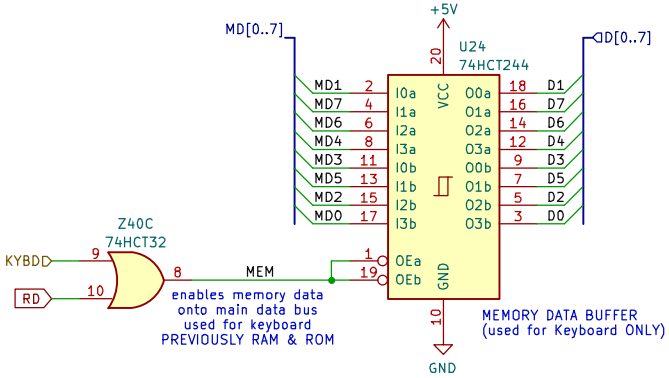



| | | |
|---|---|---|
| Mark Pruden | | |
| Sheet: /VIDEO OUT/ | | |
| File: TRS80JP_VIDOUT.kicad_sch | | |
| **Title: TRS-80 Model 1K** | | |
| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
| KiCad E.D.A. 8.0.8 | | Id: 15/21 |


INPUT STAGE
OUTPUT
controlled by MOTORON (below)
from Z3 driver (VIDEO page)
Z3_5
1N4001
CR4
K1
G5V-1
R1
100R
C2
100nF
J3
CASSETTE
+5V
GND
R37
220R 1/2W
C17
220pF
C18
220pF
R42
360K
R43
560K
R38
360K
Z252IN-
Z252IN+
Z2520UT
R44
470K
R45
470K
Z251IN-
Z251IN+
Z2510UT
CR5
1N4148
CR6
1N4148
R35
680K
R36
1M8
R34
10K
Out Port
Latch
Z4
74HCT175
D[0..7]
D0
D1
D2
D3
OUTSIGD
MOTORON
MOTOROFF
R5
220K
R4
7K5
R3
7K5
R2
1K2
J13
AUDIO
Header for Audio
R51
1M
R50
470K
Z254IN-
Z254IN+
Z2540UT
R33
1M
C48
1nF
CR7
1N4148
CR8
1N4148
R47
470K
R46
470K
Z253IN-
Z253IN+
Z2530UT
C50
2.7nF
C1
10uF 16V
C41
100nF
In Port
Buffer
Z59
74HCT367
MODESIG is Vid
32 Char Mode
MODESIG
FTAPEIN
INSIGD
D[0..7]
D6
D7
NOTE : 4 BITS NOT USED
PWR_FLAG
Z25
LM3900N
R39
10R
C19
100uF 16V
Z2510UT
Z2520UT
Z2530UT
Z2540UT
R52
8K2
R53
8K2
Z31C
74LS132
Z31B
74LS132
FTAPEIN
OUTSIG
Mark Pruden
Sheet: /CASSETTE/
File: TRS80IJP_TAPE.kicad_sch
Title: TRS-80 Model 1K
Size: A4
Date: 2025-08-09
Rev: 1a
KiCad E.D.A. 8.0.8
Id: 20/21

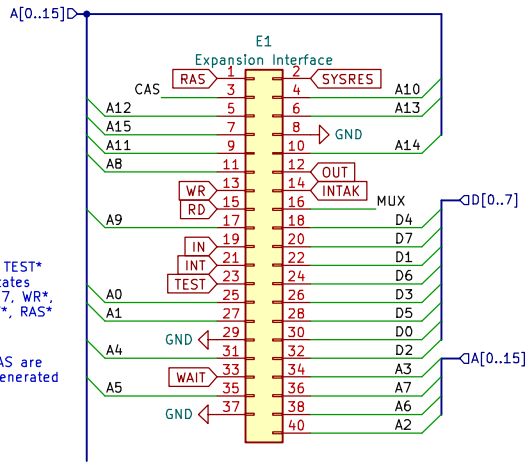
KEYBOARD CONNECTOR




| | | |
|---|---|---|
| Mark Pruden | | |
| Sheet: /KEYBOARD/ | | |
| File: TRS801JP_KB_CONN.kicad_sch | | |
| **Title: TRS-80 Model 1K** | | |
| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
| KiCad E.D.A. 8.0.8 | | Id: 21/21 |

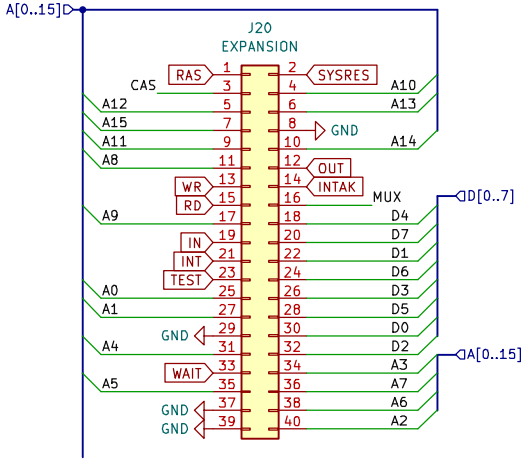
## EXPANSION EDGE CONNECTOR

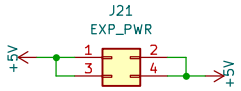



A logic 0 on TEST* input tri-states A0-A15, D0-D7, WR*, RD*, IN*, OUT*, RAS*

MUX and CAS are NO LONGER Generated

## INTERNAL EXPANSION HEADER



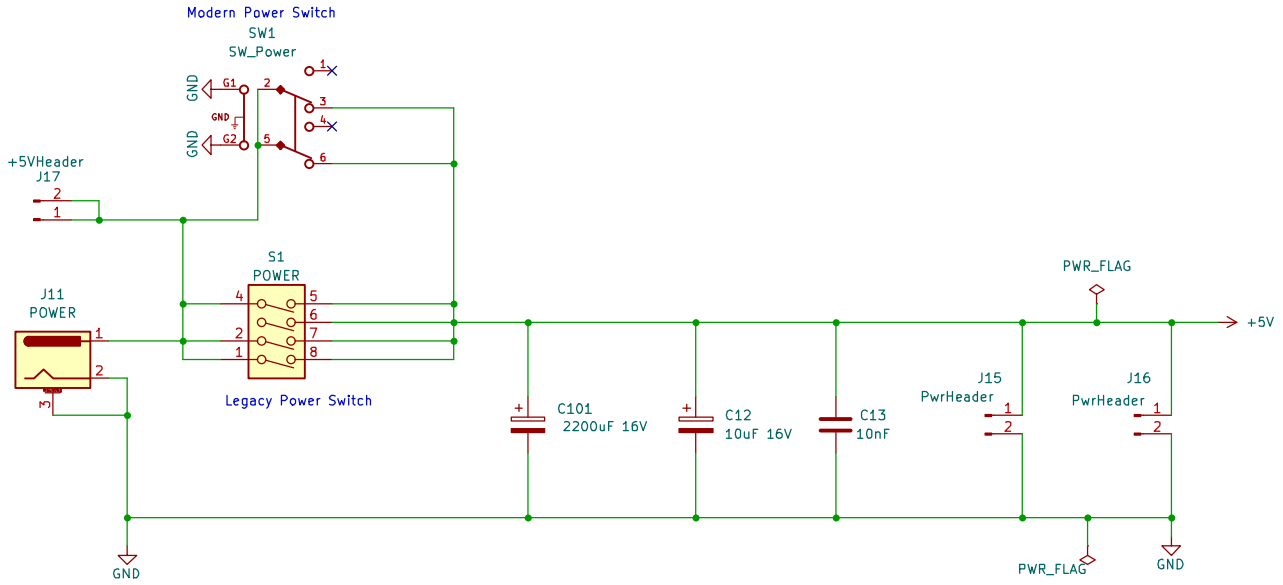

Mark Pruden

Sheet: /EXPANSION-I-O/

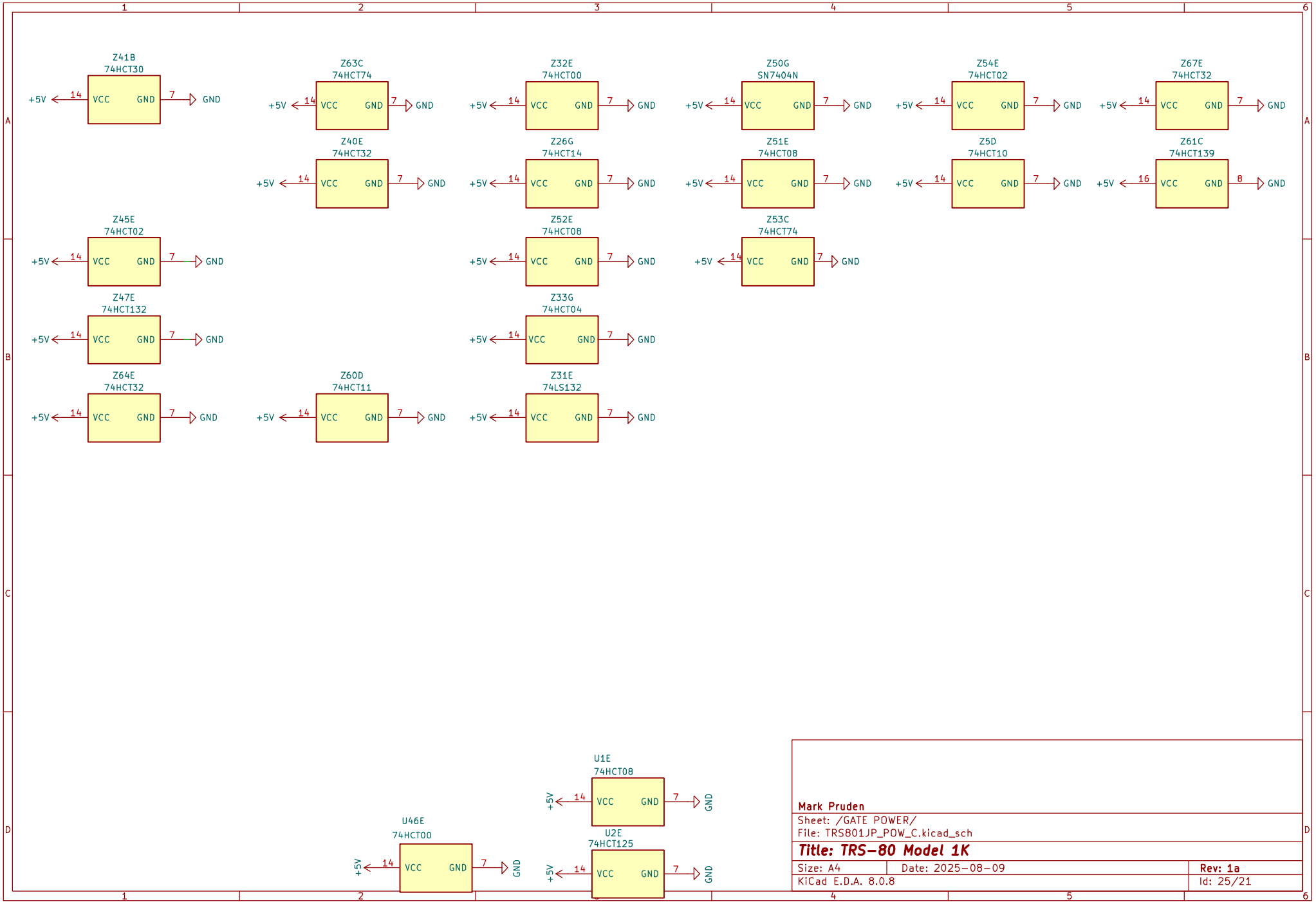
File: TRS80IJP_KEYBOARD.kicad_sch

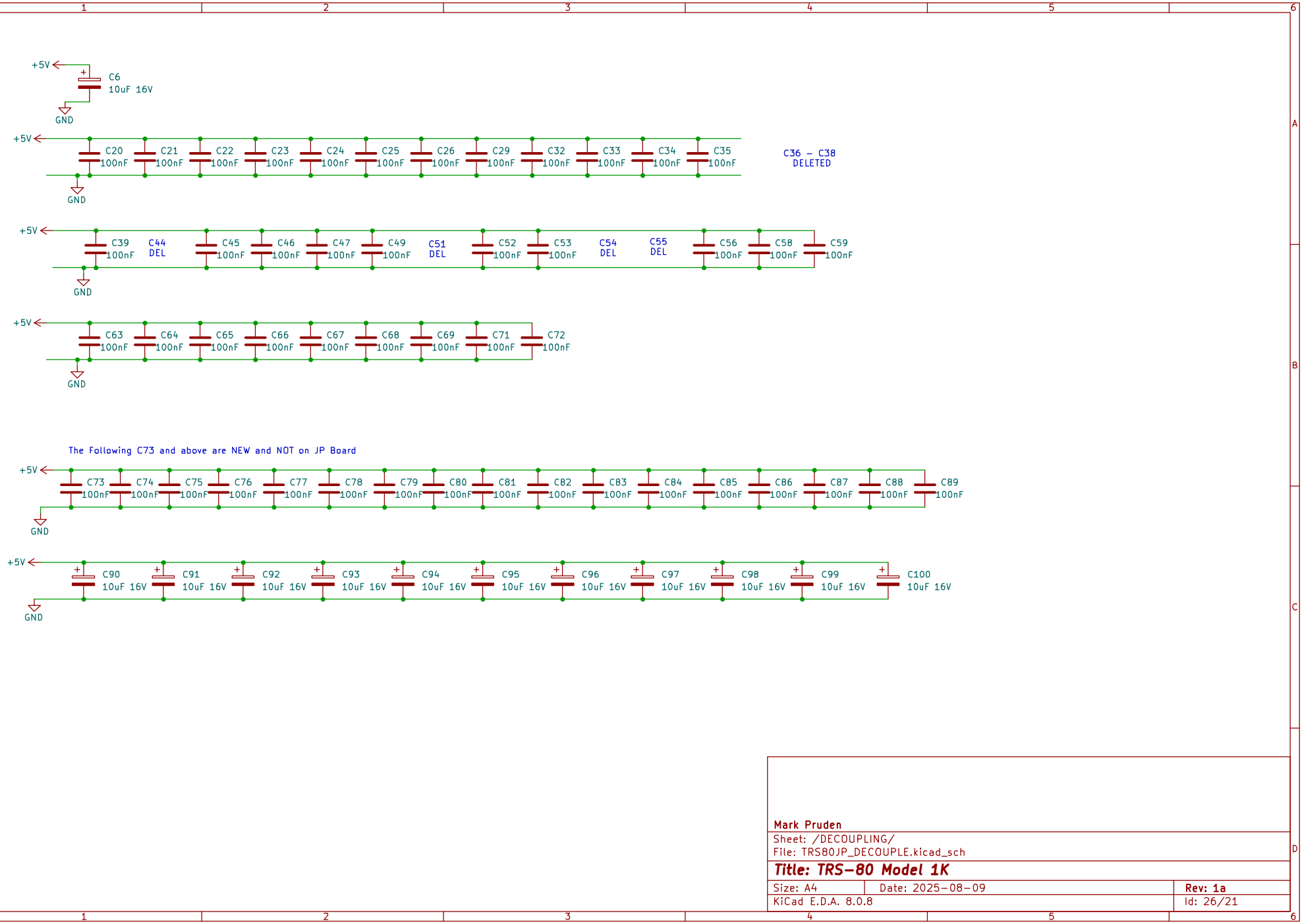
**Title: TRS-80 Model 1K**

| | | |
|---|---|---|
| Size: A4 | Date: 2025-08-09 | Rev: 1a |
| KiCad E.D.A. 8.0.8 | | Id: 22/21 |




| | | |
|---|---|---|
| Mark Pruden | | |
| Sheet: /POWER/ | | |
| File: TRS80IJP_POWER.kicad_sch | | |
| **Title: TRS-80 Model 1K** | | |
| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
| KiCad E.D.A. 8.0.8 | | Id: 23/21 |


Z41B
74HCT30
Z63C
74HCT74
Z32E
74HCT00
Z50G
SN7404N
Z54E
74HCT02
Z67E
74HCT32
Z40E
74HCT32
Z26G
74HCT14
Z51E
74HCT08
Z5D
74HCT10
Z61C
74HCT139
Z45E
74HCT02
Z52E
74HCT08
Z53C
74HCT74
Z47E
74HCT132
Z33G
74HCT04
Z64E
74HCT32
Z60D
74HCT11
Z31E
74LS132
U1E
74HCT08
U46E
74HCT00
U2E
74HCT125
+5V
GND
VCC
Mark Pruden
Sheet: /GATE POWER/
File: TRS801JP_POW_C.kicad_sch
Title: TRS-80 Model 1K
Size: A4
Date: 2025-08-09
Rev: 1a
KiCad E.D.A. 8.0.8
Id: 25/21




Mark Pruden

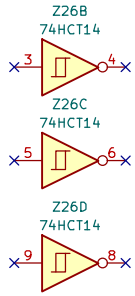
Sheet: /DECOUPLING/

File: TRS80JP_DECOUPLE.kicad_sch

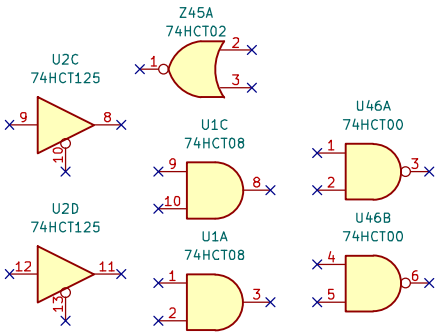
**Title: TRS-80 Model 1K**

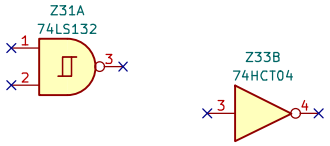
| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
|---|---|---|
| KiCad E.D.A. 8.0.8 | | Id: 26/21 |

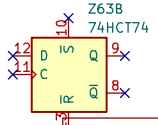
# Spare Gates are SHOWN in general PHYSICAL LOCATION on the Board



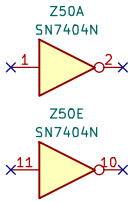

think move 2 used Inverters to NAND and Delete Inverters

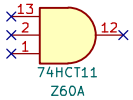



NOTE From Tech Manual –> REMOVED this and Grounded Pins Notice pins 6 and 7 of Z58. These inputs are used to clear the counter to zero. If you find CTR on sheet 1, you will see it comes from inverter Z42, pin 8, which controls the CPU CLK divider. Normally, CTR is held low. Only during automatic testing at the factory is CTR allowed to go high and clear Z58. You might find "A" and "D" Level Boards with Z58, pins 6 and 7, simply tied to ground.

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Sheet: /SPARE GATES/

File: TRS80IJP_SPARE.kicad_sch

**Title: TRS-80 Model 1K**

| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
|---|---|---|
| KiCad E.D.A. 8.0.8 | | Id: 27/21 |

## MOUNTING HOLES

H1
MountingHole

H2
MountingHole

H3
MountingHole

H4
MountingHole

H5
MountingHole

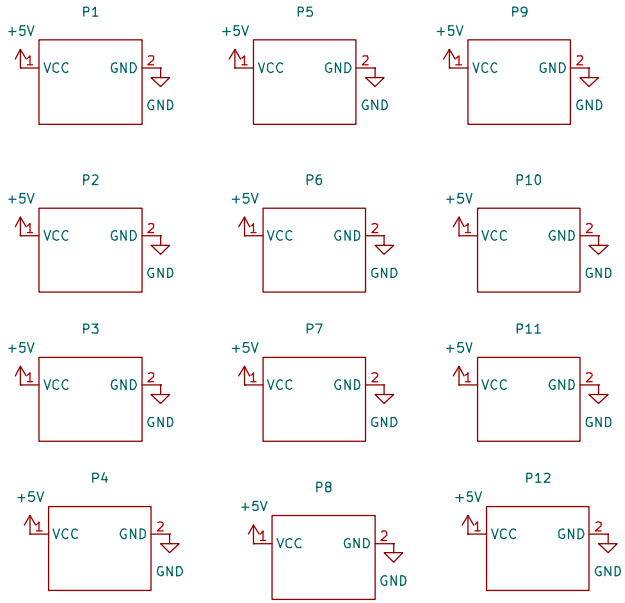
H6
MountingHole

H7
MountingHole

H9
MountingHole

H8
MountingHole

## PROTOTYPE AREAS




Mark Pruden
Sheet: /HARDWARE/
File: TRS801JP_HW.kicad_sch

**Title: TRS-80 Model 1K**

| Size: A4 | Date: 2025-08-09 | **Rev: 1a** |
|---|---|---|
| KiCad E.D.A. 8.0.8 | | Id: 28/21 |