HW#3 (Due 11/13)

1. Consider a *dynamic pipeline* with the following assumptions:

i. Function units are not pipelined. There is 1 FP adder, 1 integer ALU for LD/SD, 1 integer ALU for other integer operations. However, there are 2 FP multipliers.

ii. There is no forwarding between function units: results are communicated by the CDB.

iii. The execution stage (EX) does both the effective address calculation and memory access for loads and stores. The EX stage for loads and stores take 1 clock cycle.

iv. The IS and WB stages each take 1 clock cycle.

v. There are four FU types with the information shown below.

FU type	Cycles in EX	Numbers of FUs	Numbers of RSs
Integer (address calculation for LD and SD)	See iii	1	4 (2 for LD, 2.for SD)
Integer ALU	1	1	4
FP Adder	2	1	4
FP Multiplier	15	2	4

vi. A queued instruction in a reservation station may **execute** in the **same** clock cycle that the previous instruction writes to the CDB.

vii. A data dependent instruction begins to **execute** in the clock **after** the data value is broadcasted on the CDB.

viii. There are 2 load buffer slots and 2 store buffer slots.

ix. There are 4 integer ALU reservation stations, 4 FP adder reservation stations, and 4 FP multiplier reservation stations.

x. There is only one CDB. In case of CDB contention, the earliest issued instruction gets the priority.

Suppose the pipeline is a **two**-issue Tomasulo pipeline **without** speculation and ROB. Show the starting time of IS, IE, and WR for the code sequence shown below.

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SUB.D.      F1,F6,F5;
ADD.D.      F2,F4,F6;
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ADD.D.	F7,F1,F9;
MUL.D	F13,F10,F1;
MUL.D	F15,F10,F2;
ADD.D	F11,F2,F7;
L.D.	F17,4(R2);
L.D	F19,8(R2);

Please use the following table for your answer.

Instructions		Issues at	Executes at	Writes CDB at	Comments
SUB.D.	F1,F6,F5;	1	2	4	First issue
ADD.D.	F2,F4,F6;	1	4	6	Wait for SUB.D.
ADD.D.	F7,F1,F9;	2	6	8	Wait for ADD.D.
MUL.D	F13,F10,F1;	2	5	20	Wait for SUB.D.
MUL.D	F15,F10,F2;	3	7	22	Wait for ADD.D
ADD.D	F11,F2,F7;	3	9	11	Wait for ADD.D
L.D.	F17,4(R2);	4	5	7	Wait for CDB
L.D	F19,8(R2);	4	7	9	Wait for CDB