Homework #2 (due 10/30)

1.

Consider the execution of the following code segment

ADD.D	F4,F6,F1;
MUL.D	F6,F4,F3;
ADD.D	F9,F4,F7;
MUL.D	F1,F3,F7;

on an architecture which uses a scoreboard to dynamically schedule instructions on a pipeline (issue, read_operand, execute, write_back) with the following non-pipelined execution units:

1-cycle, Integer unit,2-cycle, FP add unit,3-cycle, FP multiply unit10-cycle, FP divide unit

Suppose the pipeline contains only one integer unit, two FP add units, one FP multiply units, and one FP divide unit. Trace the execution by showing the instruction status, the functional unit status and the register result status at clock cycles 1, 2, 3, 4 and 5.

Hint:

At Clock Cycle 1:

	Instruction status								
Instructions	Issue	Read operands	Execution complete	Write result					
ADD.D F4,F6,F1;	1								
MUL.D F6,F4,F3;									
ADD.D F9,F4,F7;									
MUL.D F1,F3,F7;									

	Function unit status									
Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk	
Integer										
Mult										
Add1	Yes	ADD.D	F4	F6	F1			Yes	Yes	
Add2										
Divide										

<u>'</u>					Regi	ster Res	ult Stat	us				
	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	
FU					Add1							

Please show the tables for each and every clock for clocks 2, 3, 4 and 5.

At Clock Cycle 2:

		Instruction status								
Instructions	Issue	Read operands	Execution complete	Write result						
ADD.D F4,F6,F1;	1	2								
MUL.D F6,F4,F3;	2									
ADD.D F9,F4,F7;										
MUL.D F1,F3,F7;										

		Function unit status										
Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk			
Integer												
Mult	Yes	MUL.D	F6	F4	F3	Add1		No	Yes			
Add1	Yes	ADD.D	F4	F6	F1			Yes	Yes			
Add2												
Divide												

					Regis	ter Res	sult Statu	ıs				
	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	
FU					Add1		Mult					

At Clock Cycle 3:

		Instruction status								
Instructions	Issue	Read operands	Execution complete	Write result						
ADD.D F4,F6,F1;	1	2								
MUL.D F6,F4,F3;	2									
ADD.D F9,F4,F7;	3									
MUL.D F1,F3,F7;										

				Func	ction unit	status				
Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk	
Integer										

Mult	Yes	MUL.D	F6	F4	F3	Add1	No	Yes
Add1	Yes	ADD.D	F4	F6	F1		No	No
Add2	Yes	ADD.D	F9	F4	F7	Add1	No	Yes
Divide								

					Regis	ter Res	ult Stat	us			
	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
FU					Add1		Mult			Add2	

At Clock Cycle 4:

		Instruction status								
Instructions	Issue	Read operands	Execution complete	Write result						
ADD.D F4,F6,F1;	1	2	4							
MUL.D F6,F4,F3;	2									
ADD.D F9,F4,F7;	3									
MUL.D F1,F3,F7;										

				Funct	tion unit	status			
Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer									
Mult	Yes	MUL.D	F6	F4	F3	Add1		No	Yes
Add1	Yes	ADD.D	F4	F6	F1			No	No
Add2	Yes	ADD.D	F9	F4	F7	Add1		No	Yes
Divide									

					Regis	ter Res	ult Stati	18			
	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
FU				•	Add1		Mult			Add2	

At Clock Cycle 5:

			Instruction status	
Instructions	Issue	Read operands	Execution complete	Write result
ADD.D F4,F6,F1;	1	2	4	5
MUL.D F6,F4,F3;	2			
ADD.D F9,F4,F7;	3			
MUL.D F1,F3,F7;				

	Function unit status										
Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk		
Integer											
Mult	Yes	MUL.D	F6	F4	F3			Yes	Yes		
Add1	No										
Add2	Yes	ADD.D	F9	F4	F7			Yes	Yes		
Divide											

	Register Result Status										
	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
FU							Mult			Add2	