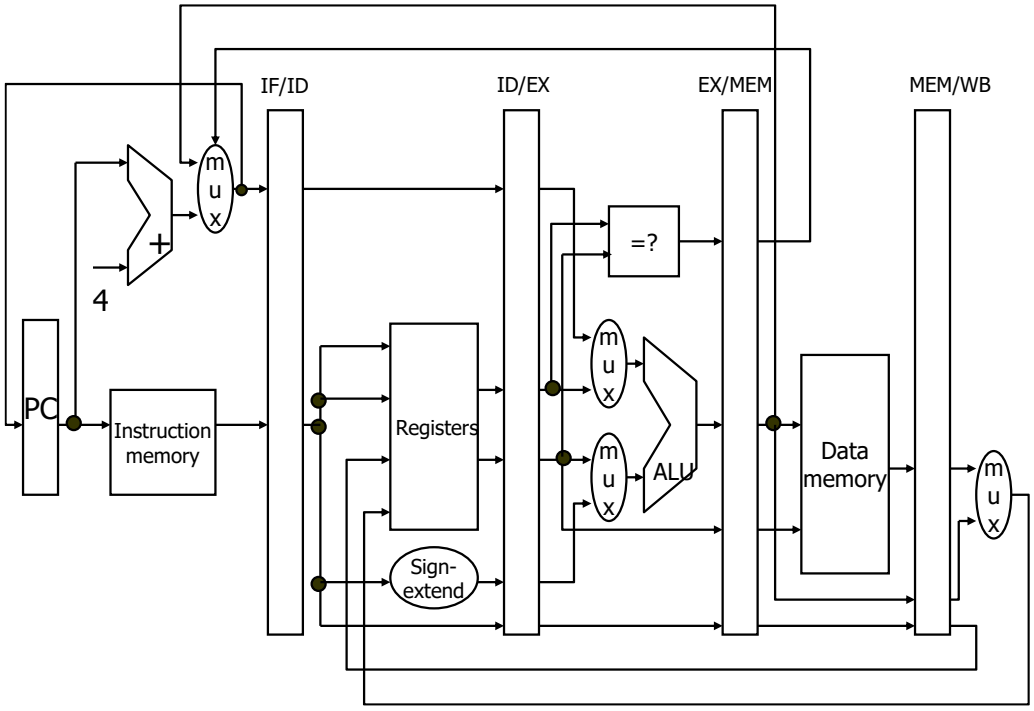
Advanced Computer Architecture
HW#1 (Due: 10/16)

1. Consider the simple 5-stage pipeline as shown below.



Suppose *forwarding* technique with interlock is employed. Consider the following instruction sequence.

```
add     x1, x2, x3;
add     x5, x6, x1;
ld      x4, 20(x8);
and     x7, x9, x4;
sd      x7, 32(x8);
```

(a) Show the timing of the execution in Table I.

Table I

Instruction		Clock Cycle													
		1	2	3	4	5	6	7	8	9	10	11	12	13	14
add	x1, x2, x3;	IF	ID	EX	MEM	WB									
add	x5, x6, x1;		IF	ID	EX	MEM	WB								
ld	x4, 20(x8);			IF	ID	EX	MEM	WB							
and	x7, x9, x4;				IF	ID	Stall	EX	MEM	WB					
sd	x7, 32(x8);					IF	Stall	ID	EX	MEM	WB				

(b) Show the timing of the execution in Table II.

Table II

Clock	Stages				
Cycles	IF	ID	EX	MEM	WB
1	ADD				
2	ADD	ADD			
3	LD	ADD	ADD		
4	AND	LD	ADD	ADD	
5	SD	AND	LD	ADD	ADD
6	SD	AND		LD	ADD
7		SD	AND		LD
8			SD	AND	
9				SD	AND
10					SD

(c) Determine the average clocks per instruction (CPI) of the code sequence.

CPI = 10 / 5 = 2

2.

Consider the following sequence.

```
        add     x1, x2, x3;
        beq     x1, x10, Target1;
        or      x12, x11, x4;
        add     x7, x5, x1;
        sub     x6, x7, x3;
Target1: add    x1, x6, x5;
        sd      x1, 64(x6);
```

Suppose the sequence is executed in the pipeline shown in Problem 1. **Assume the branch is taken.** Show the timing of the execution in Table III

Table III

Instruction			Clock Cycle												
			1	2	3	4	5	6	7	8	9	10	11	12	13	14
	add	x1, x2, x3;	IF	ID	EX	MEM	WB									
	beq	x1, x10, Target1;		IF	ID	EX	MEM	WB								
	or	x12, x11, x4;			IF	ID	EX	IDLE	IDLE							
	add	x7, x5, x1;				IF	ID	IDLE	IDLE	IDLE						
	sub	x6, x7, x3;					IF	IDLE	IDLE	IDLE	IDLE					
Target1:	add	x1, x6, x5;						IF	ID	EX	MEM	WB				
	sd	x1, 64(x6);							IF	ID	EX	MEM	WB			