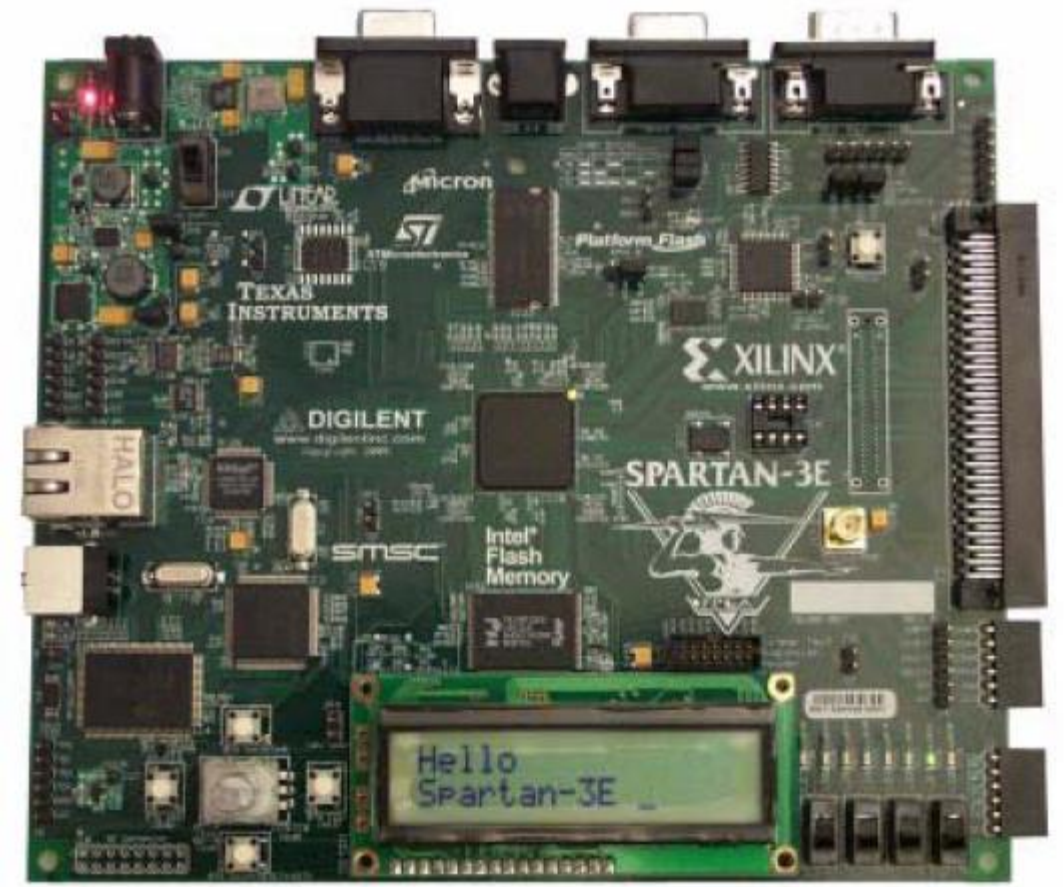
SPARTAN 3E STARTER BOARD

Fabio Schygiel

Diseño de Sistemas con FPGA

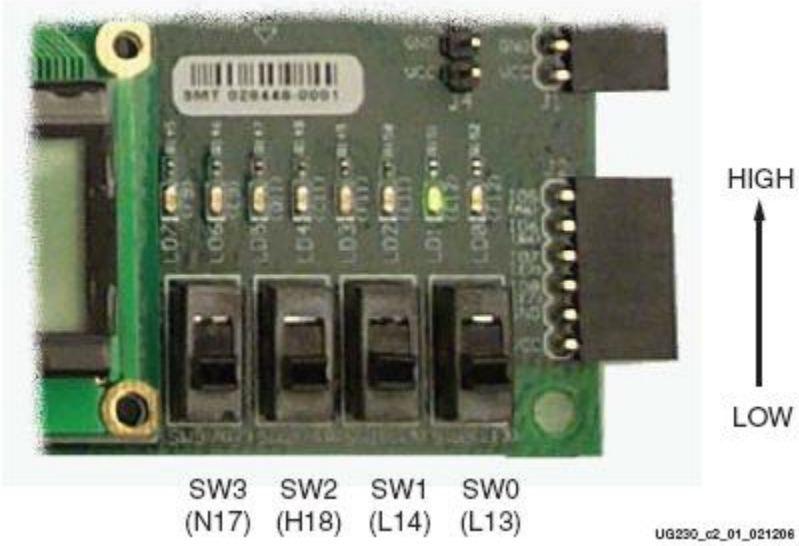
Placa de desarrollo Spartan 3E Starter



Características Principales

- Xilinx XC3S500E Spartan-3E FPGA
- Xilinx 4 Mbit Platform Flash configuration PROM
- Xilinx 64-macrocell XC2C64A CoolRunner CPLD
- 64 MByte (512 Mbit) of DDR SDRAM, x16 data interface, 100+ MHz
- 16 MByte (128 Mbit) of parallel NOR Flash (Intel StrataFlash)
- 16 Mbits of SPI serial Flash (STMicro)
- 2-line, 16-character LCD screen
- PS/2 mouse or keyboard port
- VGA display port
- 10/100 Ethernet PHY (requires Ethernet MAC in FPGA)
- Two 9-pin RS-232 ports (DTE- and DCE-style)
- On-board USB-based FPGA/CPLD download/debug interface
- 50 MHz clock oscillator
- SHA-1 1-wire serial EEPROM for bitstream copy protection
- Hirose FX2 expansion connector
- Three Digilent 6-pin expansion connectors
- Four-output, SPI-based Digital-to-Analog Converter (DAC)
- Two-input, SPI-based Analog-to-Digital Converter (ADC) with programmable-gain
- pre-amplifier
- ChipScope™ SoftTouch debugging port
- Rotary-encoder with push-button shaft
- Eight discrete LEDs
- Four slide switches

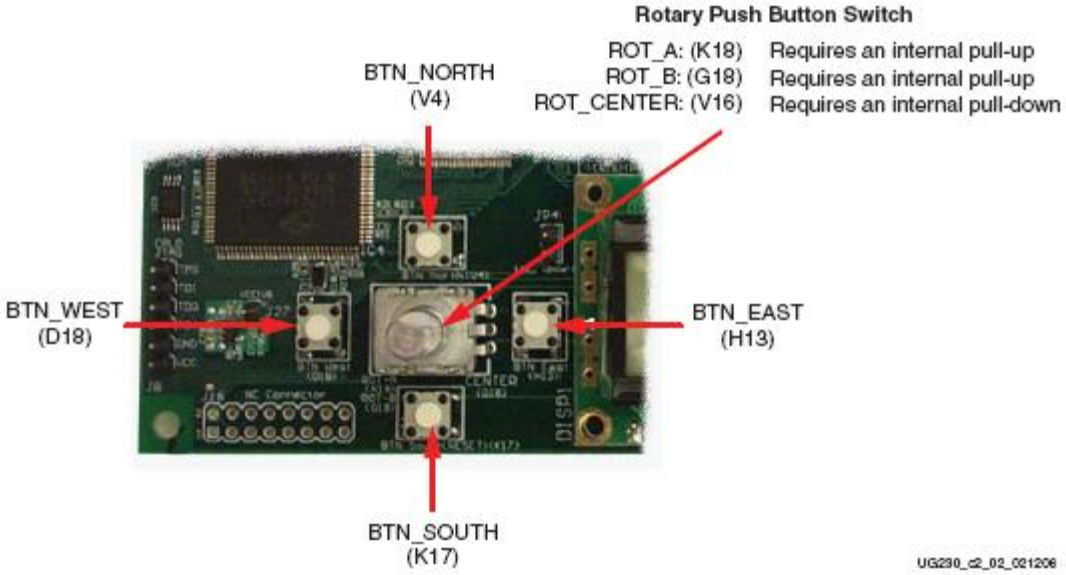
Primero lo conocido, switches




```
NET "SW<0>" LOC = "L13" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<1>" LOC = "L14" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<2>" LOC = "H18" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<3>" LOC = "N17" | IOSTANDARD = LVTTL | PULLUP ;
```

Push Buttons

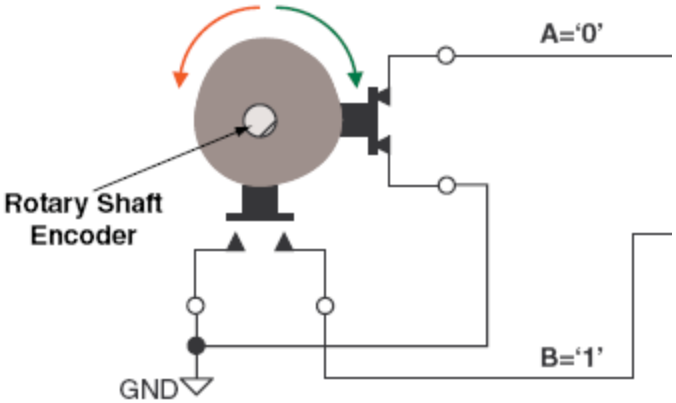
- No hay circuito antirebote en los botones, hay que implementarlos en la FPGA!



- NET "BTN_EAST" LOC = "H13" | IOSTANDARD = LVTTL | PULLDOWN ;
- NET "BTN_NORTH" LOC = "V4" | IOSTANDARD = LVTTL | PULLDOWN ;
- NET "BTN_SOUTH" LOC = "K17" | IOSTANDARD = LVTTL | PULLDOWN ;
- NET "BTN_WEST" LOC = "D18" | IOSTANDARD = LVTTL | PULLDOWN ;

Algo nuevo,Rotary Push Button Switch

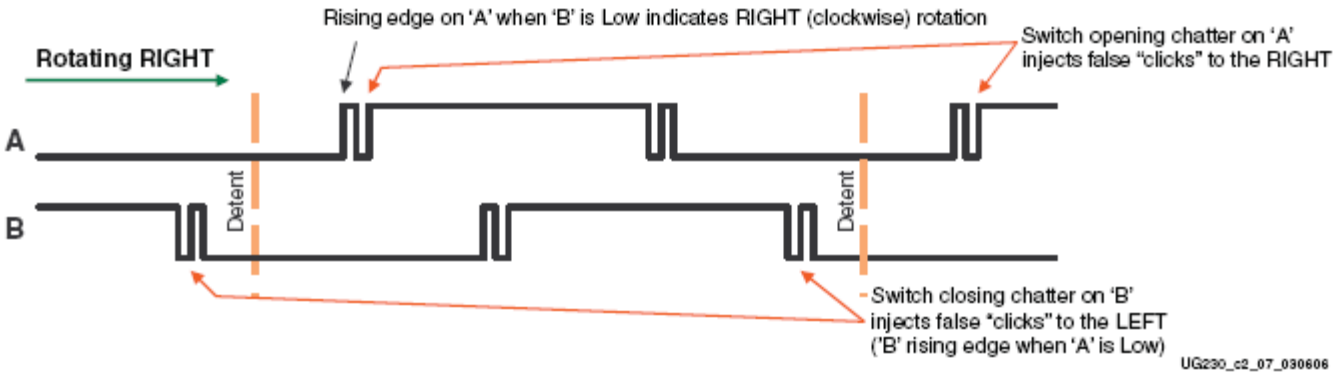
- Dos funciones en uno.
- Push Button Switch, actua como un push button común.
- Rotary Shaft Encoder, actua como dos push buttons. Dependiendo de la dirección de giro se cierra un switch antes que el otro. Cuando esta detenido ambos switchs estan cerrados (‘0’).



- NET "ROT_A" LOC = "K18" | IOSTANDARD = LVTTL | PULLUP ;
- NET "ROT_B" LOC = "G18" | IOSTANDARD = LVTTL | PULLUP ;
- NET "ROT_CENTER" LOC = "V16" | IOSTANDARD = LVTTL | PULLDOWN ;

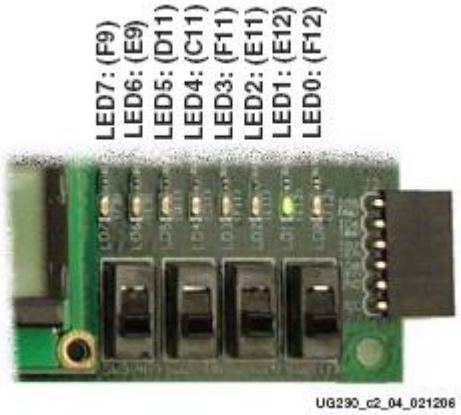
¿Hacia que lado gira?

- Un flanco ascendente en ROT_A mientras ROT_B esta bajo indica un giro en el sentido de las agujas del reloj.
- Un flanco ascendente en ROT_B cuando ROT_A esta bajo indica giro en el sentido contrario a las agujas del reloj.
- Debe considerarse un efecto llamado “chatter” similar al rebote de los push buttons que puede provocar falsos giros.



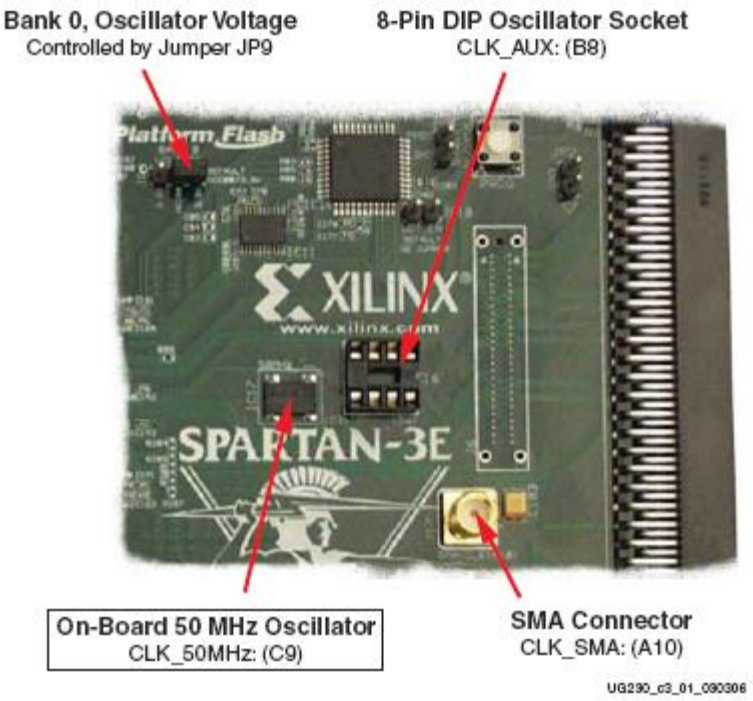
Sacando datos, la forma fácil

- Los leds se encienden colocando un ‘1’ en la señal correspondiente de la FPGA.




```
NET "LED<7>" LOC = "F9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<6>" LOC = "E9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<5>" LOC = "D11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<4>" LOC = "C11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<3>" LOC = "F11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<2>" LOC = "E11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<1>" LOC = "E12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED<0>" LOC = "F12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
```

Reloj, ¿que tan rápido vamos?



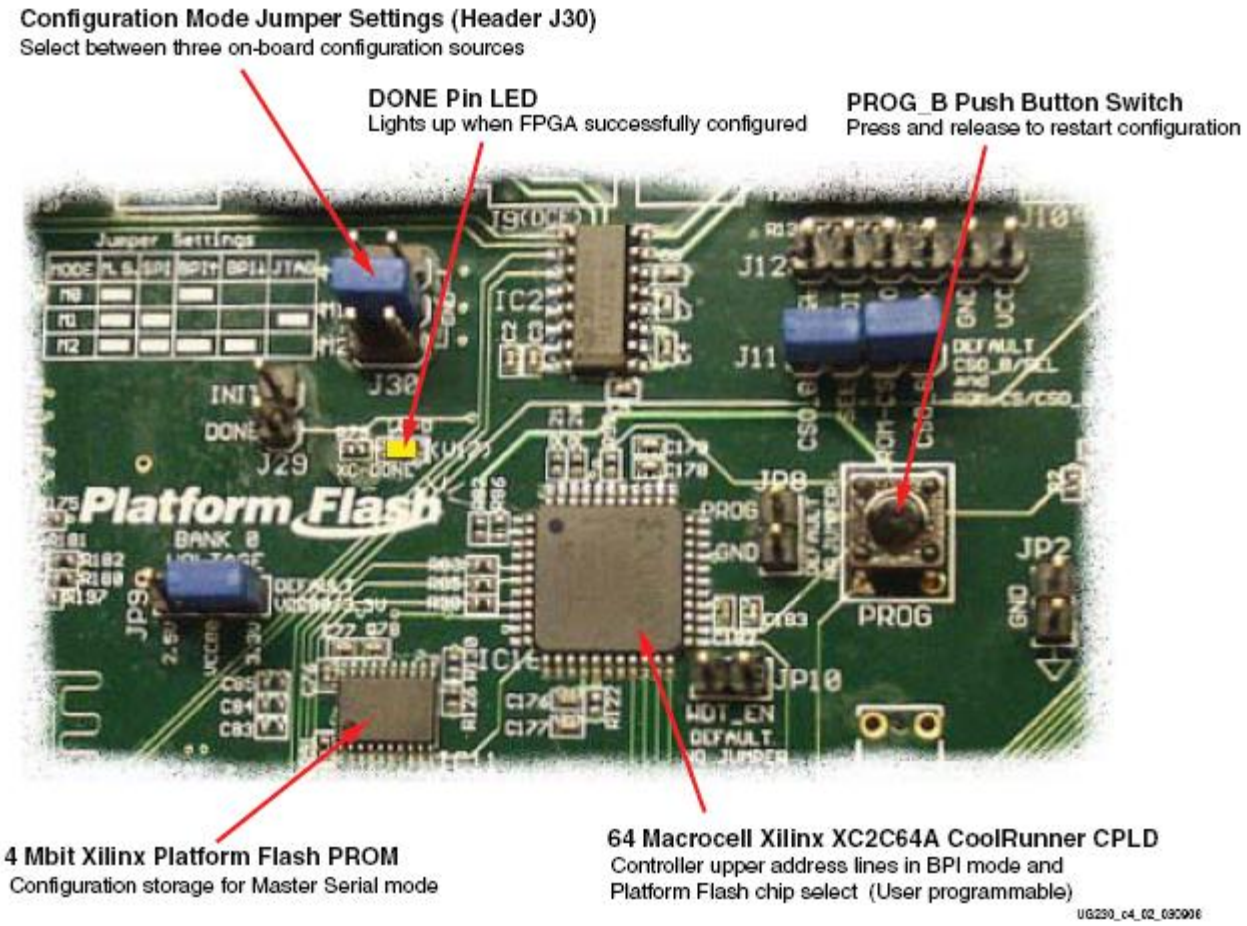

```
NET "CLK_50MHZ" LOC = "C9" | IOSTANDARD = LVCMOS33 ;
NET "CLK_SMA" LOC = "A10" | IOSTANDARD = LVCMOS33 ;
NET "CLK_AUX" LOC = "B8" | IOSTANDARD = LVCMOS33 ;
# Define clock period for 50 MHz oscillator
NET "CLK_50MHZ" PERIOD = 20.0ns HIGH 40%;
```

¿Como la programamos?

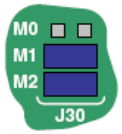
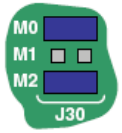
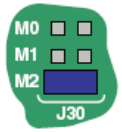
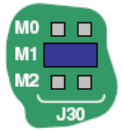
Tenemos varios modos de programar la FPGA

- Enviar diseños directamente a la FPGA via JTAG, utilizando la interfaz USB de la placa.
- Programar la Xilinx XCF04S serial Platform Flash PROM y configurar la FPGA desde la imagen guardado utilizando el modo Master Serial.
- Programar la Microelectronics SPI serial Flash PROM y configurar la FPGA desde la imagen guardado utilizando el modo SPI.
- Programar la Intel StrataFlash parallel NOR Flash PROM y configurar la FPGA desde la imagen guardada utilizando los modos BPI Up o BPI down.

Jumpers y botón de programación

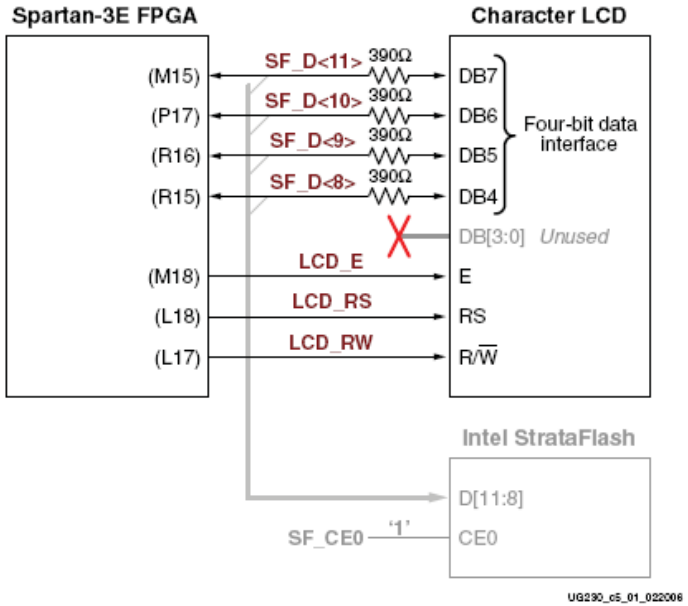


Seleccionando el origen

Configuration Mode	Mode Pins M2:M1:M0	FPGA Configuration Image Source	Jumper Settings
Master Serial	0:0:0	Platform Flash PROM	
SPI (see Chapter 12, "SPI Serial Flash")	1:1:0	SPI Serial Flash PROM starting at address 0	
BPI Up (see Chapter 11, "Intel StrataFlash Parallel NOR Flash PROM")	0:1:0	StrataFlash parallel Flash PROM, starting at address 0 and incrementing through address space. The CPLD controls address lines A[24:20] during BPI configuration.	
BPI Down (see Chapter 11, "Intel StrataFlash Parallel NOR Flash PROM")	0:1:1	StrataFlash parallel Flash PROM, starting at address 0x1FF_FFFF and decrementing through address space. The CPLD controls address lines A[24:20] during BPI configuration.	
JTAG	0:1:0	Downloaded from host via USB-JTAG port	

Mejorando la salida, LCD

La placa cuenta con un LCD de 2 líneas x 16 caracteres.




```
NET "LCD_E" LOC = "M18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "LCD_RS" LOC = "L18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "LCD_RW" LOC = "L17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "SF_D<8>" LOC = "R15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "SF_D<9>" LOC = "R16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "SF_D<10>" LOC = "P17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "SF_D<11>" LOC = "M15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
```

Evitando escribir en dos partes

Si bien el LCD soporta una interface de 8 bits, la placa utiliza una interfaz de 4 bits.

Las líneas de datos son compartidas con la StrataFlash.

Para evitar escribir / leer de ambos componentes deben activarse / desactivarse los mismo.

Existe un modo de operación de la StrataFlash (en 8 bits) que permite utilizarlos en forma simultanea.

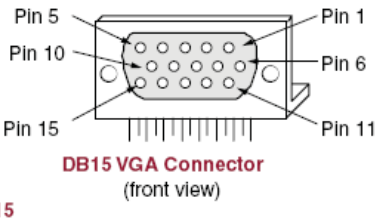
SF_CE0	SF_BYTE	LCD_RW	Operation
1	X	X	StrataFlash disabled. Full read/write access to LCD.
X	X	0	LCD write access only. Full access to StrataFlash.
X	0	X	StrataFlash in byte-wide (x8) mode. Upper data lines are not used. Full access to both LCD and StrataFlash.

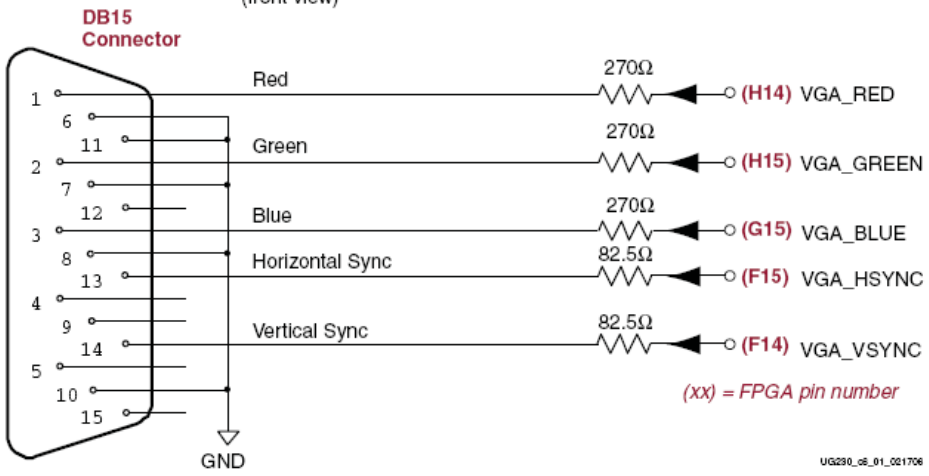
Control y datos

Signal Name	FPGA Pin	Function	
SF_D<11>	M15	Data bit DB7	Shared with StrataFlash pins SF_D<11:8>
SF_D<10>	P17	Data bit DB6	
SF_D<9>	R16	Data bit DB5	
SF_D<8>	R15	Data bit DB4	
LCD_E	M18	Read/Write Enable Pulse 0: Disabled 1: Read/Write operation enabled	
LCD_RS	L18	Register Select 0: Instruction register during write operations. Busy Flash during read operations 1: Data for read or write operations	
LCD_RW	L17	Read/Write Control 0: WRITE, LCD accepts data 1: READ, LCD presents data	

Para los amantes del video

La placa tiene un puerto de video VGA con un conector DB15.

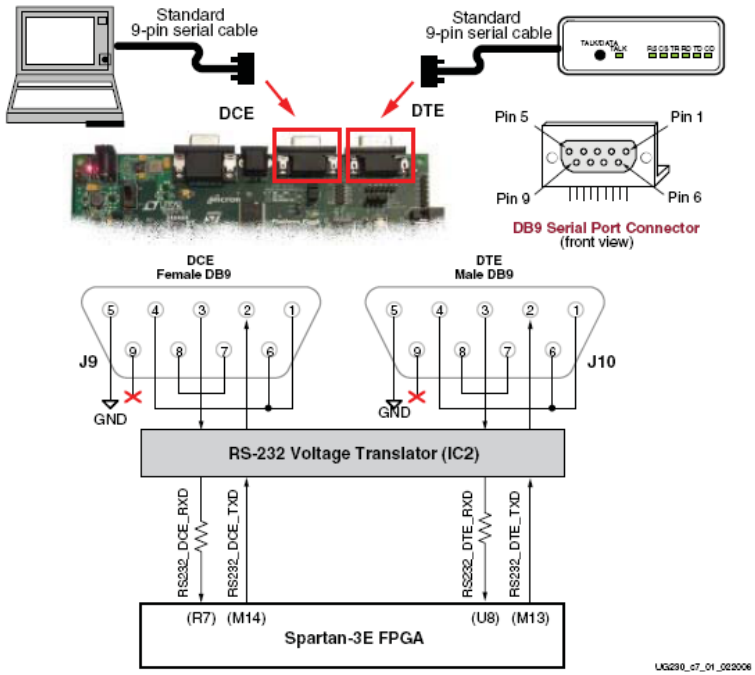





```
NET "VGA_RED" LOC = "H14" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = FAST ;
NET "VGA_GREEN" LOC = "H15" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = FAST ;
NET "VGA_BLUE" LOC = "G15" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = FAST ;
NET "VGA_HSYNC" LOC = "F15" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = FAST ;
NET "VGA_VSYNC" LOC = "F14" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = FAST ;
```

I/O como en los viejos tiempos

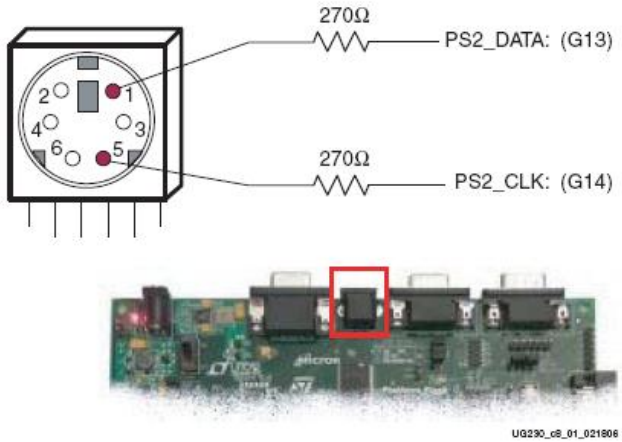
La placa tiene dos puertos serie RS-232, un conector hembra DB9 DCE y un macho DTE.




```
NET "RS232_DTE_RXD" LOC = "U8" | IOSTANDARD = LVTTL ;
NET "RS232_DTE_TXD" LOC = "M13" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = SLOW ;
NET "RS232_DCE_RXD" LOC = "R7" | IOSTANDARD = LVTTL ;
NET "RS232_DCE_TXD" LOC = "M14" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = SLOW ;
```

Ingreso de datos manual

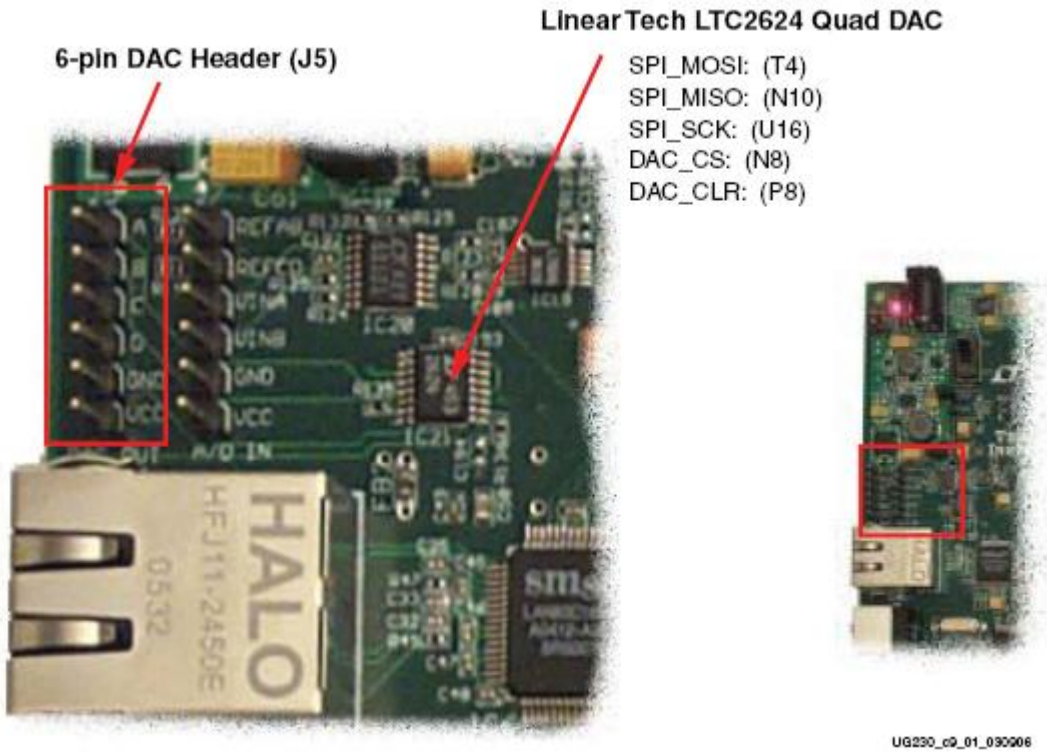
Para el ingreso de datos manual la placa tiene un puerto PS/2 donde puede conectarse un mouse o teclado.



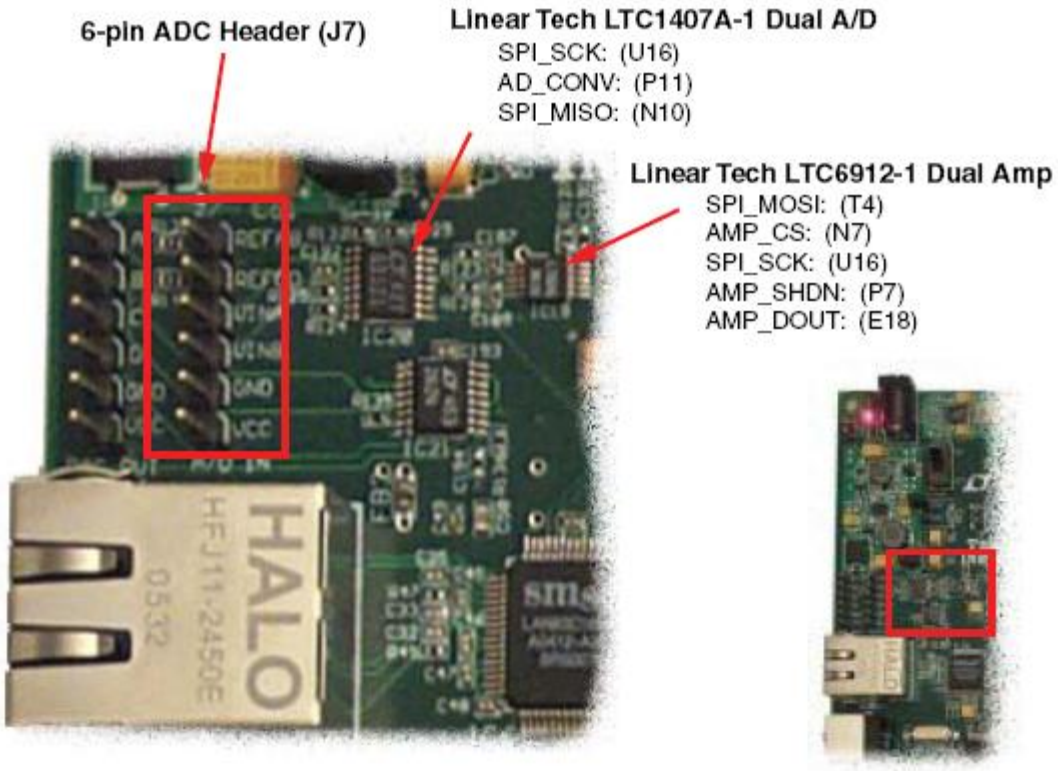
PS/2 DIN Pin	Signal	FPGA Pin
1	DATA (PS2_DATA)	G13
2	Reserved	G13
3	GND	GND
4	+5V	—
5	CLK (PS2_CLK)	G14
6	Reserved	G13

```
NET "PS2_CLK" LOC = "G14" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
NET "PS2_DATA" LOC = "G13" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
```

Conversor Digital/Analógico

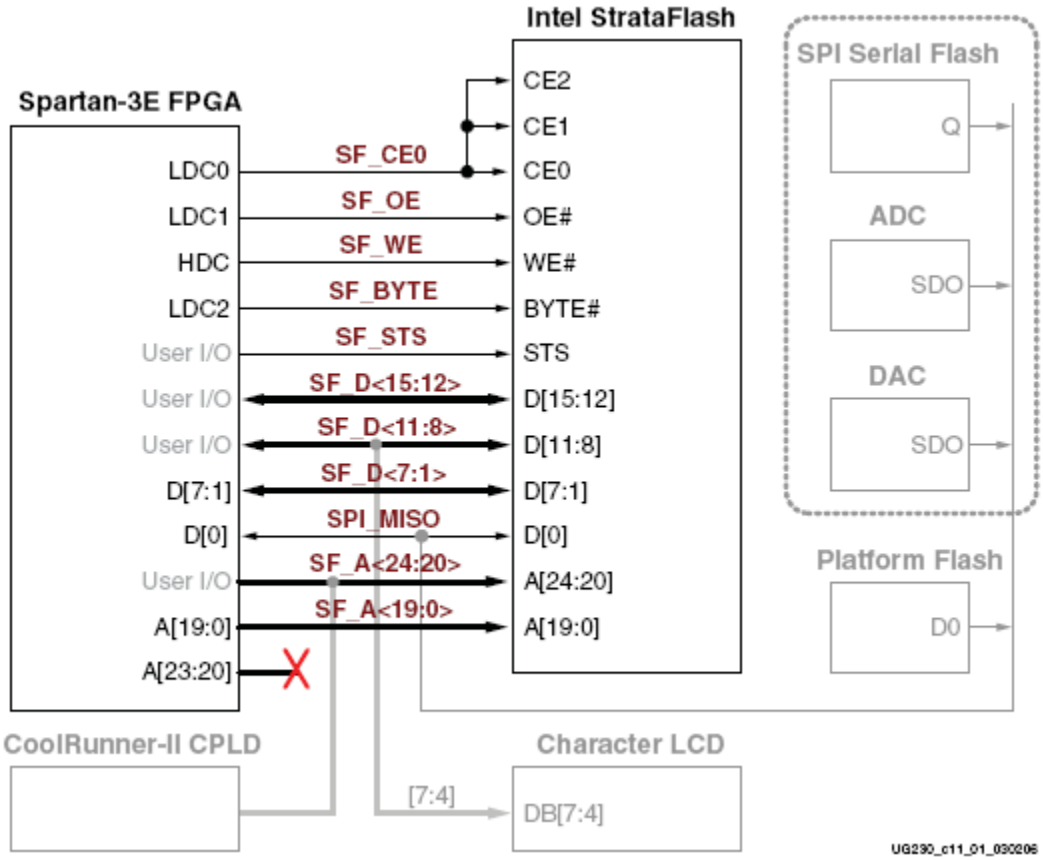


Captura Analógica



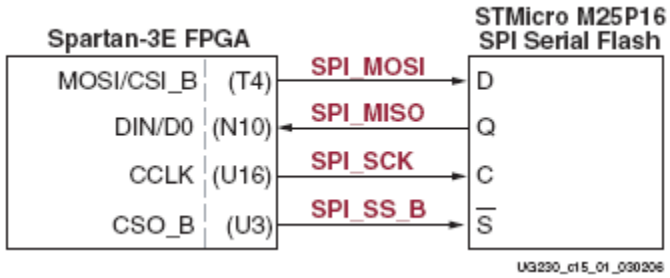
Memoria, memoria, memoria

La placa contiene una **Intel StrataFlash parallel NOR Flash PROM** de 128 Mbit (16 Mbyte).



Memoria, memoria, memoria

La placa contiene una **STMicroelectronics M25P16 16 Mbit SPI serial Flash**.




```
NET "SPI_MISO" LOC = "N10" | IOSTANDARD = LVCMOS33 ;
NET "SPI_MOSI" LOC = "T4" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;
NET "SPI_SCK" LOC = "U16" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;
NET "SPI_SS_B" LOC = "U3" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;
NET "SPI_ALT_CS_JP11" LOC = "R12" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;
```

Memoria, memoria, memoria

La placa contiene una **512 Mbit (32M x 16) Micron Technology DDR SDRAM** (MT46V32M16)

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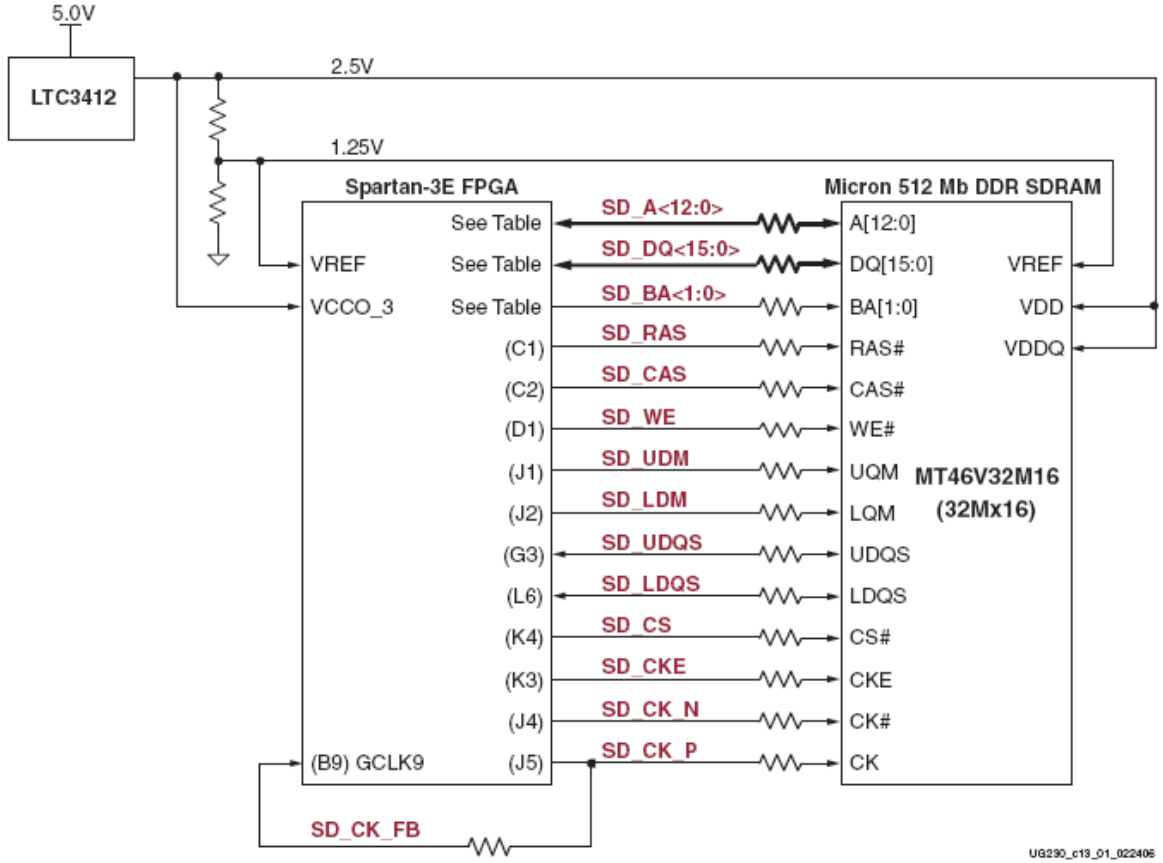
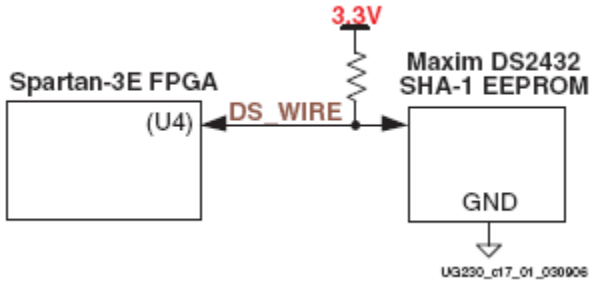
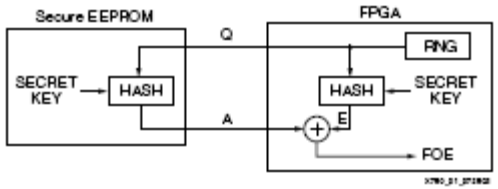


Seguridad, amigo/enemigo

La placa contiene una Maxim DS2432 serial EEPROM, la cual cuenta con:

- 64-bit read-only unique serial number (no two devices share the same ID)
- 64-bit write-only secret key that can be rewritten at any time, but there is no way of reading it back
- Secure Hash Algorithm (SHA-1) cryptographic engine






```
NET "DS_WIRE" LOC = "U4" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;
```

Conectandose con el mundo

La placa incluye una interfaz Ethernet con un conector RJ45. Para utilizarlo debe implementarse en la FPGA un Ethernet Media Access Controller (MAC). Para facilitar esto un IP core para utilizar en forma conjunta con el MicroBlaze es parte del EDK.