Translásia.	Materia:	Process Automation Laboratory
Tecnológico de Monterrey	Grupo:	
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	Práctica:	4. Logic Control Systems
Campus Estado de México	Fecha de entrega:	
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# **Introduction (Previous Activity)**

- 1. Explain which are the rules and laws that are used to simplify logic functions in Boolean algebra.
- 2. Explain the postulates for the logic sum and for the logic product.
- 3. Explain the De Morgan's Theorems and the Duality Theorem.
- 4. Explain what are the Maxterms and the NOR universal gate.

### **Materials**

- 1 Dip Switch of 4 positions
- 3 resistor of 270 ohms
- 4 resistor of 330 ohms
- 2 LEDs
- 1 protoboard

- 1 digital multimeter
- 1 cut pliers
- 1 needled-nose pliers
- AND, OR, NOT, NAND, NOR gates
- Power Supply\*

# **Exercise 1: Verifying the Truth Table of Logic Functions.**

Connect the Dip switch, the resistors of 330 ohms, the electronic logic circuit (AND, OR, NOT, NAND and NOR) a 270 ohm resistor and the LED on the protoboard as shown in figure 1. Put the power supply at 5 VDC.

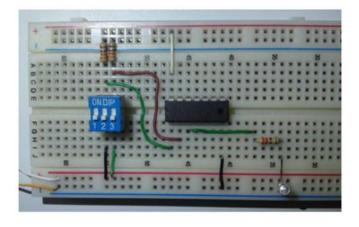


Figure 1 Truth Table Test Circuit

Turn on the power supply and Verify first the Truth Table for a 2 input AND gate. Turn off the power supply and change the AND gate with the OR gate, turn on the power supply and verify its Truth Table. Do the same for the NOT, NAND and NOR gates. Take pictures for each state of each logic function.

## **Exercise 2: Logic Combinatory Design**

A logic control circuit has to activate 2 electro-valves using 4 sensors. The first electro-valve will work when sensor 1 or sensor 2 are activated and also sensor 3 is activated but not sensor 4. The second electro-valve will turn on when sensor 2 and sensor 4 are activated and will turn off when sensor 1 and sensor 3 are activated simultaneously. Obtain the True Table, the simplified logic equations and the logic diagram. Build your solution on the protoboard, determining the number of AND, OR and NOT gates needed, the electro-valves are going to be simulated using LEDs.

### Discussion:

Which will be the simplified logic diagram of exercise 2 using only NAND gates? Write this diagram on your report.